A Novel Low-Voltage Cross-Coupled Passive Sampling Branch for Reset- and Switched-Opamp Circuits

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***Abstract*—This paper proposes a novel cross-coupled passive input sampling branch that can be applied to low-voltage switched- and reset-opamp circuits. The proposed circuit allows the direct passive interface from the external input signal to the 1st stage switched- and reset-opamp, directly providing a sample-and-hold-and-reset output without the use of an extra-stage of opamps as in the case of traditional interface designs that implement only track-and-reset output, thus saving one front-stage opamp power. Simulations with real switches in 1-V supply voltage are presented to verify the effectiveness of the proposed circuit.**

I. INTRODUCTION

Recent research results show that CMOS analog integrated circuits are becoming more and more difficult to design due to continuously decreasing supply voltage imposed by down-scaling of technology, for the reason that digital circuits can achieve greater benefits from speed (due to reduction in gate capacitance) and power (proportional to VDD^2) with reduced supply voltages and technology feature sizes. The same benefits do not appeared completely in analog and mixed signal designs that make use of switches and opamps, mainly due to the fact that the threshold voltage does not scale down linearly with supply voltage [1-6]. The main difficulties in very low-voltage circuit designs include mainly the inability to turn on the floating switches as the supply voltage is less than the sum of NMOS and PMOS threshold voltage, i.e. $V_{DD} < V_{thn} + |V_{thp}|$ [6]. Since the floating switches cannot be easily turned on, two state-of-the-art techniques, namely reset-opamp [3,6] and switched-opamp [2,4], are available to replace the floating switch problems in modern low-voltage designs. These two techniques do not require generation of on-chip higher voltages and thus are truly compatible with future low-voltage deep-submicron CMOS processes.

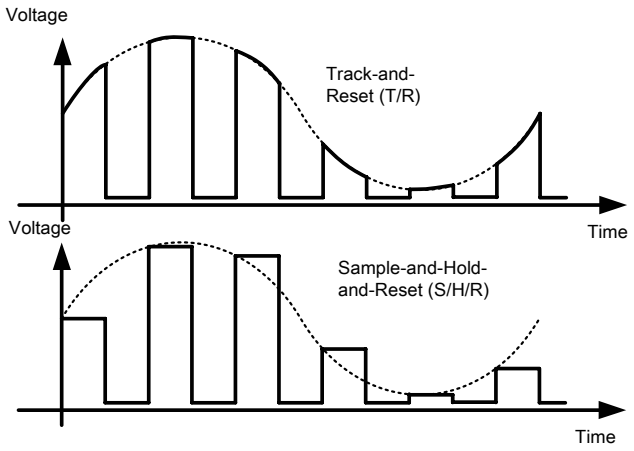

Fig. 1: Track-and-Reset (T/R) vs. Sample-and-Hold-and-Reset (S/H/R).

The reason why switched-opamp circuits can alleviate the floating switch problems is related with the replacement of such switches by the previous stage opamps that switch-off in one phase, thus turning-off the output from the opamps and simulating the switching function [2]. Similarly in reset-opamp circuits, the previous stage opamps are reset in one phase to discharge the next stage sampling capacitors [3,6]. It becomes evident that both techniques require opamps in the previous stage to simulate the switches, and an extra effort must be devoted to design the front-end input sampling circuits, since there are no such opamps preceding the foremost front-end stages that interface with external input signals (except for bandpass applications [4], for which a input coupling capacitor can be used to solve this problem).

Although several input interfaces have been proposed [2, 7-10], they can only either provide Track-and-Reset (T/R) output signals as shown in Fig. 1 [7-10] (thus an extra opamp must be used to accurately reproduce the T/R output before the normal switched-capacitor (SC) processing), or extra clock phases are required with the potential problems of direct signal feedthrough [2]. Thus, in this paper, a novel

low-voltage cross-coupled passive sampling circuit is proposed. With this circuit, a direct Sample-and-Hold-and-Reset (S/H/R) waveform can be produced in the foremost front-end stage (as shown in Fig. 1), making possible to imbed such sampling circuit into normal low-voltage SC building blocks (e.g. SC-S/H in pipelined ADC, or in the first stage SC-integrator in sigma-delta modulators). The proposed circuits can be equivalently applied to both reset- and switched-opamp circuits. As such, the need for a T/R stage is eliminated and thus one-stage opamp power can be saved. In section II, several existing sampling circuits will be firstly introduced to demonstrate their limitations, and based on this the cross-coupled passive sampling branch will be presented thus acting as a remedy to overcome those problems. Simulation results in transient and FFT analysis are later provided in section III to verify the performance of the proposed circuits, and finally the conclusion is drawn in section IV.

II. THE CROSS-COUPLED PASSIVE SAMPLING BRANCH

Several low-voltage input sampling interface using switched-opamp and reset-opamp circuits have already been published. One of such interfaces described in [10], and shown in Fig. 2, utilizes a resistor as voltage divider during the resetting phase, thus allowing the discharge of the sampling capacitor. This interface actually simulates the normal non-inverting, non-delay switched-capacitor branches that can only provide T/R output if the input is a continuous-time signal, thus this circuit cannot be imbedded into normal SC building blocks and an extra opamp must be used to perform the T/R function. Similar techniques are used in [7-9] where the input interface is actually an inverting resistive amplifier, again implementing only the T/R function. Extra T/R stages not only consume one extra-stage opamp power, but they will also influence and limit the linearity and speed, since the performance of such T/R is directly linked to the full resolution (or dynamic range) of the whole system. Another passive sampling interface exists in the context of switched-opamp circuits [2] that simulates the usual inverting, half-delay SC branches, then allowing truly S/H/R waveforms and thus can be imbedded into normal SC building blocks. However, extra clock phases are needed and most importantly, direct signal feedthrough from input to output can occur during the amplification phase. To suppress such signal feedthrough some limitations are placed on the size selection of various component values including switches and resistors [2].

Fig. 3 shows the proposed low voltage cross-coupled passive sampling circuits (in differential configuration) that can be used as a remedy for the issues previously discussed. When compared with the sampling circuit from Fig. 2, this circuit would be able to simulate the common inverting, half-delay SC branch. The resistor R has a similar function as the one in Fig. 1, providing resistive division with the on-resistance of switches S1 thus allowing the discharge

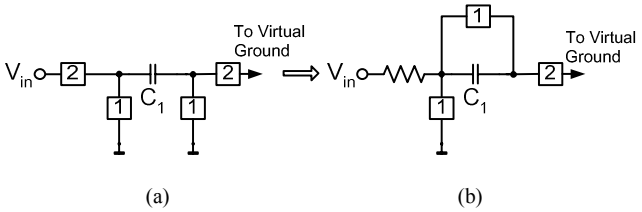

Fig. 2: Low-voltage passive sampling circuit proposed in [10]: (a) non-inverting, non-delay SC branches; (b) The low-voltage substitute of (a).

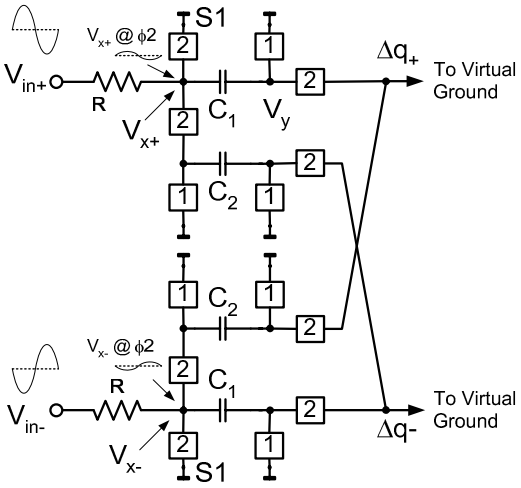

Fig. 3: The proposed low-voltage cross-coupled passive sampling circuits.

operation of the sampling capacitor C_1 in phase ϕ2. An extra pair of capacitors C_2 is added, each with the same size of C_1. The circuit operates as follows: In phase ϕ1, the differential signal will be sampled by the capacitor pair C_1, while the capacitor pair C_2 is reset. At phase ϕ2, the switches S1 are turned on and form the voltage divider with resistors R, thus the signal swing on nodes V_{x+},V_{x-} will be attenuated and all the switches connected to this nodes can now be turned on without any problem. In this phase the capacitor pair C_1 is discharged between the virtual ground of opamps and the attenuated signal, thus causing direct signal feedthrough interference in the charge transfer phase already analyzed previously. The capacitor pair C_2 is used to eliminate this problem, since C_2 is connected between the virtual ground and the attenuated signal in the opposite differential path. If $C_1 = C_2$, then the signal feedthrough will cancel each other and only the differential charge sampled in C_1 in phase ϕ1 is transferred to the virtual ground.

A simple quantitative analysis of the differential charge transfer during phase ϕ2 in the circuit from Fig. 3 yields:

$$\Delta q_+ - \Delta q_- = -C_1 V_{in}[\phi 1] - \frac{R_{on}}{R + R_{on}}(C_2 - C_1)V_{in}[\phi 2] \qquad (1)$$

where $\Delta q_+ - \Delta q_-$ represents the amount of differential charge transferred to the virtual ground at the end of ϕ2, R_{on} the on resistance of the switches S1, $V_{in} = V_{in+} - V_{in-}$ is the

differential input signal, and $V_{in}[\phi 1]$ the input signal at the end of ϕ1. From (1) it can be observed that the differential signal feedthrough will appear during ϕ2, but it will be cancelled if C_1=C_2 through a cross-coupling action of the passive sampling branch.

The on resistance R_{on} of switches S1 depends on the gate-source voltage and thus on V_{x+} and V_{x-}, modulating the voltage on those nodes by voltage division and thus causing harmonics distortion in phase ϕ2. However, the proposed circuit is insensitive to such distortion as the produced even harmonics will be cancelled by fully-differential operation, while those odd harmonics are similar to the attenuated signal feedthrough and thus cancelled by the action of the cross-coupled sampling branch. In additions, the proposed circuit has the advantages that only simple two-phase clock is needed, and also the signal feedthrough will be cancelled provided that C_1 matches C_2 and suitable size of switches S1 are chosen such that S1 can be turned on. This greatly relaxes the limitations of component values selection as discussed before [2]. Also, since the input signal is sampled in phase ϕ1 while charge transfer is performed in phase ϕ2, the sampling circuit simulates the normal inverting, half-delay SC branches which can provide S/H/R output with reset- or switched-opamp since the input continuous-time signal is decoupled in the charge transfer phase. This means that the circuit can be imbedded in normal SC building blocks such as S/H and integrators, eliminating the need of additional T/R stages and thus reducing power consumption. Although extra passive components (capacitors C_2) are added, the proposed circuit still consumes lesser area and power compared to previous designs since the added passive component is used to trade with the whole extra T/R stages that also contain more of passive components and one extra opamp as well. A drawback of the proposed circuit is its reduced feedback factor, and thus the speed, when compared with previous designs, since one additional pair of capacitors is connected to the opamp virtual ground.

III. Simulation Results

In order to verify the effectiveness of the passive sampling circuit, simulation results using Spectre simulator with 1-V supply voltage and real switches (0.35 μm CMOS process with V_{thn} = 0.56V and V_{thp} = -0.73V) were obtained with the SC S/H circuit shown in Fig. 4. The S/H circuit can be used as the front-end stage of a reset-opamp pipelined ADC, employing the cross-coupled sampling circuit to sample the input signal. Two single-ended opamp working in pseudo-differential mode are also used as in traditional designs of reset-opamp circuits [6], and a single-pole opamp model with finite gain-bandwidth product is used in the simulation. The value of R is chosen as 1.5kΩ. An input signal with frequency of f_{in} = 2 MHz and $1V_{pp}$ differential swing is applied to the S/H circuit (sampling rate f_s = 20 MHz). Fig. 5 shows the transient simulation results. As shown in the figure, the differential signal V_{x+} - V_{x-} shows full input signal swing in phase ϕ1 and being attenuated by voltage divider in phase ϕ2. It is clearly evident from the transient waveforms that, although an attenuated version of tracking signal is presented at nodes V_{x+} and V_{x-} in ϕ2, the passive sampling circuit can still provide the proper sampling function with direct S/H/R output in the reset-opamp S/H circuit.

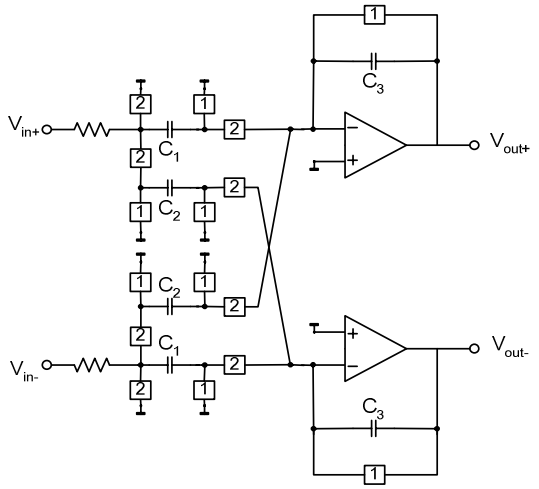

Fig. 4: Reset-opamp S/H circuit with cross-coupled input sampling branch.

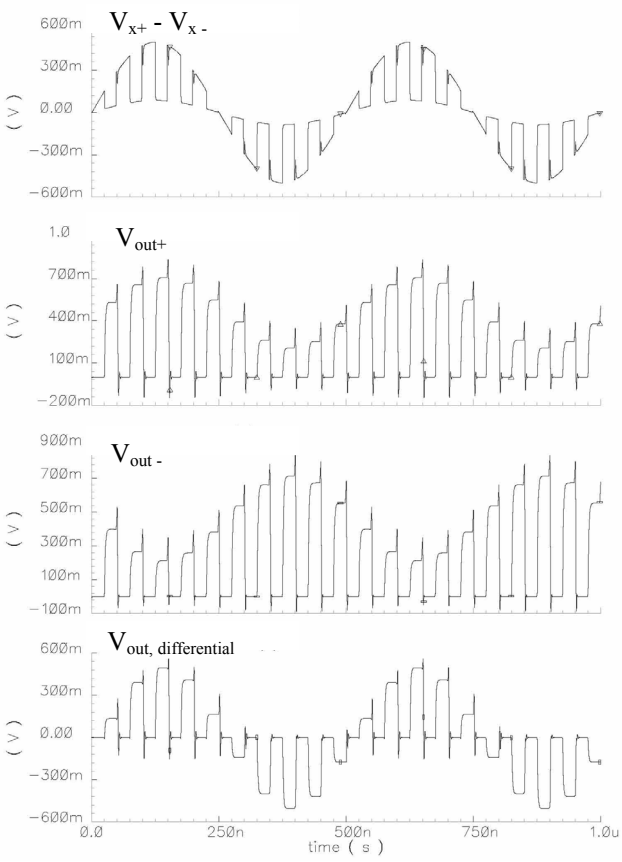

Fig. 5: Simulated transient waveforms of the S/H circuit in Fig. 4.

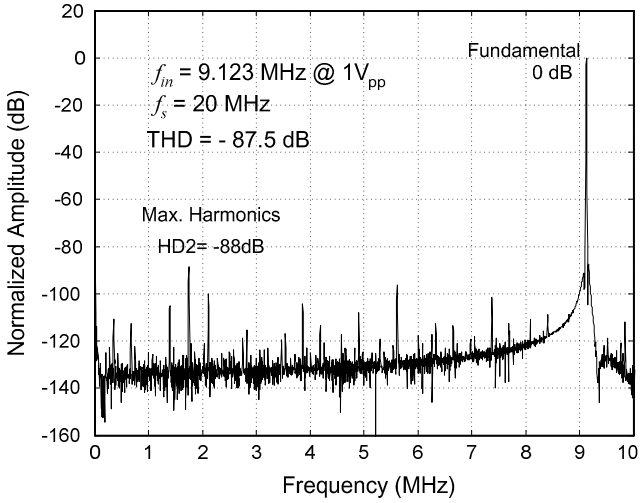

Fig. 6: Output spectrum of the S/H circuit.

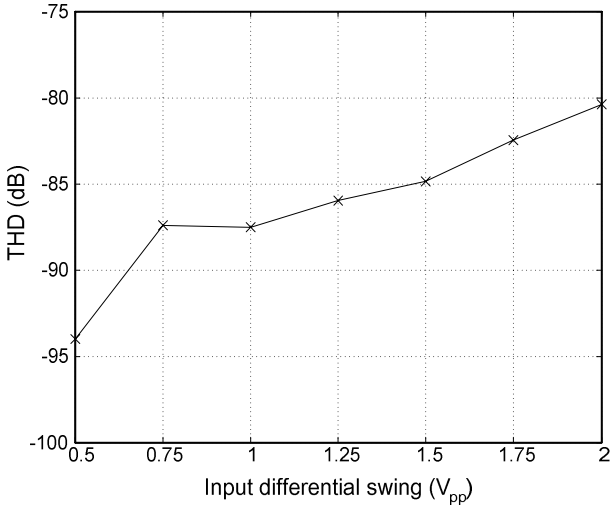

Fig. 7: Simulated THD vs input differential swing for the S/H circuit.

Besides the transient simulation, a FFT analysis has also been performed on the output differential voltage to evaluate the Total Harmonic Distortion (THD). An input signal with near-Nyquist rate (f_o = 9.123 MHz, f_s = 20 MHz, 1-V_{pp} differential swing) was used in this simulation, and 1% mismatches are introduced between C_1 and C_2, and also between the switch pair S1. Fig. 6 shows the FFT spectrum and a THD as low as –87.5 dB is achieved. Fig. 7 also shows a plot of THD as a function of input differential swing. The figure shows an -80.4dB THD even under the large differential signal swing, revealing the high-linearity of the cross-coupled passive sampling circuit.

IV. Conclusion

A novel cross-coupled low-voltage passive input sampling circuit has been proposed which can be applied for the direct input sampling interface, as required in reset- and switched-opamp circuits, eliminating the need of extra T/R stages as those used in traditional designs and thus saving one-stage opamp power. Requiring no extra clock phases, the circuit is insensitive to signal feedthrough, as well as to harmonics distortion produced by the switches, due to the action of the cross-coupling branch. Simulation results with 1-V supply voltage and real switches show a -87.5 dB THD @ 1V_{pp} input differential signal swing in a reset-opamp S/H circuit, and a -80.4 dB THD even at 2V_{pp} input, thus showing the effectiveness of the proposed circuit technique.

Acknowledgment

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