A 1-V 5.12-MHz Sampling-Rate 13-Bit CMOS ΔΣ Modulator Using Reset-Opamp Technique for Portable Audio Data Acquisition System

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Abstract—A 1-V ΔΣ modulator with 1-bit internal quantizer operating at 128x OSR based on reset-opamp technique is presented. The opamps do not need to be turned off during the reset phase of the operation and thus can achieve a high sampling rate. In this paper, challenging solutions for low-voltage design are described. Several low-voltage circuit techniques will also be discussed and among those the reset-opamp technique with pseudodifferential opamps is used in the ΔΣ modulator. The number of level shifter branches is reduced and the input voltage range of the quantizer covers completely the output voltage range of the opamp by using a current-mode comparator. The circuit has been implemented in a 0.35-μm CMOS process with a clock rate of 5.12-MHz, achieving 72.6-dB (SNDR) for a 20-kHz signal bandwidth. The chip area is 1.57-mm^2 with a power consumption of 9.39-mW.

Keywords—Analog-to-digital converter (ADC), charge-pump circuits, delta-sigma (ΔΣ), low-voltage (LV), sigma-delta modulator (SDM), switched-capacitor (SC), switched-opamp (SO), reset-opamp (RO).

I. INTRODUCTION

The current demand for mobile phones and audio devices is growing rapidly, and applications like the MP3 player, the VCD/DVD karaoke system, etc., usually imply System On Chip (SoC) designs in order to reduce size and weight. Also, the battery dimensions contribute to an important portion of portable device's size and weight. Low-voltage (LV) supply is a straightforward way to accomplish low power consumption and also for digital circuits to reduce the battery size and increase its life [1], as well as it is mandatory due to the technology down-scaling [1]. It is the continuing trend toward downscaling of the transistor dimensions one of the reasons why the future deep submicrometer MOST devices will not be able to withstand the multiplied voltage. From [2], ITRS (International Technology

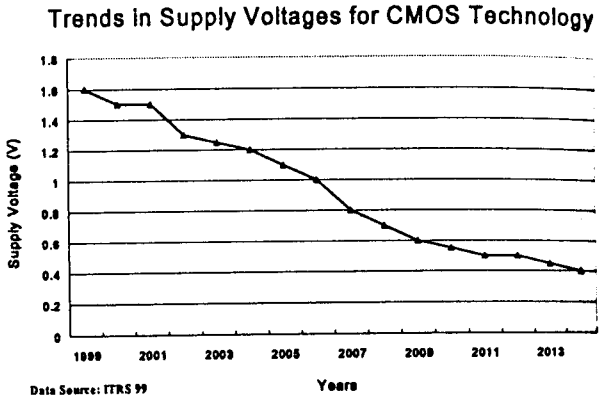

Fig. 1: Trends in supply voltage.

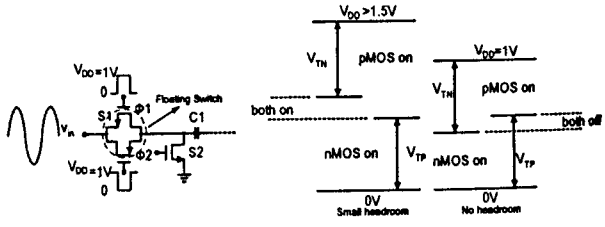

Fig. 2: Fundamental problem of CMOS switch.

Roadmap for Semiconductors) predicted that the maximum supply voltage will drop to 1.5-V in 2001 and 0.4-V in 2014 with the tendency shown in Fig. 1.

On the other hand, the most design-challenging building blocks of low-voltage ΔΣ modulator are the operational amplifiers and the switches and in many cases they are considered as the design bottlenecks. It is a great challenge to make those analog components operate under such low supply voltage because the LV supply may make it difficult to turn on those floating switches which operate at signal voltage levels [3]. This implies a difficult implementation of the commonly used SC circuits. To overcome these problems, several SC circuits and techniques can be adopted, such as the switched-opamp (SO) [4] and the reset-opamp (RO) technique [3]. The SO technique requires turning on and off the opamps in

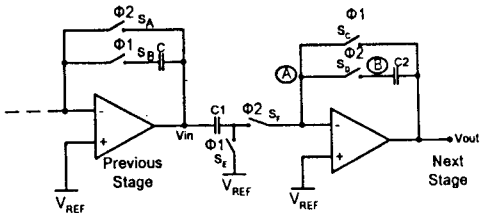

Fig. 3: SC circuit based on reset-opamp technique.

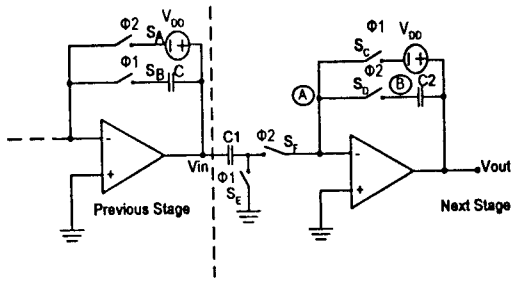

Fig. 4: Integrator realization using a floating voltage supply.

alternated clock phases, but the disabling of the amplifiers slows down the operation. The modulator presented in this paper uses the RO technique in the modulator function since it enables faster operation. Moreover, different from the previous designs [3], level shifters are reduced by using current-mode comparator, resulting in reduced power consumption. The operational amplifier of the first stage in a ΔΣ ADC is the most power consuming block, since it should drive the largest capacitive load with the least settling error. This paper describes a LV pseudodifferential opamp which is used in a 1-V ΔΣ modulator with 1-bit internal quantizer operating at 128x OSR.

In Section II, available techniques for the design of LV SC circuits will be discussed. The RO technique that is used to accomplish the ΔΣ modulator function is discussed in Section III. Finally, in Section IV, the design and performance simulations of a 1-bit LV ΔΣ modulator implementation are presented, followed by the conclusion in Section V.

II. Challenges In Low-Voltage SC Circuits

One of the main problems in a very LV SC circuits are the switches. With the reduction of the supply voltage, the MOS switches overdrive voltage is reduced, inhibiting proper operation of classical transmission gate in signal paths. As seen in Fig. 2, the nMOS transistor conducts for an input signal from 0-V up to $V_{DD} - V_{TN}$, and the pMOS transistor conducts from $|V_{TP}|$ to V_{DD}. When the supply voltage is less than $|V_{TP}| + V_{TN}$, none of the switches will be turned on for some signal values [4]. In Fig. 2, it is evidence that the switch S1 acts as a floating switch and cannot operate properly in LV environment.

There are several techniques that solve the problem described above. These include the use of low-threshold devices [5], voltage bootstrap circuits [6] and switched-opamp circuits [4]. However, they suffered from the problem of the expensive costs, oxide reliability issue for on-chip high voltage and also the speed limitation.

In this paper, reset-opamp technique is presented, which eliminates the use of floating switches by setting an opamp output voltage to a fixed value in one clock phase. In Fig. 3, the principle of this technique is illustrated. Since the opamps in this structure are always in high-gain operation, it is not necessary to powerup/powerdown of opamps, and thus can be operated with a higher clock rate. However, in the straight forward implementation of this stage would introduce practical problem due to forward biasing some p-n junction in the S_B switch [3]. In the next section, the operation of the circuits and the solutions to the forward biasing problem will be discussed.

III. Low-Voltage Reset-Opamp Integrators

In Fig. 3, C_1 is the sampling capacitor and C_2 is the integrating capacitor. In phase 1, C_1 acquires a charge equal to $C_1(V_{in} - V_A)$. However, the second stage of the opamp is reset to V_A. During phase 2, the output of the previous stage is reset to V_A, hence, C_1 discharges into the virtual ground of the opamp at the second stage. Also, the integrating capacitor C_2 is reconnected into the feedback branch during this phase (Φ2 = 1) and absorbs the charge of C_1. The input-output relation of the stage containing C_1 and C_2 is therefore a non-inverting integrator with a half-clock-period delay [3].

As discussed in the previous section, in Fig. 3, it is needed to set the reference level V_{REF} equal to 0-V, which permits a supply voltage as low as 1-V. This, however, introduces two problems. First, the switch on the right side of the integration capacitor C_2 is an nMOS transistor, whose junction diode easily becomes forward biased when the signal voltage on the capacitor pushes the node between the switch and the capacitor down in the reset

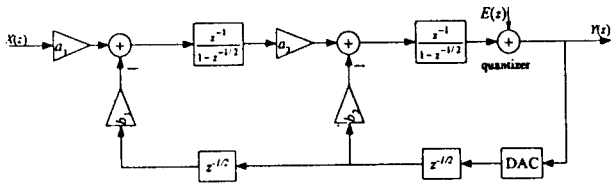

Fig. 5: 2nd-order low-pass sigma-delta modulator block diagram.

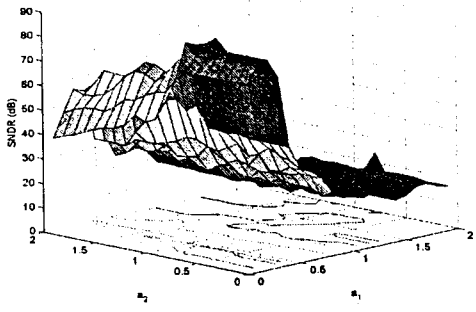

Fig. 6: Simulation to determine the optimal coefficients of a 1-bit second-order LPSDM.

phase [3]. Second, the driving the opamp output all the way down to virtual ground in the reset phase pushes its output stage transistors out of the saturation, resulting in a recovery time which is not much better than in a well-designed switchable opamp.

The technique used in this paper for solving the junction leakage problem is shown in Fig. 4. The circuit is added a floating voltage source in the unity gain feedback loop so as to prevent the charge leakage without increasing the supply voltage. Now the output is reset to V_{DD} instead of V_{SS}, which pulls the node B behind the integration capacitors up when entering the reset phase and thus no leakage can occur. However, the opamp output is still driven out of saturation, which can be avoided by making the voltage source somewhat smaller than V_{DD}, for example 0.8-V is used in this paper. The voltage source can easily be realized with a SC implementation.

IV. The Design Of Low-Voltage ΔΣ Modulator

In this section, a 1-bit 1-V 2nd-order ΔΣ ADC by using floating-supply integrator is implemented. The modulator block diagram is shown in Fig. 5. Normally, full clock period delay is used in ΔΣ modulator integrators. However, RO technique can only be implemented

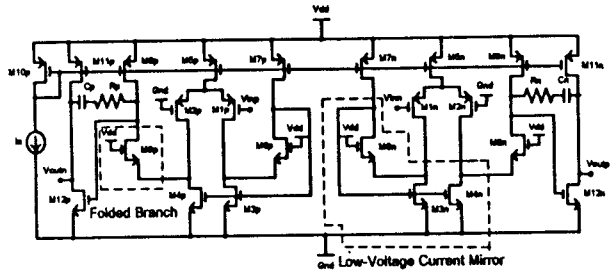

Fig. 7: Low-voltage pseudodifferential opamp.

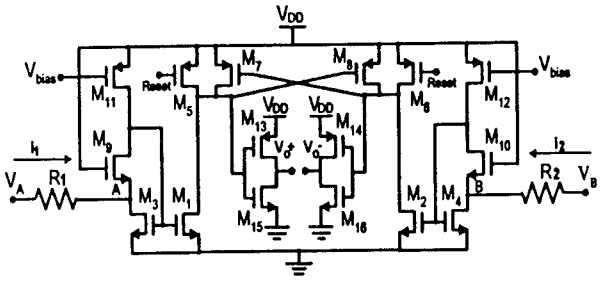

Fig. 8: Low-voltage current-mode comparator.

Table. 1: Performance result of the low-voltage opamp.

A_{dc}	f_u	PM	Tsettling	Slew Rate
67.8 dB	166.6 MHz	51.5°	21.38 ns	51.02 V/μs

half-delay integrators; an additional half-period delay is needed in each feedback loops [1]. The half-delays are implemented by flip-flops, which delay and hold the signal to correct phase for feedback. The flip-flops also act as buffer to drive the capacitive feedback load. Fig. 6 shows the behavioral simulation of the single-bit quantizer, in which $b_1 = b_2 = 1$, $F_1(z) = F_2(z) = 1$. It can be readily verified that, the coefficient a_2 has less effect on the performance compared to a_1, while a_1 should be kept smaller than 0.5 to avoid integrator saturation. Therefore the optimal coefficients for the single-bit LPSDM are $a_1 = b_1 = 0.25$, $a_2 = b_2 = 0.5$.

In LV operation, traditional folded-cascode OTA and telescopic OTA cannot be used, and it is also hard to implement the internal CMFB circuit in LV supply to enable the use of fully differential opamps [7]. Fig. 7 shows the LV pseudodifferential opamp structure [8], which enables the efficient implementation of only external CMFB circuit [3]. In this LV opamp, two LV techniques are utilized; one is the LV current-mirror in the input stage [9], and another one is the folded branch which is used to make sure the output stage transistors always operate in their linear region. The key performance

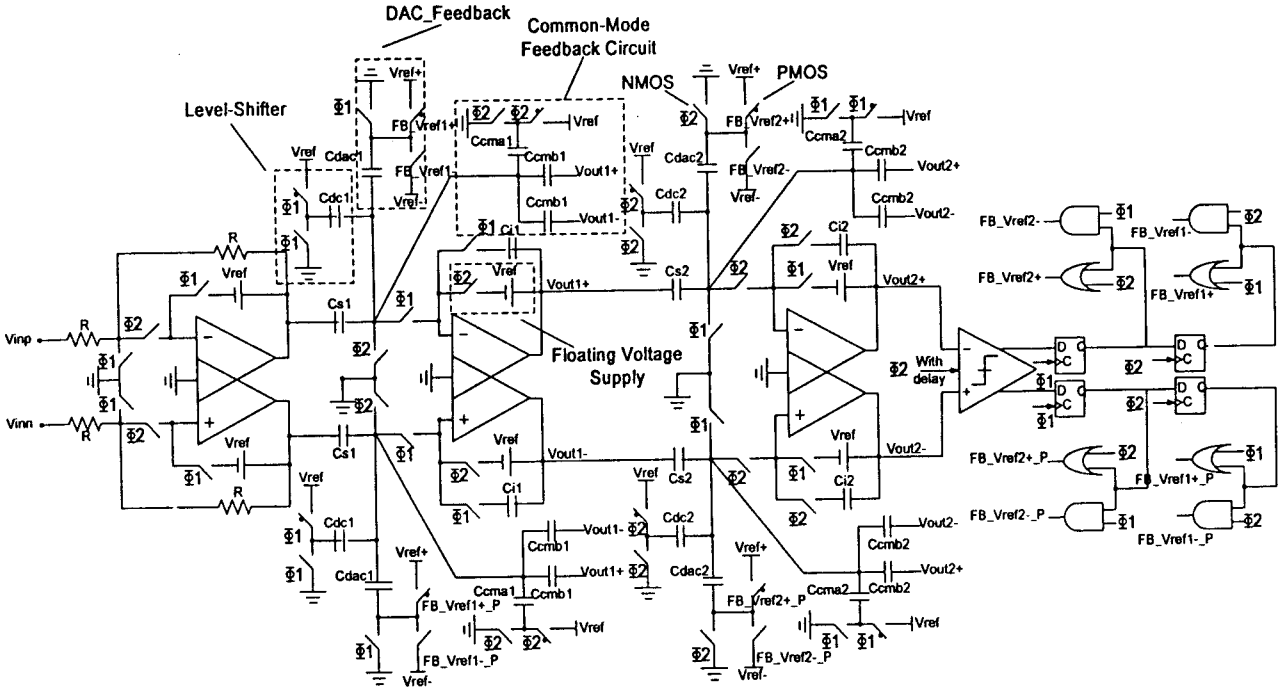

Fig. 9: Low-voltage second-order ΔΣ modulator.

Table. 2: The element values in Fig. 9.

R	30 kΩ	C_{s1}	2 pF	C_{s2}	0.5 pF
V_{ref}	0.8 V	C_{i1}	8 pF	C_{i2}	1 pF
V_{ref+}	0.75 V	C_{dc1}	0.75 pF	C_{dc2}	0.2 pF
V_{ref-}	0.25 V	C_{dac1}	2 pF	C_{dac2}	0.5 pF
NMOS switch	20 μ/0.3 μ	C_{cma1}	2.25 pF	C_{cma2}	1.875 pF
PMOS switch	70 μ/0.3 μ	C_{cmb1}	3 pF	C_{cmb2}	2.5 pF

results of the LV opamp with a maximum capacitive load of 7-pF are summarized in Table. 1.

Fig. 8 shows the LV current-mode comparator structure. Different from the previous designs [3], [10]-[13], current-mode comparator is preferred since the branches of level shifters are reduced and the input voltage range of the quantizer covers completely the output voltage range of an opamp. Therefore, circuit complexity and power consumption are reduced. However, when the voltage-mode comparator is used, level shifters are necessary. Since the output voltage of the opamp is normally halfway between V_{DD} and *GND*, and the input voltage range of the comparator is also close to either of the supply rails, the output range of the opamp and the input range of the comparator have a very small overlap. This makes the direct connection between the opamp and the comparator almost impractical [1], [14]. To overcome this problem, the output voltage of the opamp should be shifted to the lower voltages. However, this DC shifting is not easy to implement and consumes extra power. Therefore, in order to design a low-voltage comparator with wide input swing, a current-mode approach is employed. In Fig. 8 nodes A and B have very low input impedance and can be determined as $1/g_{m3}g_{m9}r_{ds11}$. The quiescent voltage V_Q for both nodes is approximately equal to $V_{DD} - V_{gs2}$. Therefore, the currents pass through R_1 and R_2 flowing to nodes A and B are equal to $(V_A - V_Q)/R_1$ and $(V_B - V_Q)/R_2$, respectively. By using current mode comparator, it is not limited by the input common-mode range. Therefore, the two outputs are shorted to the *GND* in order to put the comparator at the metastable point. Transistors M_5 and M_6 are used for this

purpose. When the V_{reset} gets high (latching phase), the voltages at the two outputs start rising. During this time, i_1 and i_2 are also compared, and a digital signal is generated at the output nodes. Since the comparator inputs are connected to resistors, high input signal swings can be obtained. The minimum supply voltage is given by max $\{V_{in9} + V_{eff9} + V_{eff3}, V_{eff11} + V_{eff9} + V_{eff3}\}$ [15], which is usually lower than 1-V. After the output voltage reach a certain value the cross-coupled transistors M_7 and M_8 form a positive feedback and depending upon the initial currents of M_1 and M_2, one of the outputs goes to V_{DD} and the other one goes to *GND*. When the two outputs reach their final values, they stay there until the V_{reset} signal goes low again. In this circuit, M_1, M_3, M_9 and M_2, M_4, M_{10} are performed as a LV current mirror structure. As the two transistors having the same gate-source voltage, their currents will be proportional to their sizes. Therefore, the currents pass through M_1 and M_2 transistors are amplified as their sizes are four times larger than that of M_3 and M_4. As a result, the comparator response is faster. For the transistors of M_9 and M_{10}, they are used to keep the transistors of M_3, M_4 and M_{11}, M_{12} in their saturation region for all of the conditions. The transistors of M_{13}, M_{15} and M_{14}, M_{16} perform as an inverter. Since the voltage at the output is never equal to full V_{DD} or *GND*, an inverter is used to overcome this problem.

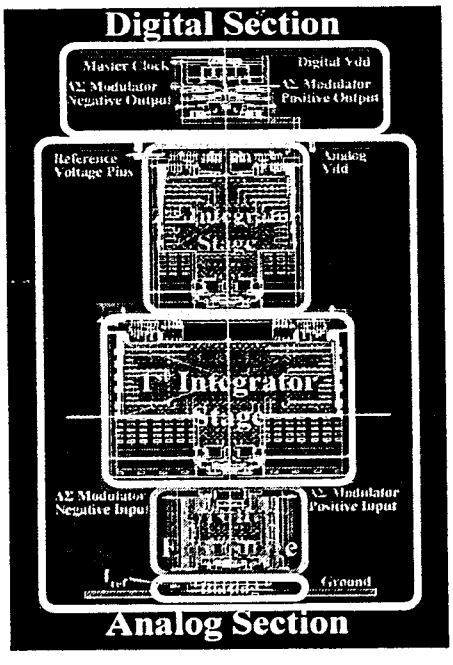

Fig. 10: Layout of overall stage in the proposed modulator.

The integrator implemented by reset-opamp in pseudodifferential way should come along with other common mode correction circuits, such as level shifters and external CMFB circuits [16]. They adjust the desired input and output common model level and remove unwanted DC offset which is caused by the inaccurate cancellation of the input dc offset and the uncancelled charge injection from the switches. The LV DAC feedback branches are included in Fig. 9. They are different from the previous designs [3]; they are connected with a negative feedback structure. All switches operate at V_{ref+} = 0.75-V or V_{ref-} = 0.25-V. The common-mode level of the DAC signal is corrected by the level shifter circuits at the opamp inputs. Finally, the whole 2nd-order single-bit SDM circuit structure is shown in Fig. 9 which includes the LV input sampling circuits, dc shift compensation circuits, external CMFB and LV DAC feedback branches, etc. The summary of element values for the overall circuit is shown in Table. 2.

Fig. 10 shows the overall layout of the proposed modulator, it is realized in a 0.35-μm double-poly triple metal CMOS technology. At the sensitive node, such as the input terminals of opamp and the clock lines, the shielding is provided to protective from the noise digital and substrate noise. Metal-2 acts as the shielding layer and is connected to the positive power supply V_{DD}. Each stage

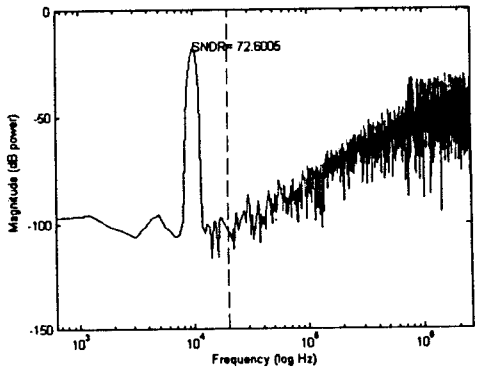

Fig. 11: The spectrum of the digital output bit stream.

Table. 3: Simulated performance of the second-order ΔΣ ADC.

Supply Voltage	1 V
Signal Bandwidth	20 kHz
Sampling Frequency	5.12 MHz
Max. Diff. Input	1 V_{PP}
ENOB	11.7 bits
Peak SNDR	72.60 dB
Power Consumption	9.39 mW

of the layout is fully symmetric, and the capacitors in the front-end stage are arranged in two-dimensional common centroid. The total chip area is 1.57-mm^2, while dissipating 9.39-mW.

The LPSDM was simulated with a 5.12-MHz clock signal and with 1-V supply voltage. In Table. 3, it gives a summary of the measured results. For audio-band (0-20-kHz) operation, ENOB of 11.7-bit accuracy is achieved. The simulation results are shown in Fig. 11.

V. Conclusion

In this paper, a 1-V single-bit sigma-delta modulator has been presented. This modulator is implemented as a 2^{nd}-order LP structure to accomplish the modulation of an audio band signal with 20-kHz bandwidth, and with 128x OSR. The problems of LV operation of SC circuits have been discussed, and solutions based on RO were presented. By using this structure, the SDM can be clocked at a higher rate. Normal SC circuits cannot be implemented in LV, but with the use of RO structure and pseudodifferential opamp, the problem of floating switches is solved. For the same reason, the on-resistance of all switches is not related to the signal level, and so it is not necessary to use delayed clock phases as in conventional SC circuits. The overall layout of the modulator is presented and the simulation results of the $\Delta\Sigma$ modulator show that the circuits operate with satisfactory results at 1-V supply voltage.

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