AUTOMATIC SYNTHESIS OF IIR SC MULTISTAGE DECIMATORS

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Abstract- **This paper presents an automated system for the design of IIR SC multistage decimators. Through the integration of different existing programs it provides a user-friendly interface that allows the implementation of IIR SC decimators from the top filter specifications down to the circuit layout. It allows the automated design of a cascade of decimator stages in order to obtain a sufficiently high ratio between the sampling frequency and the maximum signal frequency of interest, and also simplifies the circuit through the minimization of the silicon area. Two design examples are given to demonstrate the feasibility of this approach.**

I. INTRODUCTION

While computer-assisted tools for the design of digital circuits with multirate techniques have already attained a considerable degree of maturity [1], there are fewer tools for the engineers working on the analog portion of the chips and namely in the design of sampled-data analog (SDA) decimators and interpolators [2-4]. Here, there is an important need to provide designers with computer-aided tools supporting SC multirate circuits design, that usually consists of a program for automatic synthesis of a SDA decimator or interpolator, which comprises the use of the available architectures and techniques that optimize the implementation of the overall circuit.

In this paper, we present a computer-aided tool designated as *ISCMRATE* [5] (Interactive Switched Capacitor Multirate Compiler) with three levels of synthesis that can be used in the automated design of multirate circuits from the filter specifications to the layout (Fig. 1). The compiler architecture also presents IIR multistage decimator design, which provides an improved solution that allows the implementation of mixed architectures comprising a library of topologies including different multi-decimation IIR SC building blocks (Externally Cascaded, Internally Cascaded [6] and Ladder building blocks [7]). For optimizing the performance of IIR SC decimating circuits while simultaneously minimizing silicon area also, a set of rules are also presented to select the most suitable steps based on a statistical approach.

In order to shorten the design period, and also provide the users with friendly interfacing, the basic architecture of the program comprehends the system level and the building block level linked to a few existing programs. The compiler starts with a set of original filter specifications, in terms of the frequency response, and a given decimating factor. A prototype filter z-transfer function, meeting a particular specification, is interactively generated by a filter synthesis tool QED [8], that is optimized by an automated-algorithm [9] using Linear/Non-linear programming with MATLAB [10].

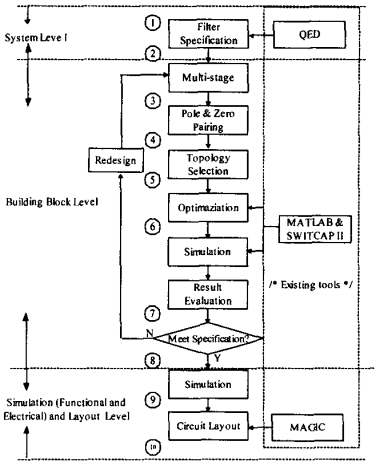

Figure 1: General architecture of the *ISCMRATE* compiler for IIR SC multirate circuits design.

This synthesis is followed by a multirate transformation and the selection of the topology for signal processing and data conversion. After capturing the set of constraints and using linear/nonlinear-programming methods, the resulting functional specifications are automatically determined in order to meet the frequency response requirements and the minimum value of the total capacitor area. This process will be followed by an external mixed-mode simulation with SWITCAP [11] that will verify the frequency response of the circuit first, and later, after maximization of the dynamic range, will generate a file of component values for future layout synthesis.

Finally, the layout synthesis of the SC decimator will be generated based on the text mode output file for MAGIC [12]. The automated layout generation of the circuit (under development) will allow the selection of the different electronic components (OA's, switches and capacitors) from a library of pre-designed standard cells. For the practical feasibility and compatibility of the compiler, the building blocks in each stage will be therefore determined and implemented independently.

II. MULTISTAGE IMPLEMENTATION OF IIR SC DECIMATORS

The concept of using a series of stages to implement a sampling rate conversion was given for digital systems in the early seventies, in order to significantly reduce computation [1]. Similarly, multistage design also has been proved to be one of the most effective solution for IIR multirate SC analog circuits, not only to allow a sufficiently

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high ratio between the sampling frequency and maximum signal frequency of interest, but also to simplify large circuits, and making it possible to design a circuit with a small silicon area [6].

In IIR SC multirate circuits, the polyphase inputs are responsible for the implementation of the numerators polynomial function and their complexity is related not only to the specified filtering requirements such as the filter order D, but also to the decimation factor M.

The single-stage architecture of an IIR multirate SC decimator, as shown in Fig. 2, can only be applied for a limited decimation ratio. When the required decimation ratio becomes larger, a multistage implementation exhibits greater efficiency when compared with a single-stage only, as illustrated in Fig. 3 [1, 6].

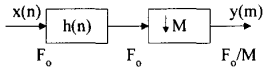

Figure 2: Single-stage implementation of IIR SC decimator.

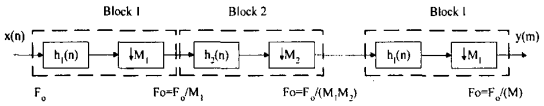

Figure 3: Multistage implementation of IIR SC decimator.

In a multistage implementation if $H(z)$ is the prototype filter z transfer function (even-order), it can be expressed as:

$$H(z) = k\prod_{i=1}^{D}\frac{(1-2r_{oi}\cos(\theta_{oi})z^{-1}+r_{oi}^2z^{-2})}{(1-2r_{pi}\cos(\theta_{pi})z^{-1}+r_{pi}^2z^{-2})} = k\prod_{i=1}^{D}h_i(z) \qquad (1)$$

Where k is a gain factor, D is the number of cascade biquadratic sections. The modified z-transfer function $\bar{H}(z)$ for multistage implementation with overall decimation factor (M) will then be:

$$\bar{H}(z) = k\prod_{i=1}^{D}\frac{(1-2r_{oi}\cos(\theta_{oi})z^{-T_i}+r_{oi}^2z^{-2T_i})}{(1-2r_{pi}\cos(\theta_{pi})z^{-T_i}+r_{pi}^2z^{-2T_i})} = k\prod_{i=1}^{D}h_i' \qquad (2)$$

Where i represents the sequence of the decimator stages from the input i =1 to the output i =D. If we designate the input sampling frequency of each SC decimator stage as F_i, then the normalized delay periods T_i appearing in the correponding z-transfer functions are determined by $T_i = M(F_s/F_i) = \prod_{j=1}^{i} M_j$, where, for the given overall decimation factor M of the multistage structure, M_j represents the factors of sampling rate reduction of the decimator stage j =1 to j =D. The decimation factor M will be the lowest common multiple of several smaller integer numbers that will be applied in the multistage structure as the decimation factors of the different cascaded blocks. The number of possible combination of circuit topologies would be quite large if the decimation factor M presents an high value.

III. Automated Design of Two Multistage Decimator Examples

The performance of the *ISCMRATE* compiler can be illustrated by means of two examples: a) a 3rd order lowpass filter with sampling frequency 500 MHz, passband ripple of 0.165 dB, cutoff frequency f_c =1 MHz, and minimum rejection of 100 dB above 5 MHz, b) a 6th order lowpass SC decimator, with reduction of the sampling frequency from 10 MHz at the input to 1MHz at the output with the maximum passband ripple of 0.25 dB, the cutoff frequency f_c =0.1 MHz, and minimum rejection of 75 dB above 0.5 MHz.

A. The nominal frequency response of the 3rd IIR SC decimator will be affected by the decimating factors (from M=4 to M=15), as illustrated in Fig. 4 (a) (b). Then, a possible circuit architecture, Externally Cascaded with FB damping and M=4, is shown in Fig. 5. To retain the specified gain at low sampling frequencies, to reduce the sensitivities and to simplify the implementation, the decimating factors should be as large as possible. A larger decimating factor in a stage can minimize the GBW values of the amplifiers required in a circuit [6], but it has the disadvantage of producing the unwanted aliasing-bands that will become even more significant as the decimating factors increase (like it is shown also in Fig. 4).

Using the above mentioned compiler - *ISCMRATE*, the comparison between different analog SC multistage and multirate circuits can be performed, and the best values of capacitance spread and total capacitor area achieved with different IIR SC decimators implementation (but for the same decimation factor M=4) is briefly summarized in Table I. From this table it can be observed that, in general, the total capacitance varies with the topologies and damping types selections. At least 70% reduction in total capacitance was observed for this approximation by using optimal combination of pole-zero-period.

B. In order to present the practical feasibility and compatibility of the program, the second example is therefore determined with a two-stage implementation with different building blocks as shown in Fig. 6.

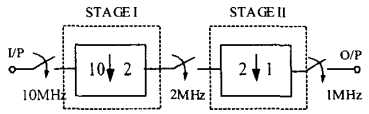

Figure 6: 6th -order multistage decimator combining externally (M_1=5) and internally cascaded (M_2=2) stages.

The selection of an optimum sequence topology, has determined an architecture with a 2nd-order externally cascaded building block with M_1=5, followed by 4th-order internally cascaded building block with M_2=2 as shown in Fig. 7.

After scaling for maximum signal handling capability and normalizing with respect to the unit capacitance values,

the decimator presents a maximum capacitance spread of 33 and a total area close to 220 capacitor units for the complete circuit.

IV. CONCLUSIONS

This paper proposes an interactive architecture compiler *ISCMRATE* applied to the design of multistage IIR SC decimators. The compiler presents three different levels, namely the system synthesis, the building block design and the simulation, followed finally by the layout. In the first level of synthesis, the multi-decimation cascaded and ladder blocks are independently determined in order to fulfill user's different requirements. The design method allows designers to quickly compute the exact capacitance ratios, implementing a pre-determined set of design specifications, which are obtained in the second level together with the verification of the circuit behavior by simulation. The design examples show the efficiency of multiple decimating structures in the elimination of unwanted aliasing frequency components arising on IIR SC multistage decimating filters and demonstrate the compiler feasibility and compatibility.

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TABLE I
COMPARISON BETWEEN THE ALTERATION METHODOLOGIES FOR 3RD ORDER SC LOWPASS DECIMATORS (M=4)

Types	Externally Cascaded					Internally Cascaded	Ladder
Damping	E			FB		FD	---
$M=M_1, M_2$	1, 4	2, 2	4, 1	4, 1	1, 4	4	4
Total-C	134.4	108.4	111.7	100.6	711.9	37.9	36.0
C-Spread	51.1	53.2	57.6	51.1	425.5	6.1	7.1

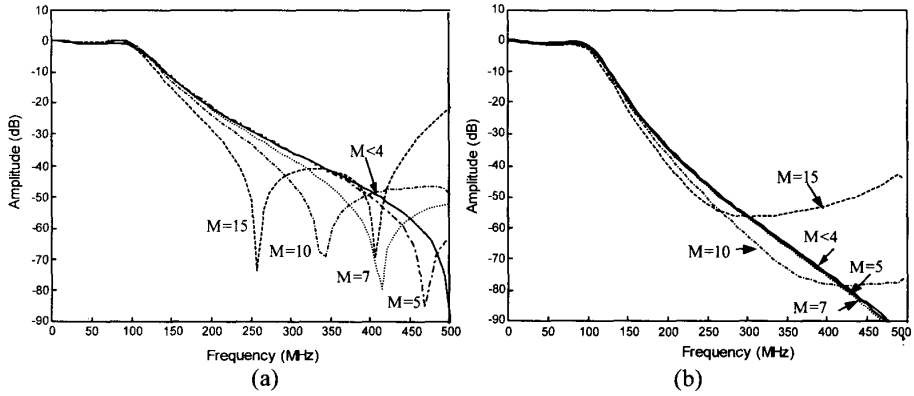

Figure 4: Computer simulated amplitude response (M=4, 5, 7, 10, and 15) (a) Externally (b) Internally and Ladder.

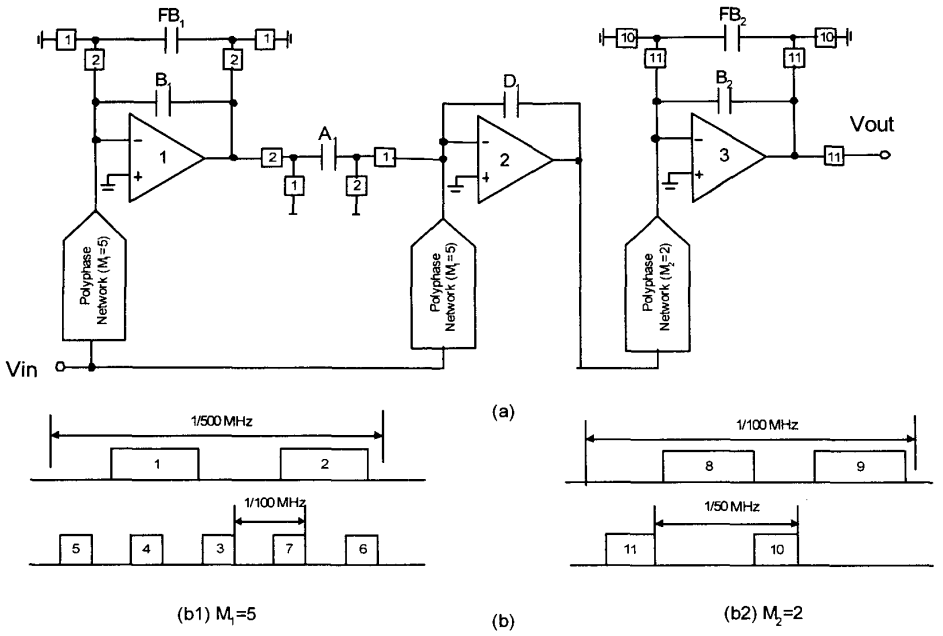

Figure 5: (a) 3rd -order IIR SC externally cascaded decimator, (b) Switching waveforms, b1) Stage 1, b2) Stage 2.

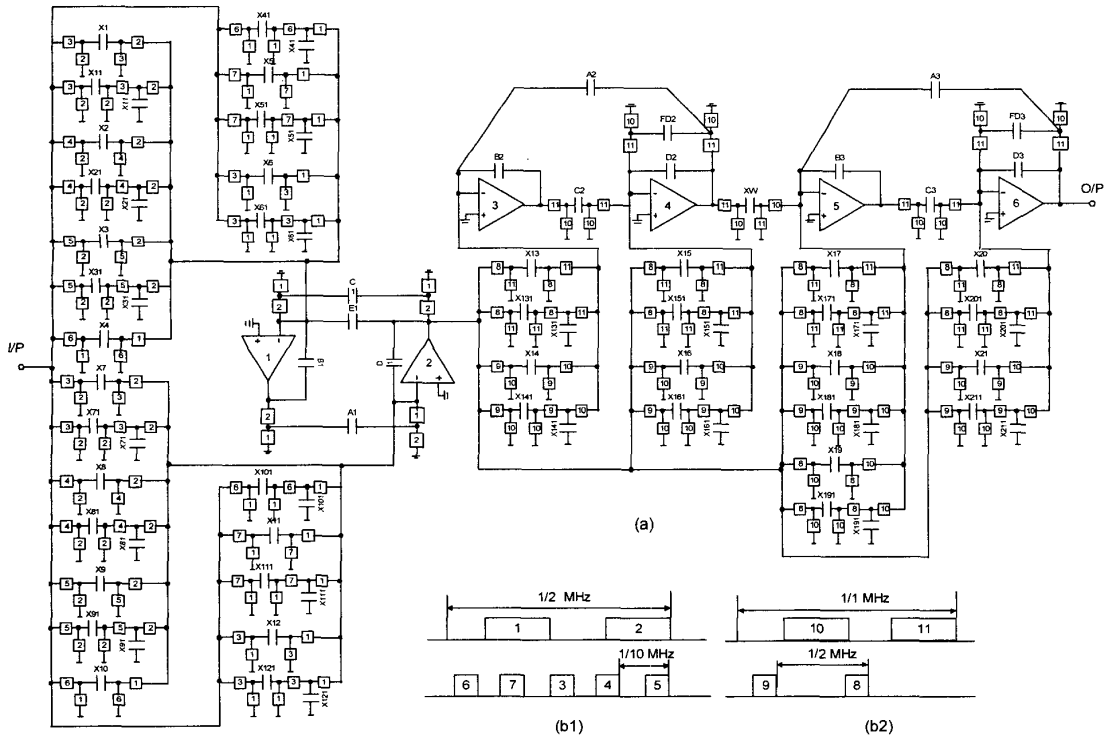

Figure 7: (a) 6th-order IIR SC multistage decimator, (b) Switching waveforms, b1) Externally, b2) Internally cascaded.