AN *I/Q*-MULTIPLEXED AND OTA-SHARED CMOS PIPELINED ADC WITH AN A-DQS S/H FRONT-END FOR TWO-STEP-CHANNEL-SELECT LOW-IF RECEIVER

Pui-In Mak, Kin-Kwan Ma, Weng-Ieng Mok, Chi-Sam Sou, Kit-Man Ho, Cheng-Man Ng,
Seng-Pan U [1] and *R.P. Martins* [2]

Analog and Mixed-Signal VLSI Laboratory, FST, University of Macau, Macao SAR, China (E-mail – p.i.mak@ieee.org)
1 – Also with Chipidea Microelectronics (Macao) Ltd., 2 – On leave from Instituto Superior Técnico (IST), Lisbon, Portugal

ABSTRACT

A novel pipelined ADC architecture that exhibits both power and area efficiencies is proposed to be accountable for the major baseband functions of the recently introduced two-step-channel-select (2-SCS) low-IF receiver. Such architecture comprises: 1) a sample-and-hold (S/H) front-end implementing Analog-Double Quadrature Sampling (A-DQS) for IF-to-baseband downconversion and IF channel selection, and 2) one OTA-shared pipelined ADC is employed for digitalization both *I* and *Q* channels through *I/Q*-multiplexing. An IC prototype was designed in a 0.35-μm CMOS process with 20-MS/s 8-bit resolution, which has been targeted for 2.4-GHz ISM band standards. The key simulated performances achieved 7.7-b ENOB with INL and DNL within ±0.5 LSB and ±0.34 LSB, respectively. A competitive chip area of only 1.34 mm^2 is achieved, while dissipating an average of 54.5 mW from 2.5 V.

1. INTRODUCTION

Power and area minimizations of wireless transceiver ICs are imperative to reduce both the battery size and manufacturing cost of portable devices. In designing receiver analog front-ends (AFEs) that satisfy modern communication standards requirements, low-IF topology is an alternative of the traditional heterodyne-based anatomies in terms of both integratability and power consumption. Recently, a two-step-channel-select (2-SCS) low-IF receiver [1] has been proposed. Such improved architecture, as shown in Fig. 1, can effectively reduce the PLL frequency synthesizer (PLL-FS) phase noise and settling time requirements through channel selection partitioning from the RF AFE to the IF one [1]. This paper presents an implementation of such receiver baseband circuitry, which includes a sample-and-hold (S/H) pair embedding Analog-Double Quadrature Sampling (A-DQS) [1]-[3], combined with an *I/Q*-multiplexing pipelined ADC. Thus, this circuitry not only performs the IF-to-baseband downconversion and second step of channel selection, but also single-ADC-*I/Q*-digitization in one chain. Obviously, this architecture can highly reduce both occupied area and power consumption of the receiver. Another vital advantage is the elimination of *I/Q* imbalance in the A/D conversion with the correspondent improvements in image-rejection. The targeted applications of this receiver are the 2.4-GHz standards including Bluetooth, IEEE 802.11FH and HomeRF, since the power consumption is a major concern, and demanding low phase noise and fast settling time requirements of the PLL-FS, which needs to perform frequency-hopping continuously.

2. ARCHITECTURE DESIGN AND SYSTEM MODELING

In low-IF receivers, selecting the IF with a value equals to half-channel bandwidth implies that the desired channel and its adjacent image will be downconverted together to the same IF. As a result, by using the forward and backward frequency shiftings characteristic of the A-DQS technique [1], the channel selection can be divided into 2 steps: the first step is still performed by the PLL-FS at RF, while the second one is implemented by the proposed digitally-controlled A-DQS S/H pair for the final selection between the two neighbor channels in the IF (i.e. the desired channel and its image). Thus, the front-end PLL-FS settling time and phase noise requirements are both relaxed since it is only necessary a dual-channel downconversion from RF. The detailed principles of such technique can be found in [1] and [3], and they are omitted here for the sake of brevity, whereas this paper concentrates on its circuit implementation and the new pipelined ADC architecture, as shown in Fig. 2. First, the A-DQS S/H pair will perform the sample-and-hold operation, IF-to-baseband frequency downconversion and IF channel selection through simple digital control. Then, the baseband *I/Q* signals will be time-interleavely sampled into the pipelined ADC core through an analog-multiplexer (MUX). The pipeline core utilizes six fully-differential 1.5-b resolution stages with OTA-shared between two consecutive stages. An offset cancellation technique, namely feedback signal polarity inverting (FSPI), is applied to reduce two-thirds of the offset voltage [4].

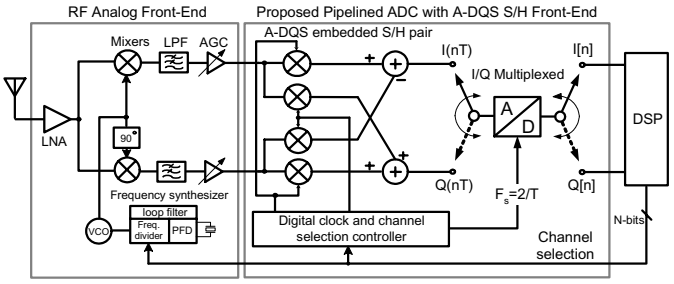


Fig. 1. Proposed pipelined ADC in 2-SCS low-IF receiver.

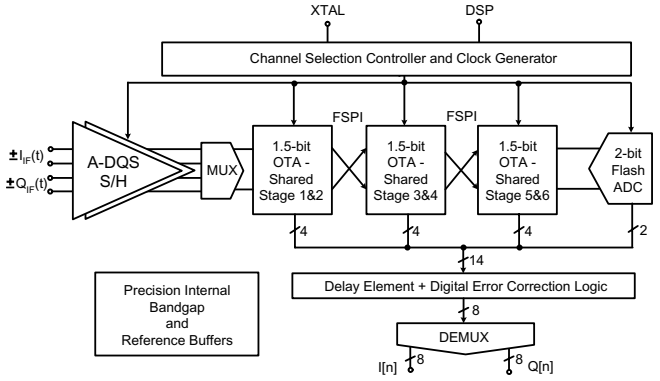
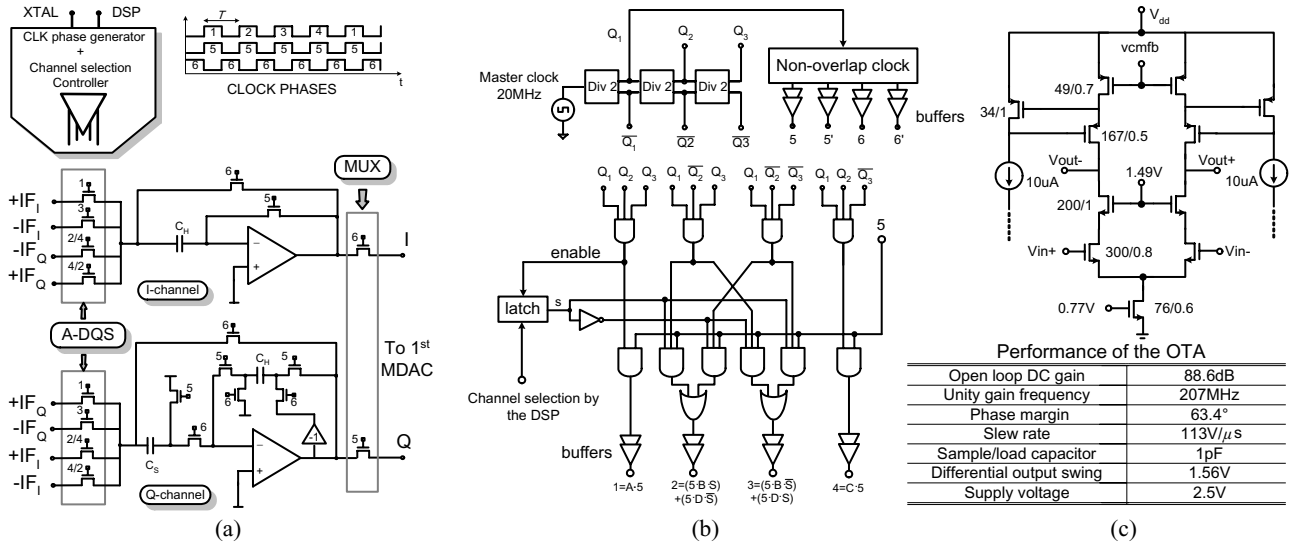


Fig. 2. Architecture of the proposed pipelined ADC.



Performance of the OTA

Open loop DC gain	88.6dB
Unity gain frequency	207MHz
Phase margin	63.4°
Slew rate	113V/μs
Sample/load capacitor	1pF
Differential output swing	1.56V
Supply voltage	2.5V

(a) (b) (c)

Fig. 3 Digital-control A-DQS S/H pair. (a) Single-ended schematic of the S/H pair with MUX. (b) Channel selection embedded clock phase generator. (c) OTA architecture and its typical performance.

Other functional blocks include a 2-b flash ADC, a digital error correction (DEC) logic with delay elements, a digital-demultiplexer (DEMUX), a clock phase generator, a pure-CMOS bandgap current reference and a multi-stage voltage reference driving buffer, to accomplish a final *I/Q*-synchronized 8-b code for both *I* and *Q* channels.

The entire system is first modeled in MATLAB™ with thorough considerations of circuit non-idealities, matching and noises. For instance the OTA non-idealities and capacitor mismatches as well as image-rejection due to *I/Q* mismatch and noises resulting from unstable voltage reference, etc. The final optimized design specifications are listed in Table 1.

3. CIRCUIT IMPLEMENTATIONS

3.1 Programmable A-DQS sample-and-hold pair

The single-ended version of the A-DQS embedded *I/Q* S/Hs and the OTA architecture, as well as its channel selection embedded clock phase generator are all shown in Fig. 3 (the actual implementation is fully-differential). The standalone implementation of this A-DQS S/H by utilizing two half-delay S/H circuits is reported in [3]. Differently in this work, the *I*-channel S/H is still a half-delay offset-insensitive S/H, whereas the *Q*-channel is a newly proposed with full-delay and polarity inversion in each phase-change to provide the offset-cancellation. This half-delay plus full-delay *I/Q* S/H architecture is specially designed for the following pipelined core to process the time-interleave *I/Q* data with only doubling of its operation frequency. It is noteworthy that the charge-transfer in the *Q* channel S/H will result in a large mismatch with the *I* channel one. However, such kind of mismatch only results unproblematic self-image problem [2]. The analog multiplexer can be simply implemented by four analog switches (differentially) controlled by two non-overlapping clock phases, thus, resulting in insignificant influence to the entire system performances. All the switches are implemented with transmission gates due to their front-end position and to minimize the distortion due to input-dependent charge-injection and on-resistance variation. The implemented OTAs are gain-boosted telescopic [Fig. 3(c)] with switched capacitor (SC) common-mode feedback (CMFB). The channel-select controller is implemented with the clock phase generator in the control path by using simple digital circuitry, in order to alter the A-DQS sampling sequences for channel selection [1], thus there is no transient effect in the sampled-data signal paths. As described above, the add-on circuitry for the frequency downconversion and channel selection comprises only a digital controller and several analog switches in the S/H circuits.

Table 1. Design specifications of the proposed pipelined ADC.

Resolution		8 bits
Conversion rate and clock frequency		20 MHz
Input signal swing (2.5 V power supply)		1 $V_{pk\text{-}to\text{-}pk}$
Reference voltage (differential)		0.5 V
Sampling / feedback capacitor value		0.5 pF
Clock duty cycle		0.4 - 0.6
Clock rise/fall time		< 1 ns
Image-rejection ratio (IRR)		> 40 dB
Circuit Non-idealities		
OTA	DC gain	> 80 dB
	Slew rate	> 100 V/μs
	Unity gain frequency	> 180 MHz
	Offset voltage	< 5 mV
	Noise power	< -70 dB
	Input parasitic capacitance	< 0.3 pF
Mismatch in sample & feedback caps.		< 0.5%
Capacitor top / bottom plates parasitic		< 10% / 30%
Voltage reference noise		< -40 dB
1.5-bit flash comparator offset voltage		< 31.25 mV
2-bit flash comparator offset voltage		< 5 mV

3.2 MDACs and comparators

The schematic of two consecutive OTA-shared MDACs with FSPI technique is shown in Fig. 4. Although the FSPI technique can reduce two-third of the offset voltage [4] in the OTA sharing circuit, the extra switches adopted in the signal paths will enlarge the settling time. A design trade-off is still needed, especially for high-speed and high-resolution applications. However, in the proposed low-speed pipelined ADC, such technique is well appropriate to minimize the chip area and power consumption. The OTA architecture in the S/H is also utilized for the MDACs. Since digital error correction logic is employed in the digital back-end to relax the specifications of the comparators in the sub-

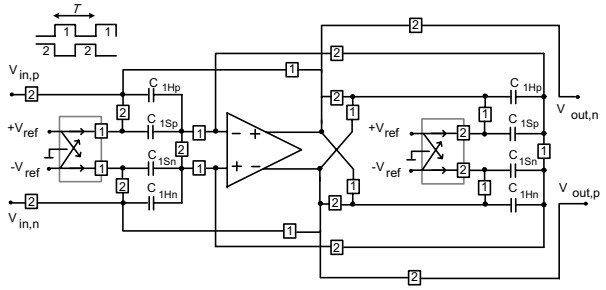


Fig. 4. Two consecutive OTA-shared MDACs with FSPI.

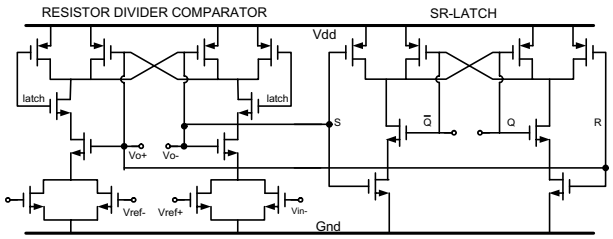


Fig. 5. Comparators with SR-latch.

and flash-ADCs, they are therefore designed in simple resistor divider comparators with SR-latch, as shown in Fig. 5.

3.3 Digital back-end architecture

The digital back-end architecture is shown in Fig. 6. The thermometer codes produced from the comparators are first re-coded into binary codes through simple logic circuitry, and they will pass to the delay elements implemented by D-type flip-flops for codes synchronization. The 14-bit output codes are then corrected to the final valid 8-bit codes through digital error correction logic. Since the *I* and *Q* data must be synchronized and held in the final output during de-multiplexing, three sets of delay elements implemented also by D-type flip-flops with simple switches control are used to delay the first-outputted *I*-channel data one more cycle than the *Q*-channel.

A careful logic design and layout for equal-propagation delay is applied in each clock phase design according to the specified requirements. Edge trigger buffers for last-stage rising-edge synchronization are adopted for driving the clocks to control the random process mismatches and minimize the time-skew and clock-jitter effects [5].

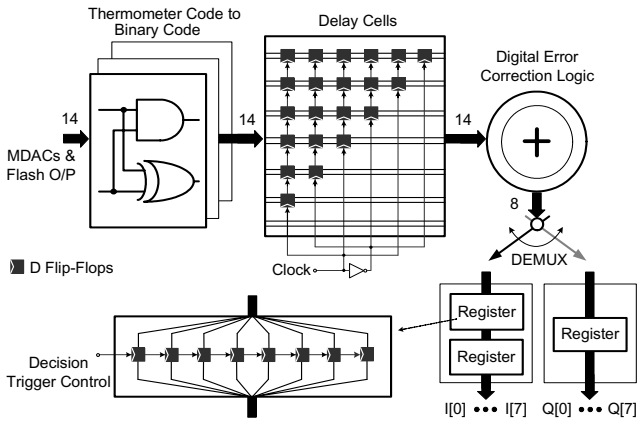


Fig. 6. Digital back-end architecture.

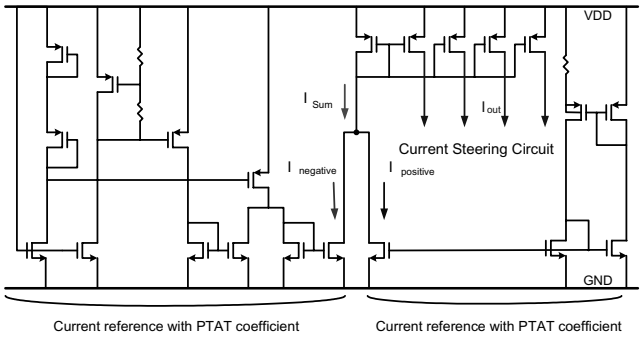


Fig. 7. Pure-CMOS bandgap current reference.

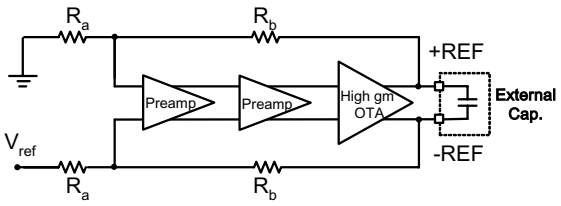


Fig. 8. Multi-stage voltage reference driving buffer.

3.4 Pure-CMOS bandgap current reference and voltage reference driving buffer

The pure-CMOS bandgap current reference is shown in Fig. 7 [6]. Summing the currents generated from two current generators, one with positive and another with negative proportional to absolute temperature (PTAT) coefficient, to produce the temperature-independent current reference. Then, each individual stable current can be obtained from the current steering circuits. From simulation, a temperature coefficient of 1.33 nA/°C and less than ±0.25 μA (±2.5% of the full-scale) for a ±10% change of supply voltage have been achieved.

The common-mode voltage is generated through the use of a simple resistor string with a voltage follower. But for the high-precision required reference voltage, a high-performance multi-stage buffer with external stabilization capacitor is employed as shown in Fig. 8 [7]. The two pre-amps are designed with low-gain but large bandwidth, while the last-stage is a high-*gm* op-amp for driving the resistance feedback and minimize the output impedance of the buffer with low-power dissipation.

3.5 Layout

Fig. 9 shows the 28-pin padded layout of the full-integrated prototype in CADENCE™ with 0.35-μm 3-metal 2-poly CMOS.

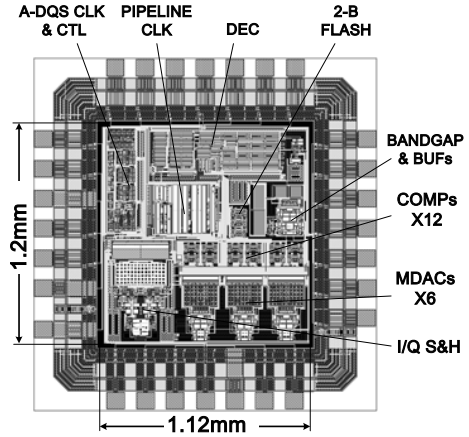


Fig. 9. Layout of the proposed pipelined ADC.

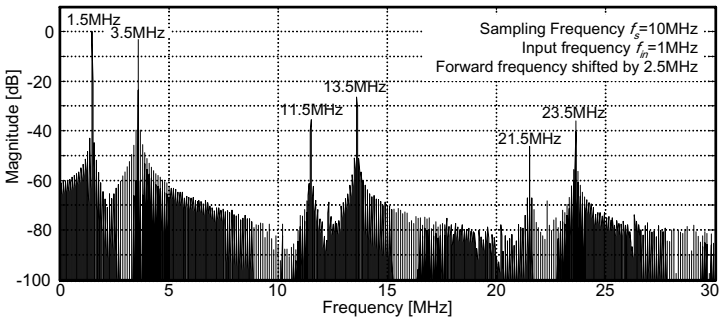


Fig. 10. FFT results $|I+jQ|$ of a 1-MHz sinusoidal signal applied in the A-DQS S/H pair with assumed forward shifting.

The substrate noise coupling in this mixed-signal environment is minimized through careful floor planning, multi-dimensional shielding and individual analog and digital power supplies. Ample substrate contacts and symmetrical traces routing are utilized throughout the analog functional blocks. The matching between the differential and *I/Q* paths of the S/H are maximized through common-centriod and dummy-periphery layout geometry to reduce the DC offset and *I/Q* mismatch. The guard-ringed pads are electrostatic discharge (ESD) protected with reversed-biased PN diodes. The total active chip area is 1.34 mm^2.

4. SIMULATION RESULTS

A-DQS S/H front-end - for simplicity, only the operation of A-DQS for forward frequency shifting (as mentioned in Section 2) will be shown. The simulated Fast Fourier Transform, FFT $|I+jQ|$ is shown in Fig. 10 with a 1-MHz sinusoidal input signal sampled at f_s=10 MHz by the A-DQS scheme. This figure is observed in complex-signal perspective, therefore the input can be considered as one positive 1-MHz and one negative 1-MHz tones existed in the two-sided spectrum. Thus, after being sampled-and-held, those tones will be shifted by 2.5 MHz (f_s/4) forwardly and, they are located at $\pm nf_s + (1+2.5)$ MHz and $\pm nf_s + (-1+2.5)$ MHz for *n=1, 2, 3…*The attenuation in their magnitudes is due to the sample-and-hold *sinc* response. The total harmonic distortion (THD) counted up to the 5th harmonics is close to –68.6 dB and the spurious-free dynamic range (SFDR) is 73.2 dB. The image-rejection ratios (IRRs) are 41 dB, 50 dB, 76 dB for 2% gain, 0.5° phase and 2% capacitor mismatches between the *I* and *Q* channels, respectively.

Overall Pipeline ADC - for a 2.3-MHz sinusoidal input signal sampled at 20 MHz by the pipelined ADC, the obtained FFT result is shown in Fig. 11. The achieved ENOB is equal to 7.7 bits, while the SFDR and THD are 57.4 dB and –57.0 dB, respectively. For the static performance, both the maximum INL (±0.5 LSB) and DNL (±0.34 LSB) are within half of the LSB as shown in Fig. 12. The total power dissipation of this chip is 54.5 mW in average for digitization of two channels.

5. CONCLUSIONS

This paper presented the design and implementation of a novel pipelined ADC architecture, which functions IF-to-baseband downconversion, IF channel selection and single-ADC *I/Q* digitization for the recently reported 2-SCS low-IF receiver. These functionalities not only enhance the receiver performance through channel selection partitioning, while simultaneously minimize the power and area consumptions, as well as *I/Q*-mismatch in the baseband through the use of *I/Q*-multiplexing in the pipelined core.

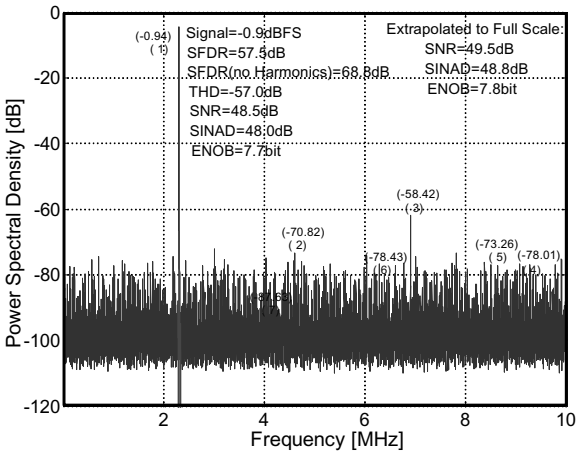


Fig. 11. FFT results of a 2.3-MHz sinusoidal signal input.

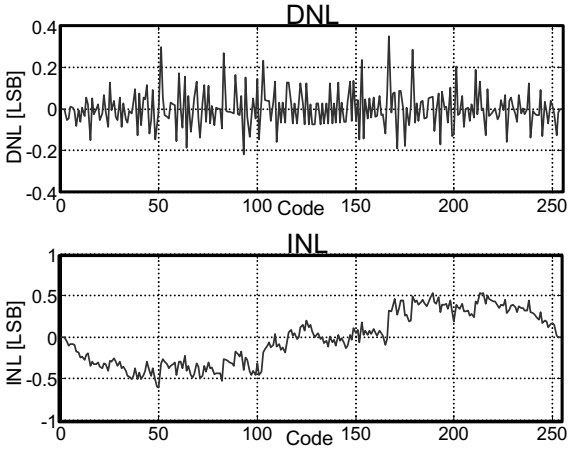


Fig. 12. Simulated DNL and INL.

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