3º Simpósio de Electrónica das Telecomunicações

Oporto, 4-6 May 1988.

DESIGN AND IMPLEMENTATION OF A CMOS INTEGRATED CIRCUIT SC DECIMATOR FOR HIGH FREQUENCY APPLICATIONS

R.P.Martins[1], J.E.Franca[1], F.Maloberti[2].

1- Centro de Electrónica Aplicada da U.T.L. e Departamento de Engenharia Electrotécnica e de Computadores do I.S.T, Lisboa.

2 - Dipartimento di Elettronica, Universitá degli Studi di Pavia, Pavia, Italia.

Abstract

The design and Integrated Circuit(IC) implementation of a high-frequency Switched-Capacitor(SC) lowpass decimator using an advanced 1.5µm CMOS technology is presented. To completely characterize the circuit performance limitations imposed by the non-ideal behaviour of the Operational Amplifiers(OA's), four different versions of this SC lowpass decimator have been implemented using high speed-low power OA's with different gain-bandwidth products. Extensive computer simulations indicate, for the optimum circuit design, a maximum frequency decimation capability from 45MHz to 15MHz with a total power consumption of only 1.5 mW.

1. INTRODUCTION

One of the strategic goals of state-of-the-art, research in Analogue Signal Processing technology is the design of high frequency and very high frequency Switched-Capacitors(SC) circuits and systems, mainly for applications in video signal processing, mobile communications and high speed data transmission [1]. SC decimator and interpolator building blocks have a great potential for such applications, and, particularly, for those requiring a filtering function together with a sampling rate alteration [2,3].

An SC decimator is a specialised SC network that implements a sampling rate reduction from MF_S to F_S together with an appropriate filtering function to reject the unwanted alias frequency components associated with the lower sampling rate F_S. SC decimators can have either FIR or IIR transfer functions depending on the system specifications. FIR SC decimators are more suitable for applications requiring multinotch stopband approximations [2]. For high selectivity applications, on the contrary, IIR SC decimators are usually employed on account of the reduced complexity of the resulting circuit [3].

For the implementation of IIR SC decimators there are currently available three alternative classes defined according to the speed requirements of the OA's. These are schematically illustrated in Fig.1 [3,4]. In a non-optimum IIR SC decimator (Fig.1-a), consisting of an input SC filter operating at MF_S followed by an output sampling switch operating at F_S, the speed requirements of the OA's are imposed by the high input sampling frequency MF_S. Sub-optimum IIR SC decimators (Fig.1-b) can be implemented using a combination of an SC filter operating at MF_S together with a non-recursive polyphase structure with a sampling rate reduction factor M [3]. This configuration gives greater design flexibility than non-optimum configurations, and also allow slower OA's in the polyphase structure operating at the low sampling frequency F_S. Finally, in the optimum class of IIR SC decimators (Fig.1-c), all the OA's operate at the lower sampling frequency F_S thus making them particularly suitable for very high-frequency applications [4-6].

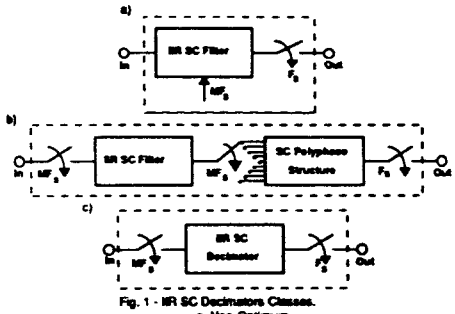


Fig. 1 - IIR SC Decimators Classes.
a- Non-Optimum.
b- Sub-Optimum.
c- Optimum.

This paper is concerned with the design and IC implementation of a high-frequency IIR SC lowpass decimator with optimum implementation. To fully characterize the behaviour of this circuit under non-ideal characteristics of the OA's we have carried-out an extensive computer-based evaluation of four different versions of the basic circuit using different types of high performance OA's. This study, has shown that the two OA's in the circuit have rather different effects in the overall frequency response. As a result, we have been able to obtain an optimized SC decimator design using appropriately tailored OA's and which is expected to achieve a maximum frequency decimation capability from 45MHz to 15MHz with a total power consumption of only 1.5mW. This has been implemented in IC form using an advanced 1.5µm CMOS analogue technology.

2. SC LOWPASS DECIMATOR WITH M=3

The SC lowpass decimator considered in this paper is designed to reduce the sampling rate from $3F_S$ to F_S (M=3), and possess a 2nd. order Tchebyshev lowpass frequency response with passband ripple of 0.01dB and normalized cut-off frequency of $F_C/F_S = 0.013$.

Modified z-Transfer Function : Based on a computer aided filter synthesis procedure [7], we obtain for the corresponding prototype filter the bilinear discrete-time coefficients given in Table 1. The modified z-transfer function for optimum implementation of this SC decimator can be written as [5]

$$\bar{H}(z) = \frac{\sum_{i=0}^{4} a_i \, z^{-i}}{1-(2r_p)^3 \cos(30_p)\, z^{-3}+(r_p)^6 \, z^{-6}} \qquad (1)$$

where, for unity gain factor, the modified discrete-time coefficients, are given in Table 2. The unit delay period, in (1), refers to the input sampling frequency $3F_S$.

F_p (MHz)	1.152
k	1.6833985E-1
$2r_p\cos(\theta_p)$	-2
r_a^2	1
$2r_p\cos(\theta_p)$	1.8832212
r_p^2	0.88996253

Table-1: Bilinear discrete-time coefficients of the 2nd. order lowpass prototype filter.

Numerator			
ao	1		
a1	3.88322	Denominator	
a2	5.75976	b1	-1.65090
a3	8.87234	b2	0.78488
a4	6.80060	$b1=(2r_p)^3\cos(3\theta_p)$	
a5	3.26006	$b2=(r_p)^6$	
a6	0.79203		

Table-2:Discrete-Time Coefficients of the SC Lowpass Decimator.

SC Decimator Circuit : In order to implement the above transfer function we have designed the SC decimator circuit shown in Fig.2-a, which operates with the switching waveforms of Fig.2-b and can be described by the following z-transfer function [5]

$$T_1(z)=\frac{[B\bar{X}(z)-(C+E)\bar{Y}(z)]+[E\bar{Y}(z)-B\bar{X}(z)]\,z^{-3}}{BD+(AC+AE-2BD)\,z^{-3}+(BD-AE)\,z^{-6}} \quad (2)$$

The denominator function is realized by a basic Two Integrator Loop (TIL) structure operating at the low output sampling frequency F_s that determines the speed requirements of the OA's. The numerator function is essentially determined by the input SC branches organized as polyphase structures [2,8] and whose equivalent transfer functions represent the terms $\bar{X}(z)$ and $\bar{Y}(z)$. After scaling for maximum signal handling capability and minimising the capacitance spread we arrive at the final normalized capacitance values given in Fig. 2-c. Fig. 3-a and Fig. 3-b illustrate, respectively, the nominal passband and overall baseband computer simulated amplitude responses [9] of this SC lowpass decimator using ideal OA's (gain=10^{12}).

For the practical IC implementation of the SC decimator we have also to consider the design of the OA's in the circuit and determine the resulting frequency response deviations due to their non-ideal characteristics. For this purpose we have carried-out the computer-based evaluation described next, and which led us to optimally tailor the design of the OA's for maximum speed of operation and minimum power consumption.

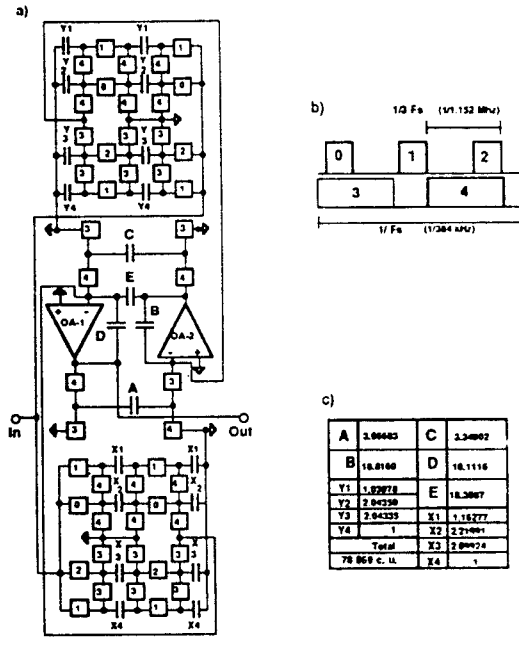
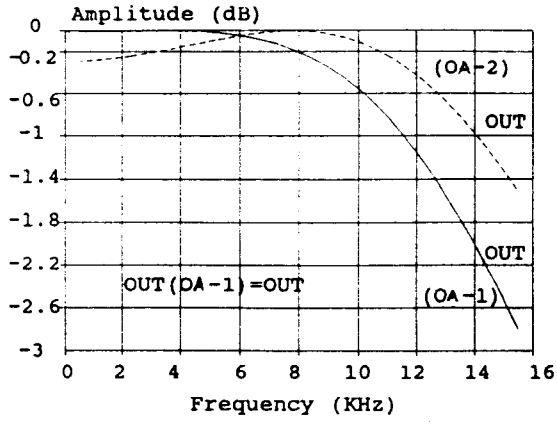


Fig. 2 - SC Lowpass Decimator (M=3).
a- SC circuit.
b- Switching wavoforms.
c- Capacitor values.



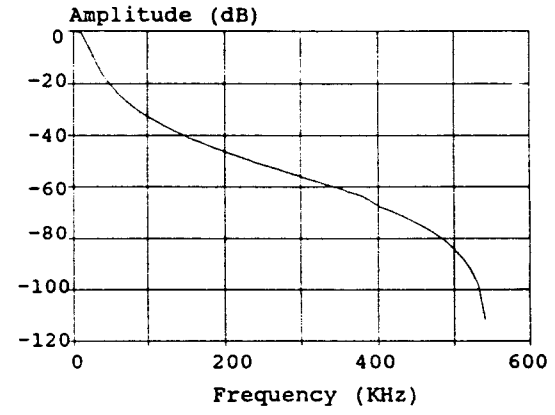


Fig.3-SC Lowpass Decimator Output Response.
a-Passband.
b-Baseband (DC-3Fs/2).

3. CIRCUIT PERFORMANCE LIMITATIONS DUE TO NON-IDEAL OA's.

One of the most important aspects affecting SC circuits performance for high-frequency applications is the non-ideal behaviour of the OA's characterized by their finite DC-gain and bandwidth. To determine the effect of such non-ideal characteristics on the performance of the above SC decimator, and thus determine the corresponding limits of operation, we have carried-out an extensive computer-based evaluation using the simple amplifier model of Fig. 4. The finite DC gain is determined by the gain factor-K_o of the voltage-controlled-voltage-source, whereas the finite bandwidth is determined by the pole frequency associated with the SC branch and capacitor simulating a first order RC section. The most significant results of this evaluation are summarized in Figs. 5 to 10, showing the baseband amplitude responses of the decimator for different values of the DC-gain and gain-bandwidth product of the amplifiers. Figs. 5 and 6 clearly show that this circuit exhibits much greater sensitivity of its amplitude response due to the finite DC-gain of OA-2 than due to the finite DC-gain of OA-1 [10]. Therefore, for a maximum allowed passband error of 0.004dB the minimum tolerable DC-gain of OA-2 is 80dB whereas OA-1 can have a finite DC-gain as low as 40dB. Fig.7 gives the computer-simulated amplitude response of the SC decimator with combined DC-gain values of 80dB for OA-2 and 40dB for OA-1. By considering these DC-gain values for the OA's, we have next evaluated the performance of the SC decimator with respect to the aditional non-ideal finite bandwidth characteristic. To obtain negligible response deviations (passband error below 0.005 dB), Figs. 8 and 9 indicate that the gain-bandwidth products of the amplifiers must be above $3.6F_s$ and $2.4F_s$, respectively for OA-2 and OA-1. These results show that for minimising power consumption the OA's of the SC decimator can be appropriately tailored according to the above minimum specifications. Fig. 10 shows the resulting computer-simulated amplitude response of the SC decimator with such combined finite gain-bandwidth products of the amplifiers.

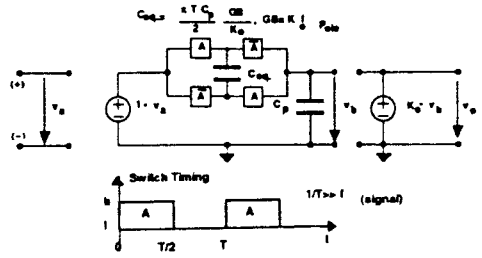


Fig. 4 - SC Model of the OA with finite Gain-Bandwidth(GB) product.

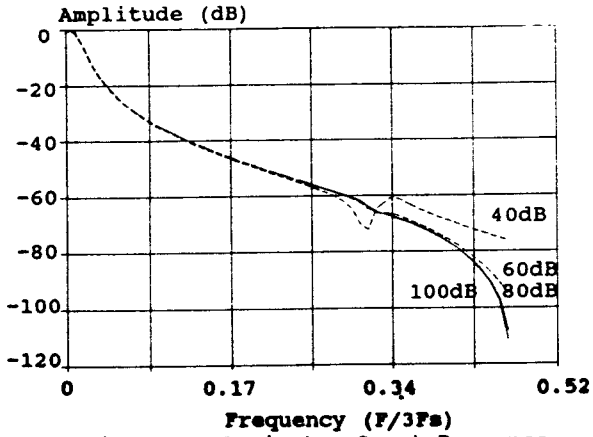


Fig.5- SC Decimator Ouput Response.
- OA-1 Ideal DC gain.
- OA-2 100dB,80dB,60dB,40dB.

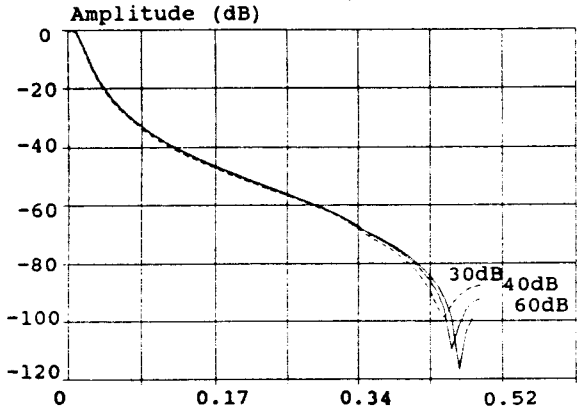


Fig.6- SC Decimator Output Response.
- OA-2 Ideal DC Gain.
- OA-1 60dB,40dB,30dB.

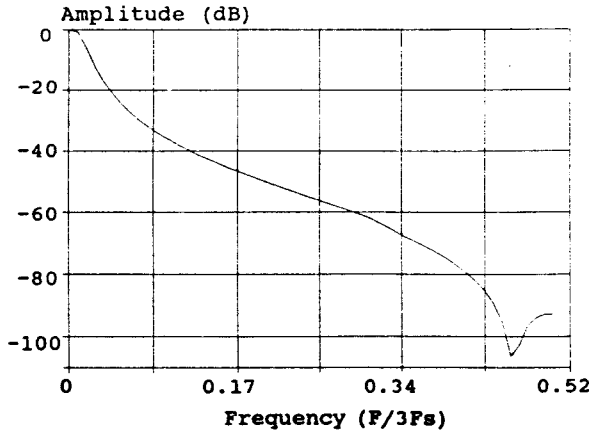


Fig.7- SC Decimator Output Response
(OA-1=40dB, OA-2=80dB).

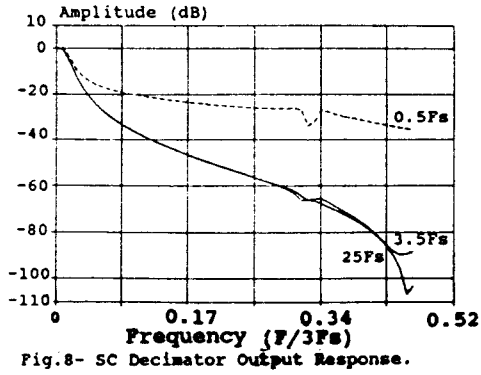


Fig.8- SC Decimator Output Response.
- OA-1 DC Gain=40dB, GB=Infinite.
- OA-2 DC Gain=80dB, GB=25Fs,3.5Fs,0.5Fs.

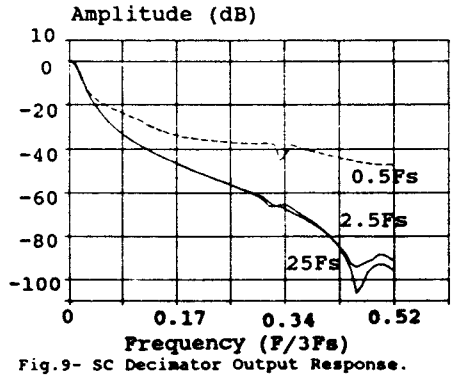


Fig.9- SC Decimator Output Response.
- OA-2 DC Gain=80dB, GB=Infinite.
- OA-1 DC Gain=40dB, GB=25Fs,2.5Fs,0.5Fs.

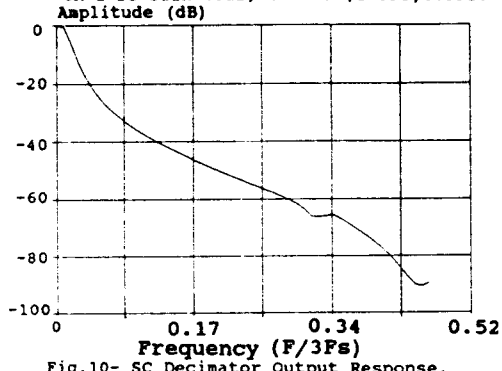
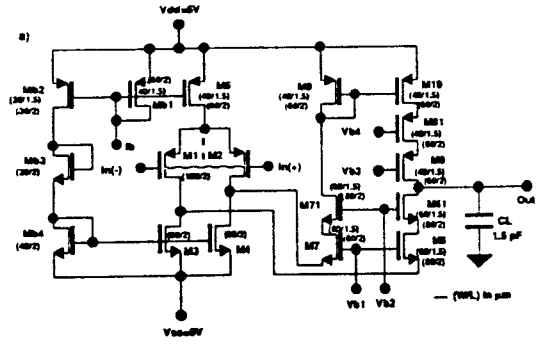


Fig.10- SC Decimator Output Response.
- OA-1 DC Gain=40dB,GB=2.4Fs.
- OA-2 DC Gain=80dB,GB=3.6Fs.

4. IC IMPLEMENTATION.

Operational Amplifiers : Based on the previous evaluation we designed two different types of OA's, which we shall designate as OP-A and OP-B. **OP-A** has the architecture illustrated in Fig. 11-a which can be considered as a single-stage folded cascode amplifier [11]. This structure exhibits a very large unity-gain bandwidth characteristic, and its dominant pole, at low frequency, is imposed by the very high output impedance. To increase the amplifier gain some aditional transistors have been positioned in the cascode stage, which can then be viewed as a "triple" cascode. The fundamental characteristics of this amplifier, obtained by computer simulation [12], are presented in Table 3 indicating a 90dB DC-gain, 80ns settling time and 66° phase margin. To avoid a possible gain reduction due to the variation of the transconductance value in the cascode transistors realized with minimum feature size (1.5µm) we have also designed a modified version of this amplifier, designated **OP-A1**, using transistors with slightly longer channels (2µm). The IC implementation of OP-A is illustrated in Fig. 11-b [13]. **OP-B** has the structure presented in Fig. 12-a consisting of only an inverter stage (Cascoded - Push-Pull) with relatively low DC-gain (40dB) and very high speed of operation (settling time close to 50ns). The main characteristics of this amplifier are also given in Table 3. The IC implementation of OP-B is presented in Fig. 12-b [13].



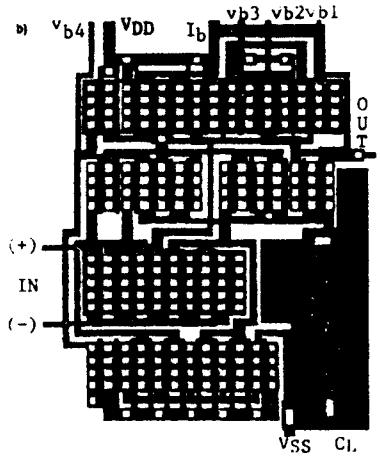
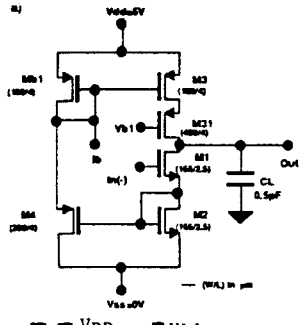
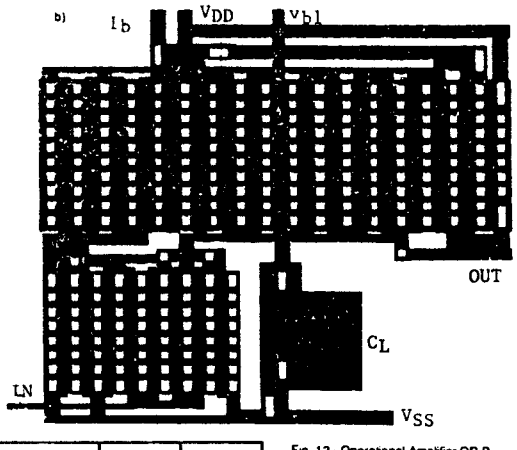


Fig. 11 - Operational Amplifier OP-A and OP-A1.
a- CMOS Circuit Structure
b- IC Implementation.





Characteristics	OP-A	OP-B
DC-Gain (dB)	90	40
GB (MHz)	20	80
Phase Margin (°)	66	——
Settling Time (ns)	80	50
Input Offset (mV)	16	——
Power Cons. (mW)	0.76	2.6
IC Area (μm^2)	125x160	160x140

Fig. 12 - Operational Amplifier OP-B.
a- CMOS circuit structure.
b- IC implementation.

Table-3: Operational Amplifiers Simulated Characteristics.

Analogue Switches : To design analogue switches that allow very high speed of operation together with low on-resistance we have adopted the circuit structure of Fig.13-a. The transistors dimensions are different for the input SC branches and for the SC branches of the TIL structure, due to the fact that capacitors Xi's and Yi's have considerably smaller values than capacitors A,B,C,D,E. Such dimensions allow higher currents in the TIL structure branches without increasing the on-resistance of the analogue switches, thus implying better performance at high frequencies. The on-resistance for both cases, in Fig. 13-b, is also evaluated by a computer simulation [12].

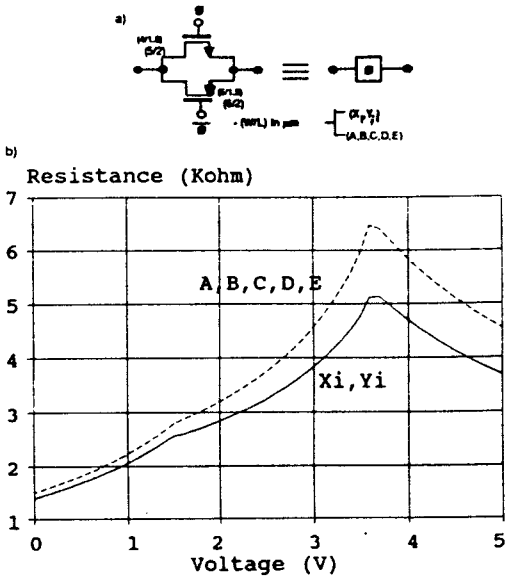


Fig.13- Analogue Switches.
a-Circuit Structure.
b-On-Resistance.

Final Architecture : The different designs of the OA's considered before led to the four basic SC decimator cells with the arrangements presented in Table 4. The final IC architecture with all four versions of the SC lowpass decimator is presented in Fig. 14 [13] occupying a total silicon area of 2x2.5mm^2. It is expected (prototype samples not being available at the writing of this paper) that the optimum design of this SC decimator can achieve a maximum decimation frequency capability from 45MHz to 15MHz consuming a total power of only 1.5mW.

Arrang.	OP-1	OP-2
1	OP-A	OP-A
2	OP-A1	OP-A1
3	OP-B	OP-A
4	OP-B	OP-A1

Table-4:Different Arrangements of OA's in the decimator.

5. CONCLUSIONS

This paper presented the design and IC implementation of a 2nd. order SC lowpass decimator appropriate for high frequency applications using an advanced 1.5µm CMOS technology. The design strategy started with the complete characterization of the basic limitations of this novel type of SC circuit, essentialy with respect to the non-ideal behaviour of the OA's, and led to the implementation of four different versions of the same SC lowpass decimator basic cell. The optimized design for maximum speed of operation and minimum power consumption employs two OA's with rather different gain-bandwidth products. It is expected that these circuits can achieve a maximum frequency decimation operation from 45 MHz to 15 MHz, with a total power consumption of only 1.5 mW, and can therefore be particularly attractive for video signal processing applications.

References

[1] - K.Nakayama,Y.Kuraishi,"Present and Future Applications of Switched-Capacitor Circuits", *IEEE Circuits and Devices Magazine*, pp. 10-21, September 1987.

[2] - J.E.Franca,"Non-Recursive Polyphase Switched Capacitor Decimators and Interpolators",*IEEE Transactions on Circuits and Systems*, vol. CAS-32, No.9, pp.877-887, September 1985.

[3] - J.E.Franca,"IIR Switched-Capacitor Decimators and Interpolators with Biquad-Polyphase Structures", *29th. Midwest Symposium on Circuits and Systems*, pp.797-800,August 1986 ,Lincoln, Nebraska,USA.

[4] - J.E.Franca,D.G.Haigh,"Optimum Implementation of IIR Switched-Capacitor Decimators", *Proc. ISCAS'87*, vol.1,pp.76-79,May 1987,Philadelfia, USA.

[5] - J.E.Franca,R.P.Martins,"IIR Switched-Capacitor Decimator Building Blocks", submitted to publication in the *IEEE Trans. on Circuits and Systems*.

[6] - R.P.Martins,J.E.Franca,"Optimum Implementation of a Multistage IIR SC Bandpass Decimator for a voiceband Analogue Interface System",to be published in the *Proc. IEEE-"ISCAS'88"*,Helsinki, Finland.

[7] - G.Szentirmai,"S/Filsyn Quick Reference Manual", April 1983.

[8] - P.Fleischer,A.Ganesan,K.Laker,"Parasitic-Compensated Switched-Capacitor Circuits", *Electronics Letters*,vol.17,No.24,pp.929-931, 26th. November,1981.

[9] - S.C.Fang,"Switcap User's Guide",Columbia University, October 1982.

[10]- E.Sanchez-Sinencio,J.S.Martinez,R.L.Geiger, "Biquadratic SC Filters with small GB Effects", *IEEE Transactions on Circuits and Systems*, vol.CAS-31,No.10,pp.876-884, October 1984.

[11]- P.R.Gray,"Basic MOS operational amplifier design-An overview",Analog MOS Integrated Circuits, *IEEE Press Selected Reprints Series*, Wiley,New York, pp. 28-49,March 1980.

[12]- L.Nagel,"SPICE2: A computer program to simulate semiconductor circuits", ERL Memo.No. VCB/ERL M75/520, May 1975.

[13]- K.Keller,G.Billingsley,"KIC: A Graphics Editor for Integrated Circuits",University of California at Berkeley,1980.

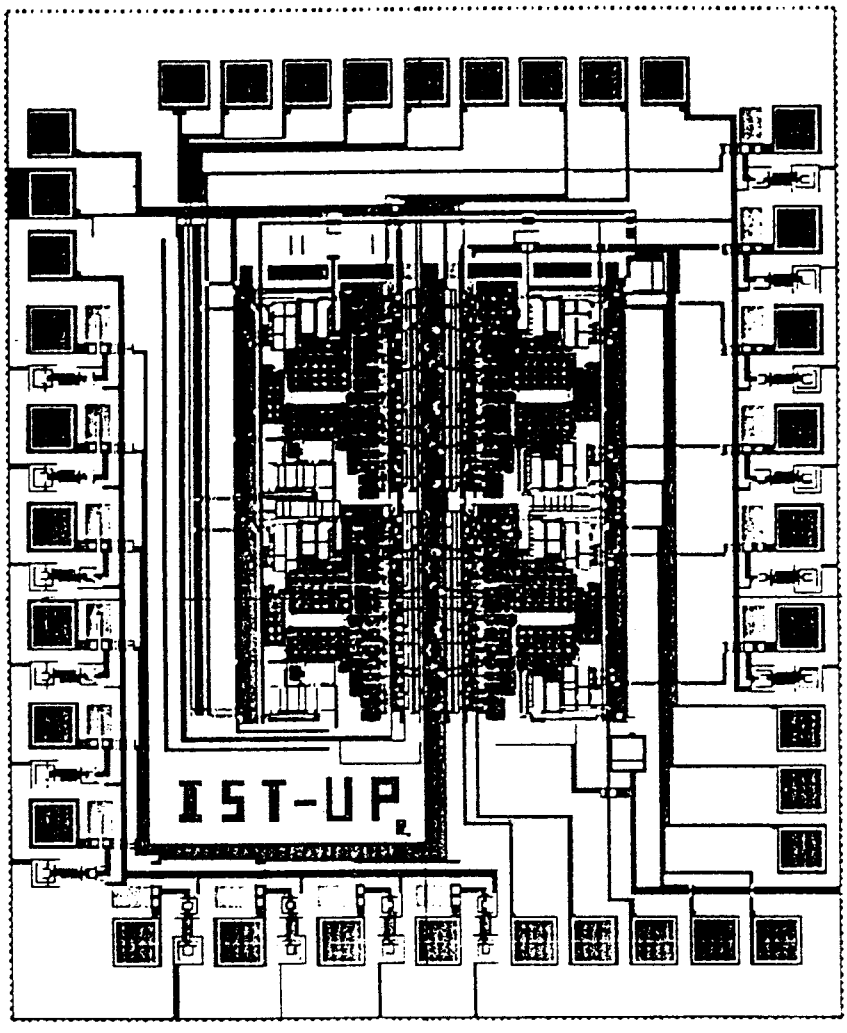


Fig.14- SC Decimator Total IC Implementation.