FREQUENCY-DOWNCONVERSION AND IF CHANNEL SELECTION A-DQS SAMPLE-AND-HOLD PAIR FOR TWO-STEP-CHANNEL-SELECT LOW-IF RECEIVER

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ABSTRACT

A novel *I/Q* sample-and-hold (S/H) pair for a recently proposed two-step-channel-select low-IF receiver, which performs both IF-to-baseband frequency down-conversion and IF channel selection, will be presented. Both functions are mainly implemented through a controllable Analog-Double Quadrature Sampling (A-DQS) technique, which can effectively perform forward/backward frequency shifting through simple digital control. Thus, a new two-step channel selection method is proposed to significantly relax the front-end frequency synthesizer phase noise and locking time requirements, by partitioning the channel selection process from the FS to the proposed S/H pair. A prototype is designed in CADENCE™ environment with 0.35-μm CMOS process parameters and adopting various circuit techniques for minimization of the image problem due to the *I/Q* mismatch.

Keywords: Analog-double quadrature sampling, complex low-IF receiver, channel selection, frequency downconversion

1. INTRODUCTION

Complex low-IF wireless receiver [1-3] promises both low-power consumption and high-integration by utilizing a complex signal frequency down-conversion method instead of off-chip filtering. Thus, the Intermediate Frequency (IF) can be set as low as half-channel bandwidth value to reduce the image-rejection requirement [2] and simplify the following IF circuitry, while still high-insusceptible to the DC-offset and *1/f* noise. Regrettably, low-IF operation implies low step-size changing of the local oscillator (LO) frequency during channel selection. For communication systems such as Bluetooth™, IEEE 802.11b WLANs (FHSS) or HomeRF™ which employ a frequency-hopping spread spectrum (FHSS) technique, the high-speed switching of the LO controlled by the frequency synthesizer (FS) in such small step-size mandates large bandwidth of the loop filter and large division ratio of the frequency divider in the frequency synthesizer (FS). The resulting major drawbacks are the long locking time and large phase noise values of the LO [3]. Moreover, the total mandatory moving steps of the LO position is equal to the number of channels in the entire frequency band.

In this paper, we propose a novel two-step-channel-select low-IF receiver topology to alleviate the problems mentioned above and simplify the front-end FS structure through the partition of the channel selection process from the RF front-end to the IF by utilizing a controllable *I/Q* sample-and-hold (S/H) pair employing Analog-Double Quadrature Sampling (A-DQS) technique. The proposed receiver topology is shown in Fig. 1, where the functionalities of such S/H circuit include the IF-to-baseband frequency down-conversion and IF channel selection. Since the detailed theoretical analysis is presented in [4] and due to space limitation, this work will mainly concentrate on the implementation of the S/H circuit and the channel selection controller, as presented in the block diagram of STEP 2 (Fig. 1).

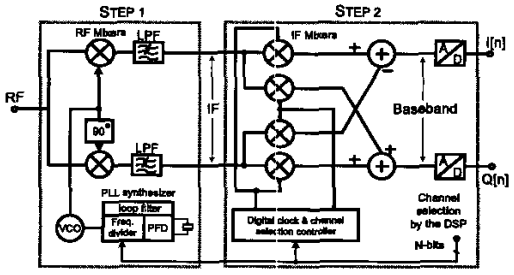

Figure 1. Proposed two-step-channel-select low-IF receiver

In Section 2, the principles of A-DQS will be briefly reviewed first. The circuit implementation will be presented in Section 3. Simulation results are provided and discussed in Section 4, and conclusions will be drawn in Section 5.

2. CHANNEL SELECTION BY A-DQS

Four sampling mixers [5] are necessary to obtain complex-to-complex frequency down-conversion prior to the A/D conversion leading to an A-DQS structure [4, 6-7]. With the sampling frequency f_s=4xIF and utilizing pseudo-differential circuit implementation, the mandatory multiplying values are only 1, 0 or –1. Hence, the A-DQS technique can be effectively embedded on a pair of S/H circuits with high precision matching in the *I* and *Q* channels.

The second function that can be extracted from the A-DQS technique explored in [4] is related with its frequency shifting properties that allow the implementation of the channel selection function. Those will imply that when the IF is set to half of the channel bandwidth value the image and the desired channel are neighbors. Thus, by utilizing the forward/backward frequency shifting characteristics of the A-DQS, the down-converted channels can be selected in between the desired channel or its adjacent one, through simple digital control and different sampling sequences. As a result, the channel selection process can be divided into two steps. The first step is still performed by the FS through the positioning of the LO frequency in between every two channels as shown in Fig. 2a and b for the traditional

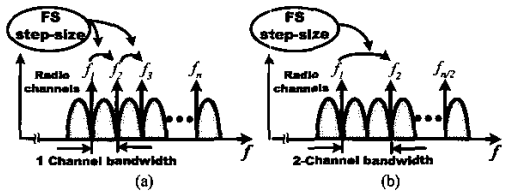

Figure 2. Channel selection by the frequency synthesizer (a) traditional method and (b) proposed method

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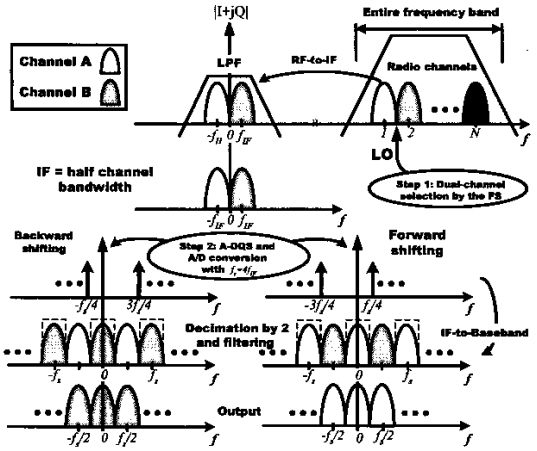

Figure 3. Spectra illustrations of proposed two-step channel selection

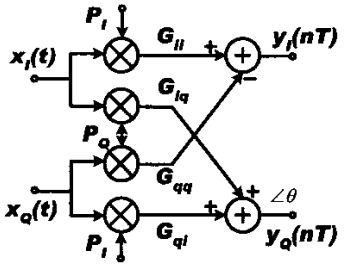

Figure 4. Non-ideal model of A-DQS scheme

and proposed methods. Obviously, the frequency resolution of the FS now is relaxed by 1 channel bandwidth, and the total number of locking position of the LO is halved. The second step is performed by the controllable A-DQS in the IF, the desired signal and its image (its adjacent channel) can be selected to the baseband through the digital controller. The spectra flows of the entire channel selection from RF-to-baseband are explained graphically in Fig. 3 for two arbitrary adjacent channels, named **A** and **B**. First, the RF-to-IF frequency downconversion selects the channel **A** and **B** to the IF by locating the LO frequency in between such channels, then, after lowpass filtering, the channels that have been settled adjacently with each other can be selected from the IF to the baseband through the A-DQS circuit and the digital controller. Finally, the desired channel can be obtained after A/D conversion, filtering and decimation by 2.

Regrettably, analog circuits suffer unavoidable *I/Q* mismatch leading to serious image problems. The non-ideal model of the A-DQS scheme is shown in Fig. 4. The P_I and P_Q are the complex samplers and the amplitude mismatches in the 4 paths are denoted as G_{ii}, G_{iq} G_{qi} and G_{qq}, .The image-rejection ratio (IRR) is given by [7]

$$IRR = \frac{1}{(\Delta G/2)^2} \tag{1}$$

With 1% amplitude mismatch, the IRR is limited to approximate 46dB. For the phase mismatch, the IRR is given by

$$IRR = \frac{1}{(\theta/2)^2} \tag{2}$$

where θ is the phase mismatch. Also, for 1° phase mismatches, the IRR is limited to around 41dB. Therefore, such A-DQS technique is appropriate for low-IF operation, where the gain and phase mismatches can be well controlled.

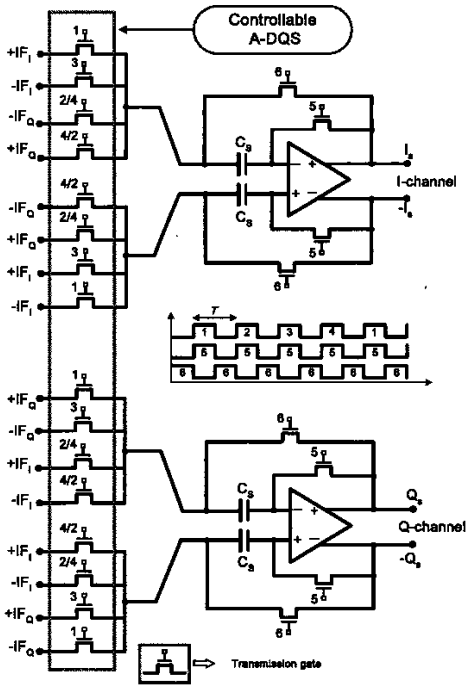

Figure 5. Fully-differential A-DQS S/H pair

3. CIRCUIT IMPLEMENTATION

3.1. A-DQS Sample-and-Hold pair

The prototype circuit of the A-DQS and the digital controller are implemented in 0.35-μm CMOS technology in a CADENCE™ environment with 2.5V power supply. Each part of the circuit can be introduced as follows:

As shown in Fig. 3, after the IF-to-baseband frequency down-conversion by A-DQS, the desired channel at the baseband will be directly affected by the DC-offset and $1/f$ noise of the following circuits. In order to minimize such noises, two Switched-Capacitor (SC) S/H circuits can be employed to realize such A-DQS, as shown in Fig. 5, which uses the technique of bottom-plate sampling. Such S/H circuits not only possess a high feedback factor to minimize the required gain-bandwidth of the op-amp, but also inherently provide a transmission zero at DC to minimize the effect of their noises in the desired signal. The operational transconductance amplifiers (OTAs) are gain-boosted with telescopic type structure including SC common-mode feedback, as shown in Fig. 6, with the corresponding performance parameters listed in Table 1. The

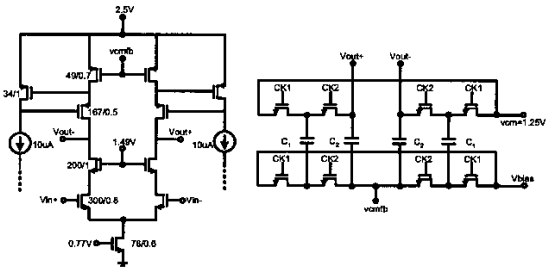

Figure 6. The OTA and common mode feedback circuit of the A-DQS S/H pair

Table 1. Performance of the OTA

Open loop DC gain	88.6dB
Unity gain frequency	207MHz
Phase margin	63.4°
Slew rate	113V/μs
Sample/load capacitances	1pF
Differential output swing	1.56V
Supply voltage	2.5V

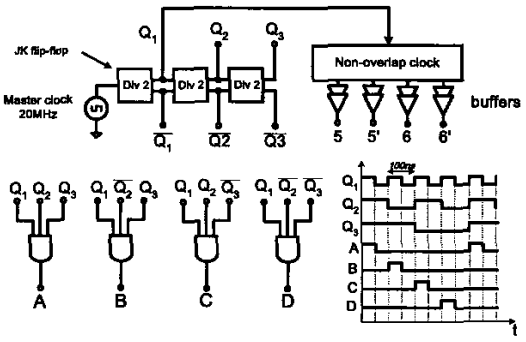

Figure 7. Mismatch insensitive clock phase generator

switches are implemented with transmission gates (TGs) to minimize the distortion through the signal-dependent charge injection, allowing also the increase of the signal dynamic range. The design of the dimensions of all TGs is made having into consideration *1/f* and thermal noises, *I/Q* matching, clock feedthrough effects and settling time.

3.2. Mismatch insensitive clock phase generator

The sequential clock phases of the A-DQS are generated by the 20MHz master clock, which is shown in Fig 7. The three clock dividers are implemented by JK flip-flops to obtain the clock phase 1-4 through logical operations. The clock phases 5 and 6 are the non-overlapping clock phases with frequency equal to 10MHz. The advantages of those logical operations are 1) synchronization of clock phases 1-4 to 5 with minimum number of logic operations. 2) Elimination of the phase errors of clock 1-4 due to propagation delay in the clock divider, since they are always synchronized. Thus, the time-skew effect, clock jittering and *I/Q* mismatch can be effectively reduced [8].

3.3. A-DQS channel selection controller

As shown in Fig 8, the channel selection digital controller is a 1-bit decision circuit for forward/backward frequency shifting during sampling. Obviously, the channel selection cannot be

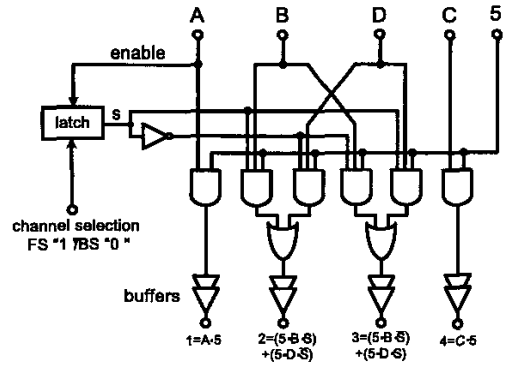

Figure 8. A-DQS channel selection controller

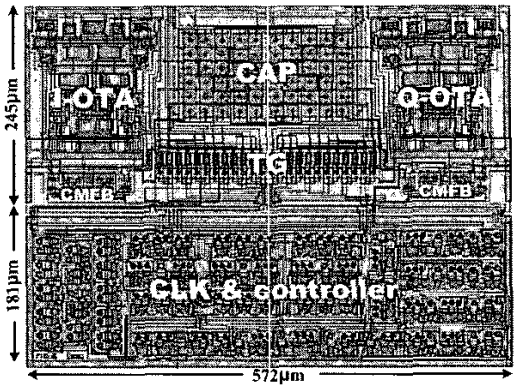

Figure 9. Layout of the proposed A-DQS S/H pair

triggered in between the sampling sequence; thus, the channel selection is enabled only by the clock phase 1 on every 4 sampling periods. In this work, the sampling frequency is 10MHz; the time needed to change the signal acquisition is 400ns, which is fast enough for any fast frequency-hopping wireless communication applications. The final gate-driving clocks are again synchronized with phase 5 to eliminate any phase errors due to different propagation delays in the controller and, simultaneously, to reduce the signal-dependent charge injection from the switches. The channel selection disturbs only the control paths, thus, there is no transient effect on the signal paths and, consequently, no influence in the performance of the receiver.

4. Layout and Simulation Results

The layout of the entire proposed circuit is shown in Fig. 9 occupying a total chip-area of 430x582μm^2. The four sampling capacitors are implemented by double-poly silicon and common-centroid geometry to minimize the mismatches. The simulation was conducted with a sampling frequency f_s=10MHz. The performance of the S/H circuit is shown in Fig. 10 by applying a 500kHz test source. The total harmonic distortion (THD) counted up to the 5th harmonics is close to –68.6dB and the Effective Number of Bits (ENOB) is 7.9-bit with 1V_{pp} and a spurious-free dynamic range (SFDR) of 73.2 dB.

For simplicity, only forward frequency shifting operation will be presented here. The simulated power spectrum density (PSD) of both *I* and *Q* channels is shown in Fig 11. After sample-and-held by the A-DQS, the sampled 1MHz input signal is shifted by 2.5MHz ($f_s/4$) and will be located at ±n1.5MHz, ±n3.5MHz,

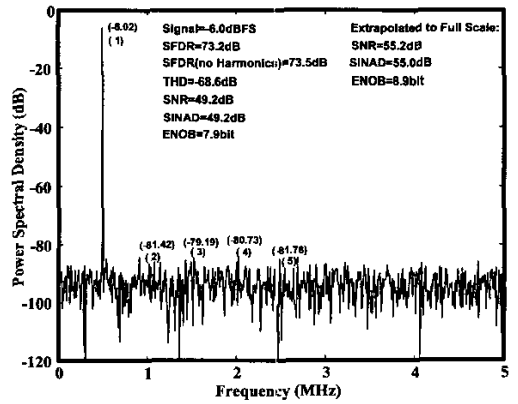

Figure 10. PSD with 500kHz input test source

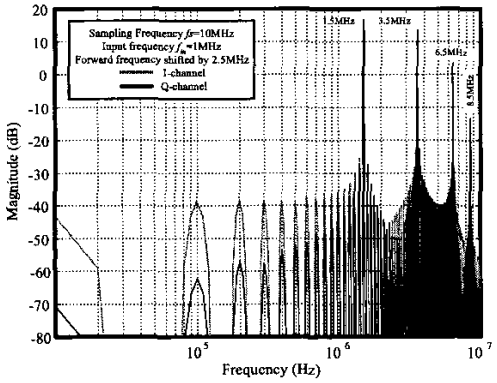

Figure 11. Simulated PSD of *I* and *Q* channels

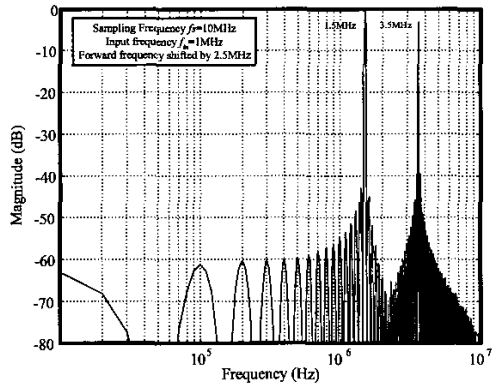

Figure 12. Simulated PSD of $|I+jQ|$

±n6.5MHz and ±n8.5MHz for n=1,2,3.... The attenuation of their magnitudes is due to the *sinc* response of the S/H circuit and not to image-rejection in this case. The signal dynamic range (DR) is greater than 50dB. For the complex PSD ($|I+jQ|$) as shown in Fig. 12, those signals at ±n6.5MHz and ±n8.5MHz for n=1, 2, 3.... are cancelled since the original phase differences between the *I* and *Q* channels are in quadrature. However, any unbalance between such channels will result in an imperfect cancellation. The analysis of the variations of IRR due to capacitor, gain and phase mismatches in the *I* and *Q* channels as shown in Fig. 13 can be discussed as follows:

Since capacitor mismatches between the *I* and *Q* channels will lead to different equivalent RC time constant constructed by the switches ON-resistance and the sampling capacitors, the sampling bandwidth is designed to be higher enough than the signal bandwidth, thus the IRR can still achieve a value greater than 60dB with 5% capacitors mismatch. For the gain mismatch, 1% mismatch degrades the IRR to around 45dB. Since bottom-plate sampling technique is employed, the sampling error is only determined by clock phase 5, resulting only in unimportant self-image problem [7]. Obviously, 45dB self-image-rejection is sufficient enough in most wireless communication applications as it is the case of the direct conversion receiver. The phase mismatch is minimized through the utilization of accurate clock phases, as introduced in previous section. Thus, for 1° phase mismatch, also a general case in CMOS implementation, the IRR is still greater than 40dB. These results show that the proposed A-DQS S/H circuits can achieve high-performance for all the S/H, frequency down-conversion and channel selection functions. Similar

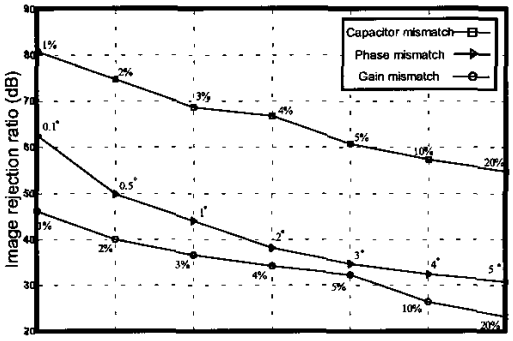

Figure 13. Simulated image-rejection ratio (IRR) versus capacitor, gain and phase mismatch between *I* and *Q* channels

results can be obtained for backward shifting, in which the sampled 1MHz input will be shifted backwardly by 2.5MHz ($f_s/4$) through the digital controller.

5. Conclusions

This paper proposed a sample-and-hold pair with embedded frequency down-conversion and channel selection by utilizing a controllable A-DQS technique. With such circuit operating in the IF stage of complex low-IF receivers, especially for frequency-hopping communication systems, a high-effective two-step channel selection approach can be adopted to, simultaneously, simplify the design complexity of the front-end frequency synthesizer, and reduce the *I/Q* mismatch in the secondary down-conversion. The prototype circuit was designed and verified in a CADENCE™ environment with 0.35-μm CMOS process parameters. This work serves as the basis for the future implementation of the two-step-channel-select low-IF receiver.

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