A Programmable Switched-Capacitor A-DQS Frequency Downconverter for Two-Step Channel Selection Wireless Receiver

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ABSTRACT

This paper presents a combined half- and full-delay switched-capacitor frequency downconverter with embedded channel selection function through a programmable analog-double quadrature sampling (A-DQS) technique. With such circuit operating in a complex low-IF wireless receiver back-end, the IF-to-baseband frequency down-conversion of the desired channel or its image can be effectively selected to the baseband to relax the settling time and phase noise requirements of the front-end frequency synthesizer. Moreover, such circuit also allows *I/Q* multiplexing for the following A/D converter and then minimizes the image problem due to *I/Q* mismatch. The prototype circuit is designed and verified in CADENCE™ environment with the parameters of a 0.35-μm CMOS process.

1. INTRODUCTION

Complex low-IF wireless receivers [1-4] usually employ a very low intermediate frequency (IF) for quadrature frequency downconversion and to minimize the power consumption, as well as, to simplify the circuitry ahead. Thus, a double quadrature IF-to-baseband downconverter is still mandatory prior to signal digitization. Traditionally, a double quadrature downconverter can be implemented by four mixers, which are driven by a quadrature local oscillator (LO) [5]. The problem of such architecture is there exists image interference due to unavoidable paths imbalance. Recently, analog-double quadrature sampling techniques (A-DQS) have been proposed for the double quadrature downconversion and channel selection. In this paper, two distinct switched-capacitor (SC) sample-and-hold (S/H) circuits, with half-delay or full-delay embedding the A-DQS, will be proposed. Their main advantages are: first, without much extra cost, the A/D converters with those S/Hs at the front-end will perform the IF-to-baseband downconversion. Second, to simplify the front-end frequency synthesizer [6] the channel selection can be divided into two steps [7-8]. Third, since such S/Hs achieve also a half- or full-delay, one double-sampled A/D converter can be utilized for the digitization of both channels (*I* and *Q*) through simple multiplexing. Then, the proposed complex low-IF receiver baseband structure will assume the format of Fig. 1.

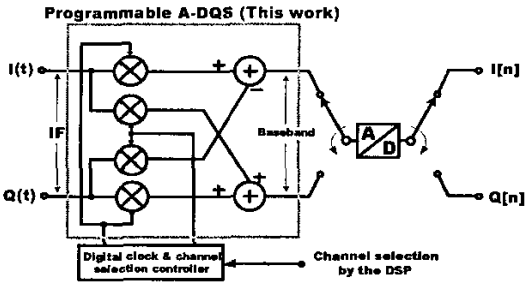

Figure 1: Proposed baseband structure of complex low-IF receiver.

Next, in section 2, the A-DQS will be briefly reviewed followed by the circuit implementation in section 3. The simulation results will be provided in section 4, and finally section 5 will conclude this paper.

2. ANALOG-DOUBLE QUADRATURE SAMPLING

The operation of four sampling mixers in complex-to-complex frequency down-conversion is usually named analog-double quadrature sampling (A-DQS), which can be employed in the baseband of complex low-IF receivers for IF-to-baseband downconversion [7-10]. The main advantage is related with the sampling frequency f_s value, when it is equal to 4 times the IF and utilizing pseudo-differential circuit implementation, the mandatory multiplying values will be only 1, 0 or –1. Hence, in both channels (*I* and *Q*) the A-DQS can be effectively embedded in a pair of S/H circuits of the two A/D converters. Another feature of the A-DQS technique, explored in [6], is its frequency shifting characteristics that will allow the channel selection, and which imply also that, when the value of IF is set to half of the channel bandwidth ,the image and the desired channel will be neighbors. Thus, by utilizing the forward/backward frequency shifting characteristics of the A-DQS, the downconverted channels can be selected between the desired channel or its adjacent one in the IF, through simple digital control on the S/Hs sampling sequences [11], to simplify the front-end voltage control oscillator (VCO) and frequency synthesizer settling time and phase noise requirements.

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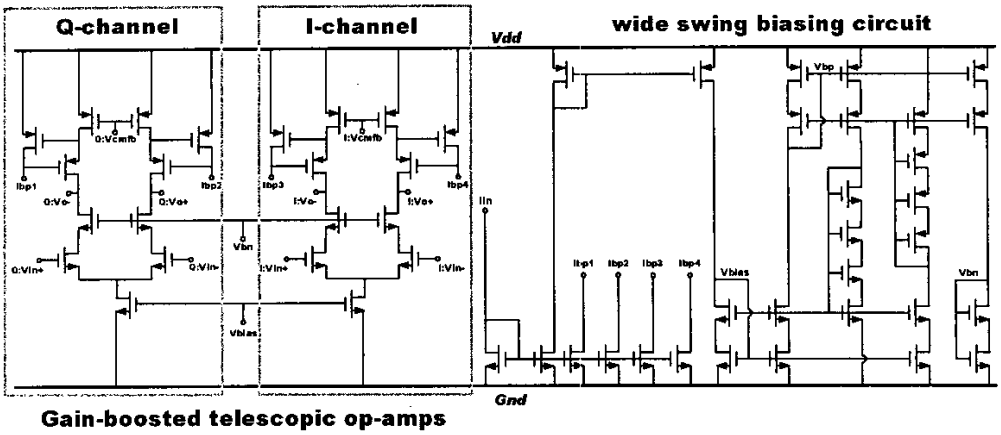

Figure 3: Schematic of the *I* and *Q* channels A-DQS S/Hs OTAs

3. CIRCUIT IMPLEMENTATION

The prototype circuit of the A-DQS is implemented in 0.35-μm CMOS technology in CADENCE™ environment. In complex low-IF receiver, after the IF-to-baseband frequency down-conversion by the A-DQS. the desired channel at the baseband will be directly affected by the DC-offset and $1/f$ noise of the circuitries ahead. To minimize the effects of such noise sources. two switched-capacitor (SC) sample-and-hold circuits are used to realize such A-DQS. as shown in Fig. 2, with also the bottom-plate sampling technique. The half-delay S/H circuits not only possess a high feedback factor to minimize the required gain-bandwidth of the op-amp, but also inherently providing a transmission zero at DC to minimize the effect of those noises into the desired signal. The S/H with full-delay also possesses the transmission zero at DC due to the inversion of polarity in the holding phase. However, at the cost of requesting a higher slew-rate op-amp because the sampled value will start every period, between every positive and negative value. This half and full delay combined structure for the *I* and *Q* channels allows the utilization of one A/D converter to process both channels since the sampled output will be time-interleaved [The non-ideal transfer functions of both half and full-delay S/Hs will be presented later in the appendix]. The operational transconductance amplifiers (OTAs) for both *I* and *Q* channels are gain-boosted telescopic structure with a common wide swing biasing circuit for that will allow the reduction of chip-area and the increase of the matching. The common-mode feedback circuit uses switched-capacitor architecture to minimize the power consumption. The full circuit schematic is shown in Fig. 3 and its typical performance is listed in Table 1. All switches are implemented by transmission gates to minimize the distortion due to signal-dependent charge injection and also to increase the signal dynamic range. The dimensions of all the TGs are balanced having into consideration. $1/f$ noise, thermal noise. *I/Q* matching. settling time and clock

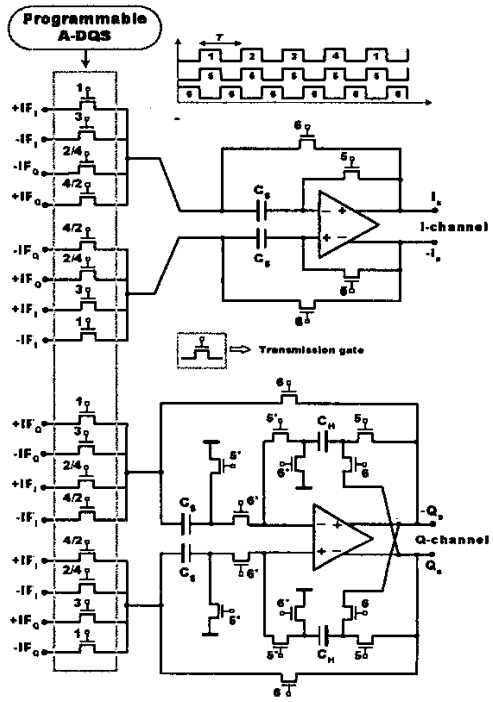

Figure 2: Half and full-delay combined A-DQS S/H circuits.

feedthrough. The clock phases and the channel selection controller can be obtained from [11].

Table 1: Performance of the OTA.

Open loop DC gain	88.6dB
Unity gain frequency	207MHz
Phase margin	63.4°
Slew rate	113V/μs
Settling time	16.19ns
Sample/load capacitances	1pF
Differential output swing	1.46V
Supply voltage	2.5V

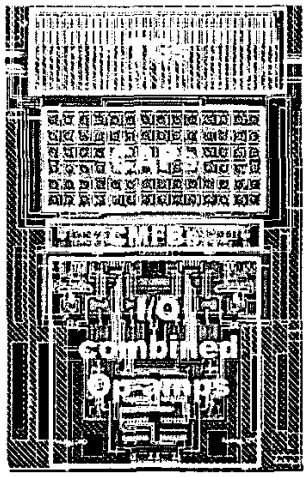

Figure 4: Layout of the A-DQS S/H circuits.

4. SIMULATION RESULTS

The layout of the proposed circuit is shown in Fig. 4 and the active chip-area is 0.17mm^2 (548x310μm) with total 5.05mW power dissipation at 2.5V power supply. The four sampling capacitors are implemented by double-poly with common-centroid geometry in the layout to reduce the non-linearity and mismatches. The simulation was conducted with a sampling frequency equal to 10MHz. The precision of the S/H circuit was tested through the application of a 500mV DC input voltage. After frequency shifting and sampling-and-holding through the A-DQS downconverter, the output held values are 498.718mV and 499.886mV, for the I Channel and the Q Channel, respectively, as shown in Fig. 5. For the frequency downconversion verification, and with the purpose of illustration, only the forward frequency shifting operation will be presented next. The simulated power spectrum densities (PSD) of both channels are shown in Fig 6a with a 1MHz sinusoidal input source. After sample-and-hold and frequency translation operations by A-DQS, the sampled 1MHz input signal is shifted by 2.5MHz (f_s/4) and will have replicas located at ±n1.5MHz, ±n3.5MHz, ±n6.5MHz and ±n8.5MHz with n=1,2,3.... The attenuation of their magnitudes is due to the *sinc* response of the sample-and-hold process, and not due to the image-rejection in this case. For the complex PSD ($|I+jQ|$) that is shown in Fig. 6b, those signals at ±n6.5MHz and ±n8.5MHz with n=1, 2, 3.... are cancelled as the original phase difference between the I and Q channels are in quadrature.

5. CONCLUSIONS

A combined half- and full-delay SC sample-and-hold circuits has been presented for a complex low-IF receiver with embedding frequency downconversion and channel selection functions by utilizing the A-DQS. Such circuit can operate in the IF to perform a high-effective two-step channel selection to simplify

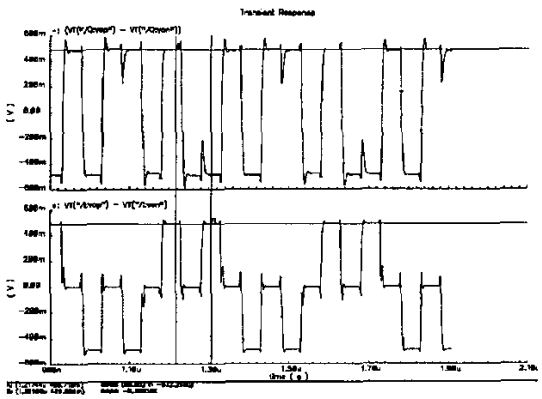

Figure 5: CADENCE™ transient simulation results of Q (upper) and I (lower) channels.

the front-end frequency synthesizer. Moreover, such circuit allows a single A/D converter for the I/Q digitization to minimize the I/Q mismatch and power consumption. The prototype circuit has been designed and verified in CADENCE™ environment with 0.35-μm CMOS technology.

6. APPENDIX

Due to the op-amp finite gain A, voltage offset V_{os} and input parastic capacitance C_{in}, the non-ideal transfer function of the half-delay S/H circuit is given by

$$H(z)=\frac{C_S z^{-\frac{1}{2}}}{\left(C_S+\frac{C_S}{A}+\frac{C_{in}}{A}\right)-\left(\frac{C_S}{A}+\frac{C_{in}}{A}\right)z^{-\frac{1}{2}}} \tag{1}$$

The feedback factor is

$$\beta=\frac{C_S}{C_S+C_{in}} \tag{2}$$

The transfer function of the full-delay S/H circuit is

$$H(z)=-\frac{-C_S V_{in}(z)z^{-\frac{1}{2}}}{\left(1+\frac{1}{A\beta_1}\right)\left(1+\frac{1}{A\beta_2}\right)}+ V_{OS}z^{-\frac{1}{2}}\left[\frac{1+\frac{C_{in}}{C_S}}{\left(1+\frac{1}{A\beta_1}\right)\left(1+\frac{1}{A\beta_2}\right)}-\frac{1+\frac{C_{in}}{C_H}}{1+\frac{1}{A\beta_2}}\right] \tag{3}$$

with the feedback factors

$$\beta_1=\frac{C_S}{C_S+C_P},\beta_2=\frac{C_H}{C_H+C_P} \tag{4-5}$$

Eq. 3 implies the offset error cannot be fully cancelled and a doubled DC gain would be required to achieve the same precision as the half-delay S/H architecture.

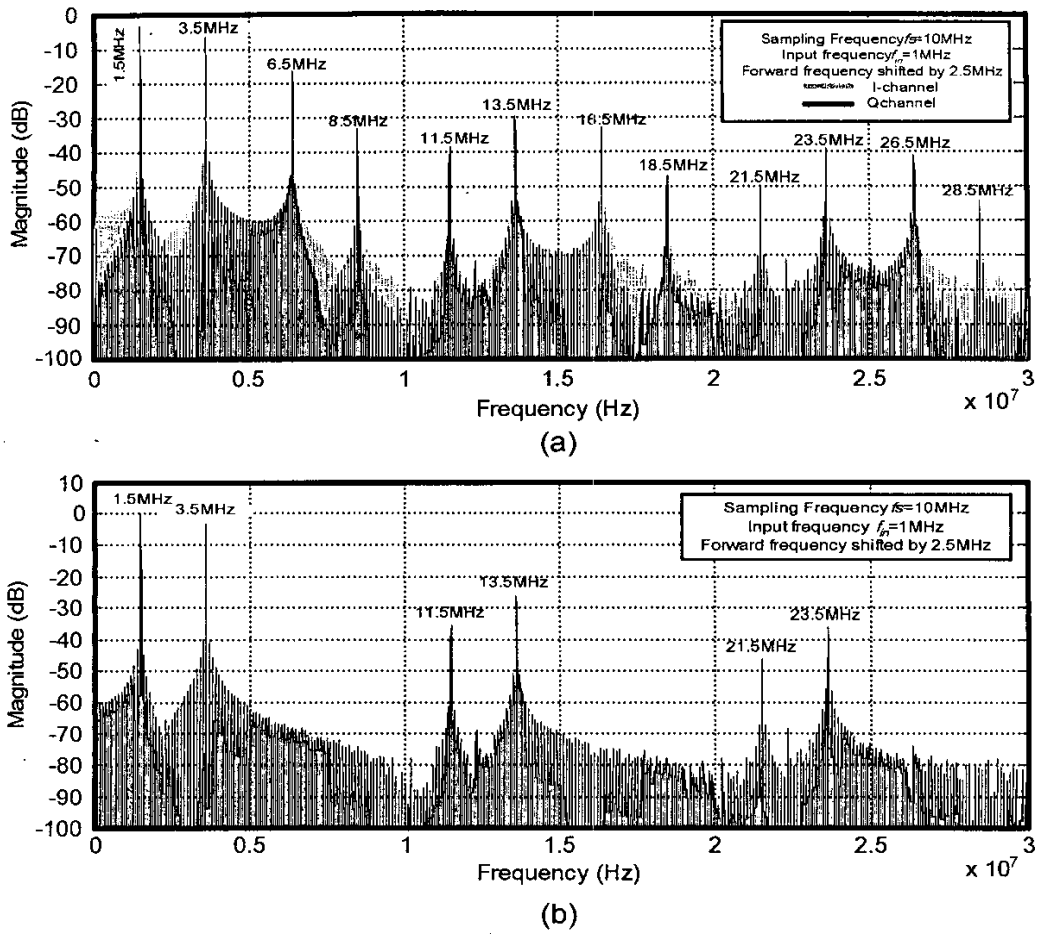

Figure 6: PSD of the A-DQS S/Hs outputs (a) I and Q channels (b) Complex response $|I+jQ|$.

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