A 10.7-MHz Bandpass Sigma-Delta Modulator Using Double-Delay Single-opamp SC Resonator with Double-Sampling

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ABSTRACT

The design of a 10.7-MHz 4th-order fs/4 bandpass sigma-delta modulator with a double-delay single-opamp resonator plus double-sampling technique is proposed for GSM standard. The circuit is implemented in 0.35- μ m double-poly, triple-metal CMOS process. Both behavioral-level and transistor-level simulation results are presented, and the circuit is expected to achieve >80 dB dynamic range, occupying 0.15 mm^2 active area and less than 12mW power consumption at 2.5V supply.

1. INTRODUCTION

Sigma-delta A/D converters provide higher resolution for narrowband (e.g., <200kHz) signals in traditional superheterodyne receiver baseband. However, this traditional receiver structure suffers from the analog non-idealities such as I/Q path mismatch and low-frequency flicker noise. A bandpass sigma-delta A/D converter, as shown in Fig.1, can perform digitization at the superheterodyne receiver IF stage avoiding those non-idealities. Furthermore, with channel-select filtering in digital domain, there would be several advantages associated, such as, the ease of programming channel-select filtering, increasing multi-standard adaptability, with the reduction of the cost in terms of area and power consumption due to the shrinking of the dimensions and the decrease of the supply, for digital CMOS technologies.

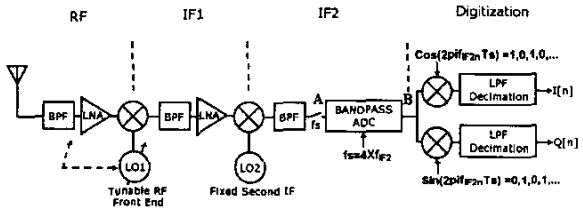

Figure 1 Superheterodyne receiver with IF digitization

Recently, several proposed bandpass sigma-delta modulators (SDM) are constructed with single-opamp resonator structures such as double-delay type[1], Pseudo-N-Path (PNP) type [2] and double-sampling PNP[3]. However, in [2] and [3] since the power consumption is directly proportional to the output swing this means that it can be reduced only by voltage supply reduction. In [1], although the modulator structure is more suitable for lower supply voltage, it operates with single-sampling scheme, so that half of the sampling period is idle. Therefore, to further relax the active element speed requirements and consequently the power consumption, this paper proposes a new modulator with double-delay single-opamp resonator structure which embeds also the double-sampling technique.

The proposed modulator is designed with a top-down design approach that comprises the use of the following: MATLAB programming and SIMULINK behavior simulations with non-idealities model, used for defining a valid building block specifications; SWITCAP2 for circuit verification; Cadence Spectre for the transistor- and layout-level simulations. The SDM architecture and its circuit implementation together with all the simulation results and circuit layout will be presented next.

2. SDM ARCHITECTURE

Fig. 2 shows the block diagram of a reference bandpass SDM [1]. The signal transfer function (STF) and noise transfer function (NTF) of the system are given by:

$$STF = \frac{Y(z)}{X(z)} = -\frac{z^{-2}}{(1+(2-F1B1F2-B2F2)z^{-2}+(1-B2F2)z^{-4})} \quad (1-a)$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{(1+z^{-2})^2}{(1+(2-F1B1F2-B2F2)z^{-2}+(1-B2F2)z^{-4})} \quad (1-b)$$

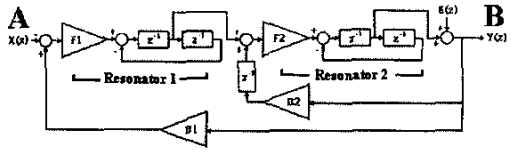

Figure 2 Block Diagram of a bandpass SDM

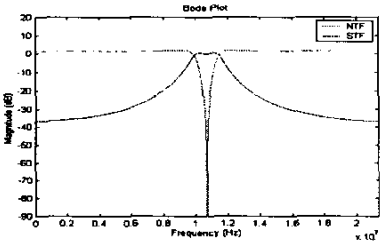

Figure 3 Bode plot of STF and NTF

Since the resonator output swing in Y(z) needs to be scaled down to accommodate the low supply voltage, the resonator gains are set as F1=0.2 and F2=0.25. The Bode plots of STF and NTF are shown in Fig. 3 considering that the desired signal information (fs/4±100kHz) will pass through and the quantization noise will be shaped in the desired signal band. However, due to the decrease of the resonator gain, the STF and NTF's poles start to move from the center of the unit circle toward the center frequency (fs/4), and the

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resulting degradation in noise shaping performance must be taken into account in the design.

3. CIRCUIT DESCRIPTION

In general, a bandpass SDM can be used to perform narrow band IF-digitization. However, when its sampling frequency becomes higher, circuit non-idealities will affect the modulator performance. Also, the saturation voltage of the opamps will affect the modulator performance since the resonator output is several times higher than the input voltage. The proposed modulator operates properly in lower supply voltage applications due to the freedom of the stage gain setting, and especially because it performs a nth-order noise transfer function by using n/2 opamps.

3.1 Resonator Structure

The proposed resonator, as shown in Fig.4, presents a double-delay single-opamp resonator structure with the corresponding clock phases. The need of only one opamp certainly reduces the power consumption. In addition, double-sampling technique is an efficient way to increase the oversampling ratio (OSR) by a factor of two in a modulator without increasing the clock rate, thus relaxing the opamp settling time. Furthermore, unlike the resonator proposed in [2],[3], this modulator is constructed by a resonator, which can scale its output swing without increasing the capacitive loading of the opamp. The feedback capacitors are never connected to the opamp output, which allows free output swing scaling without any power consumption penalty. The operation of the proposed resonator and modulator will be explained in more detail next.

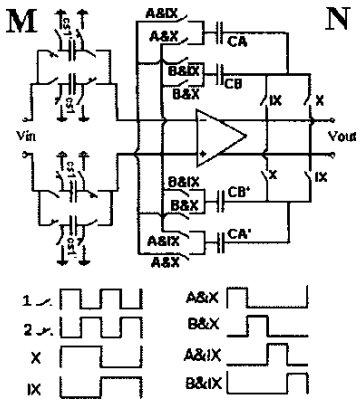


Figure 4 The proposed resonator structure

The proposed resonator is an enhanced version of the one presented in [1] with the use of the double-sampling technique. The capacitors sets (Cs1, Cs1') and (CA, CB, CA', CB') will be represented in the following equations, by the sampling capacitor (Cs) and the storage capacitor (Ch), respectively. There is a total of eight clock phases (1, 2, X, IX, A&X, B&X, A&IX, B&IX) needed for the resonator operation.

The operation can be summarized as follows: the proposed resonator operates in the A&B path for double sampling and performing time-interleaved integration. The phases X&IX control the inversion of the negative feedback path for each clock cycle. In more detail, after sampling the input voltage by Cs1 (or Cs1'), the charge will be transferred in the next clock phase 1 (or 2) to the storage capacitor, which already has stored the previous output voltage charge. This operation will be repeated at the next clock cycle except the inversion of the storage capacitor pairs (CA, CB) and (CA',CB') for performing the negative feedback. Then, it is possible to get the following time difference equation:

$$Cs\times -Vin[n-1]-(Ch\times -Vout[n-2])=Ch\times -Vout[n] \qquad (2)$$

and the transfer function of the resonator will be:

$$\frac{Vout(z)}{Vin(z)}=\frac{Cs}{Ch}\frac{z^{-1}}{1+z^{-2}} \qquad (3)$$

From the above equation, the resonator gain is the ratio between Cs and Ch, which can be used for scaling down the output swing, accommodating also the low supply voltage.

Although the double-sampling resonator relaxes the opamp settling time and doubles the operating speed, it suffers from the mismatch errors resulted from the clock phase timing-skew and path mismatch, which can damage the performance of the communication channel due to the appearance of a mirror signal.

3.2 Overall Bandpass Sigma-Delta Modulator

Fig. 5 shows the complete circuit of the proposed double-sampling Bandpass SDM including two comparators at each clock phase (clock 1,2). The modulator feedback directly connects to the sample capacitor in order to reduce switch thermal noise and chip size. The modulator feedback digital-to-analog converter (DAC) and its outputs can be described by:

$$Vp1[n]=Vout1[n+1]=-Vn1[n] \qquad (4-a)$$

$$Vp1d[n]=Vout1[n+2]=-Vn1d[n] \qquad (4-b)$$

$$Vp2[n]=Vout2[n+1]=-Vn2[n] \qquad (4-c)$$

$$Vp2d[n]=Vout2[n+2]=-Vn2d[n] \qquad (4-d)$$

The modulator output will be given by:

$$Vout=\left(1+\left(2-\frac{Cs2}{Ch2}\frac{Cs1}{Ch1}-\frac{Cs2}{Ch2}\right)z^{-2}+\left(1-\frac{Cs2}{Ch2}\right)z^{-4}\right)^{-1}\times \left(-\frac{Cs2}{Ch2}\frac{Cs1}{Ch1}z^{-2}Vin(z)+(1+z^{-2})^2E(z)\right) \qquad (5)$$

Comparing with in the block diagram of Fig. 2, we can obtain:

$$F1=\frac{Ch1}{Cs1},\quad F2=\frac{Ch2}{Cs2},\quad B1=1,\quad B2=1$$

The two resonator gains are F1 and F2, respectively. The feedback gain is equal to the unity.

4. BUILDING BLOCKS SPECIFICATION

The design building block specifications are obtained by using MATLAB programming and SIMULINK behavioral simulations with a comprehensive non-idealities modeling [4]. The modeled non-idealities for this bandpass modulator includes opamp DC gain, SR and GBW, random clock-jitter and periodic timing-skew, noise analysis, and capacitor mismatch. The final required specifications are presented in Table. 1.

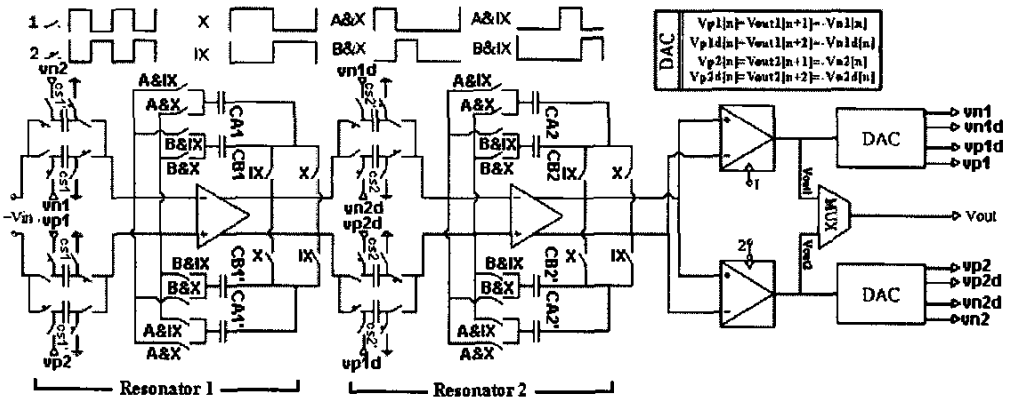


Figure 5 Proposed Band-Pass Sigma-delta Modulator

Specification			
Centre Frequency		10.7MHz	
Bandwidth		200kHz	
Sampling Frequency		42.8MHz	
Clock Frequency		21.4MHz	
Circuit parameter			
F1	0.2	Cs1	0.5 pF
F2	0.25	Ch1	2.5 pF
B1	1	Cs2	0.5 pF
B2	1	Ch2	2.0 pF
Non-idealities			
Dc Gain	90 dB	Jitter	<=0.1 %
Cin	0.288 pF	Time-Skew	<=0.1 %
GBW	220 MHz	Sat. Voltage	1.2 V
SR	280V/μs	Cap.Mismatch	<=0.1%
Cs thermal Noise	Cs=0.5 pF	Opamp Noise	<= -80dB
Performance			
Peak SNR		79 dB	
DR		83 dB	

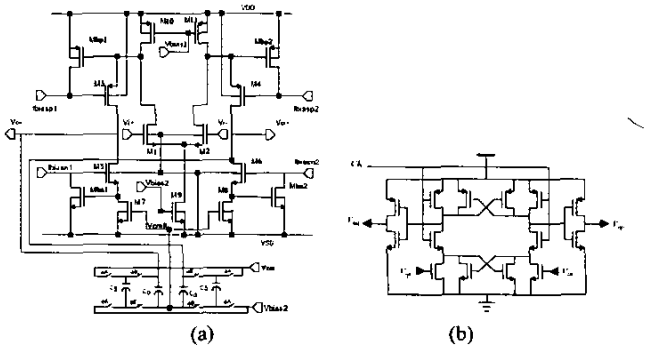
Table.1 Design Specifications obtained from behavior simulation with appropriate modeling

5. IC IMPLEMENTATION

The proposed 4th-order bandpass SDM is implemented in a 0.35 μ m double-poly, triple-metal CMOS process.

5.1 Circuit Structure

In order to meet the high-resolution specification from Table 1, a fully differential Gain Boosted Folded-Cascode OTA [5] with SC common-mode feedback (CMFB) circuit is designed, as shown in Fig 6(a). The Gain-boosted stage increases the DC gain up to 92 dB from the original 40 dB in basic cascode configuration. The input referred noise results mainly from the nmos input stage, and the noisy loads in the nmos and pmos bias current sources. The simulated performances of the opamps are presented in Table. 2.



(a) (b)

Figure 6 (a) Gain Boosted Folded Cascode OTA (b) Class AB comparator

Parameters	Resonator 1	Resonator 2
DC gain (open loop Gain)	92.7 dB	94.7dB
Phase Margin	63.9 Deg	60.6 Deg
Settling Time (closed loop)	12.8ns	14.5ns
Power Consumption	6.93 mW	4.25mW
Slew rate	345 V/us	305V/us
Unity gain frequency	246 MHz	222MHz
In-band Input referred noise	5.8 nVrms	10.9 nVrms
Capacitor Load	3.1p F	2.1p F

Table. 2 Simulated performance results of the operational amplifiers

In the SDM, the performance of the comparator is not critical, two 1-bit fully differential class AB comparators, in Fig. 6(b), will be used here, operating at each non-overlapping clock phase with the corresponding latched output feedback data.

The block diagram of the clock generator is shown in Fig.7. The non-overlapping phase generator implements a bottom-plate sampling to eliminate signal-dependent charge injection distortion. Other clocks are generated by the multi-phase encoding logic part. Moreover, falling-edge synchronization buffers are used in phase A and B to minimize the timing-mismatch errors during the input

IF sampling which will result in undesired inband image tone. The accumulated propagation gate delays for all interleaved phases are also balanced by a careful logic design.

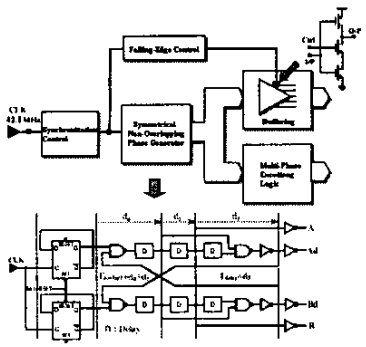


Figure 7 Clock Generator Block Diagram

5.2 Layout

The input stage of the opamp must be carefully implemented to optimize its performance. Symmetrical splitting transistors and dummy transistors are used in the input pair. The common-centroid geometry is adopted in the biasing of the input stage. Other parts are laid out with symmetrical-mirror arrangements.

In order to minimize the errors due to the gradient of the oxide thickness, interspersing the unit-sized capacitors with a common-centroid layout is needed. The proposed bandpass SDM is not sensitive to the resonator gain. However, as it is a time-interleaved structure, the capacitors mismatch between two paths will cause the transfer function mismatch and create inband image signal. As a result, the sampling capacitors and the hold capacitors will have their own common-centroid structure, respectively. The overall layout is shown in Fig. 8 with an active core area about 0.15mm^2.

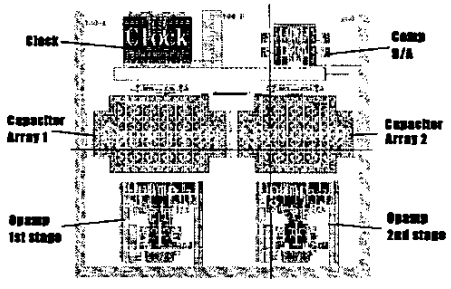


Figure 8 The proposed BPSDM layout

6. SIMULATION RESULTS

The SNR vs. input signal level obtained from MATLAB and SWITCAP2 is presented in Fig. 9. The simulation is based on the opamps specifications, shown in Table. 2. The expected dynamic range is greater than the required 80 dB, which fulfills the GSM standard. The drop of SNR when the input signal is near the middle of full scale is due to the quantization noise which is not well randomized. This drop will disappear by adding a testing dithering signal tone. The output PSD of the transistor-level simulation by Spectre is also shown in Fig. 10.

7. CONCLUSIONS

This paper has proposed a 10.7-MHz 4th-order fs/4 bandpass sigma-delta modulator with a double-delay single-opamp resonator. This modulator benefits from the double-sampling technique and has adjustable gain in the resonator. The circuit is implemented in a 0.35- μ m double-poly, triple-metal CMOS process with 2.5V supply voltage. The building-block of modulator specifications are optimized by dedicated system-level behavior modeling simulations. This bandpass SDM achieves a simulated dynamic range greater than 80 dB and occupies 0.15 mm^2 active area consuming less than 12mW at 2.5V supply.

8. REFERENCE

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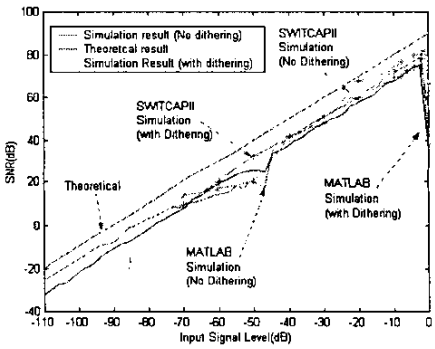

Figure 9 SNR vs input signal level

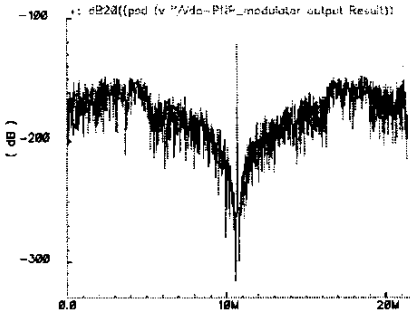

Figure 10 Output PSD with –6 dB input signal level from transistor-level simulation