# MISMATCH-INSENSITIVE N-PATH MULTIRATE SIGMA-DELTA MODULATOR FOR HIGH-FREQUENCY APPLICATIONS

Fan Lou', Seng-Pan U', R.P. Martins'

- 1 Faculty of Science and Technology, University of Macau, P.O.Box 3001, Macao SAR, China (Email: m946312@umac.mo, benspu@umac.mo)
- 1'- Faculty of Science and Technology, University of Macau, P.O.Box 3001, Macao SAR, China (on leave from Instituto Superior Técnico, Portugal, Email: rmartins@umae.mo)

#### ABSTRACT

An N-path multirate Sigma-Delta Modulator (SDM) was recently proposed where the first integrator was implemented using an N-path architecture and a comb filter. The replacement of the first integrator in the N-path structure and the comb filter can relax the speed requirements of the opamps in the first stage and alleviate various mismatch effects. An improved structure for the comb filter is proposed here which eliminates thoroughly the mismatch effects between paths. Analysis and simulations also show that the proposed structure makes the N-path multirate SDM more stable and mismatch insensitive.

#### 1. INTRODUCTION

One of the limitations for implementing SDM in highfrequency is the internal clock rate and the op-amp bandwidth. In order to obtain resolution equivalent to 8-bit PCM for the video signal, the sampling rate has to be over 200MHz which increases the difficulty of design of an active filter for operation at such high frequency. A new type of SDM, called N-path multirate SDM was proposed [1] where the first integrator is implemented by an N-path architecture combined with a comb filter. Figure 1 shows the linear model of the Npath multirate SDM. The first stage operates at low sampling rate and the second remains at higher sampling rate. By using N-path integrator, it can eliminate the aliasing caused by sample rate conversion due to its perfect reconstruction nature. However, even as all N-path filters, this N-path integrator is subject to the mismatch effects between the N paths. The effect of coefficient mismatch on the performance of a block digital filter as presented in [2] shows that due to mismatches, the overall structure becomes time-varying and hence aliasing will be present. It was also emphasized that those portions of the spectrum around  $2\pi i/N$  (i = 1, 2, ..., N) would be folded back into the baseband. In N-path filter version, the aliased components A(z) can be described as,

$$A(z) = \frac{1}{N} \sum_{i=1}^{N-1} X(zW^{i}) \sum_{j=0}^{N-1} z^{-(N-1-j)} \sum_{k=0}^{M_{j}-1} a_{jk} h_{jk} z^{-k}$$
 (1)

where  $M_j$  is the order of each FIR term in a sub-filter  $H_j(z)$ ,  $a_{jk}$ 's are the mismatch ratios and  $h_{jk}$ 's are the ideal coefficients.

In other words, aliased components of the input spectrum X(zW') which will first get multiplied by the terms originated by the mismatch ratios and the ideal coefficients are then folded back into the baseband.

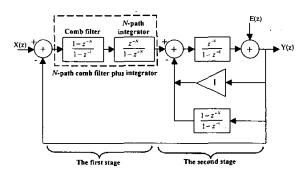


Fig. 1 N-path multirate second-order sigma-delta modulator

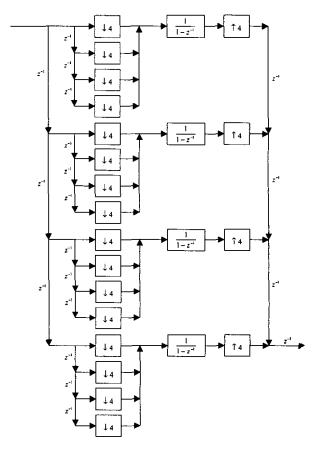


Fig. 2 N-path comb filter plus integrator with N=4

As it is known, the comb filter is a good solution to eliminate the major aliased components by placing the zeros on  $2\pi i/N$ . Therefore, a comb filter is applied prior to the N-path integrator to cancel the re-sample effect and to alleviate the mismatch effects on the N-path integrator.

By carefully analyzing the model in Figure 1, the output of the modulator can be described as.

$$Y(z) = \frac{z^{-1}}{1-z^{-1}} \cdot \left\{ \frac{1-z^{-N}}{1-z^{-1}} \cdot \frac{z^{-N}}{1-z^{-N}} \cdot [X(z) - Y(z)] - \left[1 + \frac{1-z^{-N}}{1-z^{-1}}\right] \cdot Y(z) \right\} + E(z)$$

that will lead finally to,

$$Y(z) = z^{-(N+1)}X(z) + (1-z^{-1})^2 E(z)$$
(3)

which is a typical transfer function of a second-order SDM. However, its first stage is operating at low sampling rate so as to relax the design requirements and reduce the power consumption, which means that the use of CMOS op-amp applied in here becomes possible. Because the performance of second-order SDM depends more critically on the first integrator, keeping the second integrator at a high sampling rate doesn't affect the performance but can simplify the circuit.

In order to lower the sampling rate for the comb filter, this can be combined into the N-path integrator, as shown in Figure 2. Because all summation and integration are done among downsamplers and upsamplers, this combined structure, N-path comb filter plus-integrator, will operate at low sampling rate

However, although the comb filter can eliminate the mismatch effects on the N-path integrator, it suffers from its own coefficient mismatch effects. For example, in the N-path comb filter plus integrator, the transfer function can be described by,

$$H(z) = \frac{1 - z^{-N}}{1 - z^{-1}} \cdot \frac{z^{-N}}{1 - z^{-N}} \tag{4}$$

where the first factor is the transfer function of the comb filter and the second is of the N-path integrator.

Ideally, the N zeros of the comb filter can exactly cancel out the N-path integrator's N poles located on the unit circle. When coefficient mismatch occurs between branches of the comb filter in Figure 2, its N zeros will dislocate away from their original positions and can not cancel the N-path integrator's N poles. This causes the SDM unstable and the Signal-to-Noise Ratio (SNR) greatly dropping down which is schematically represented in Figure 3, where the comb filter's branches mismatch affects the performance of the SDM.

In order to overcome this shortcoming, a new architecture is developed that uses a cascade form in the comb decimation filter instead of a parallel direct form. In the following analysis and simulations, it will be demonstrated that the coefficient mismatch on the cascade comb decimation filter can be represented as path gain error and eventually eliminated by the comb filter itself.

## 2. IMPROVED SYSTEM ARCHITECTURE

#### 2.1. The cascade comb decimation filter

The cascade comb decimation filter mentioned before as shown in Figure 4, and its transfer function can be expressed as,

$$H(z) = \prod_{i=0}^{(\log_2 N) - 1} (1 + z^{-2^i}) = \frac{1 - z^{-N}}{1 - z^{-1}}$$
 (5)

where N is a power of 2.

In this structure, the coefficient mismatch ratios of the different blocks,  $\alpha_i$ , will be multiplied together and the result will represent the gain error of the comb filter,

$$H(z) = \prod_{i=0}^{(\log_2 N) - 1} \alpha_i (1 + z^{-2^i}) = \alpha \cdot \frac{1 - z^{-N}}{1 - z^{-1}} , \quad \alpha = \prod_{i=0}^{(\log_2 N) - 1} \alpha_i$$
(6)

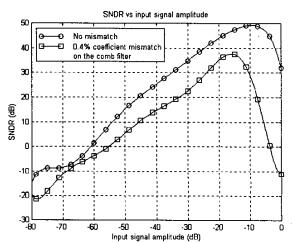


Fig.3 SNDR drops due to coefficient mismatch on the direct form comb filter

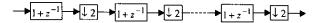


Fig.4 Cascade comb decimation filter

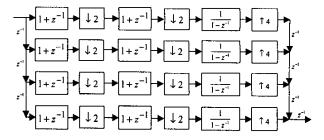


Fig. 5 Improved N-path comb filter plus integrator by using cascade comb decimation filter, N=4

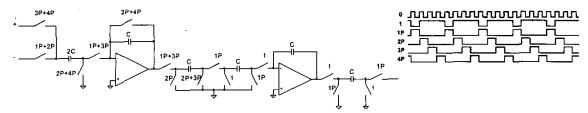


Fig. 6 One path of the improved 4-path comb-filter plus integrator

#### 2.2. Improved N-path comb filter plus integrator

Figure 5 shows the combined architecture of the improved structure where cascade comb decimation filters replace direct form comb filters.

The coefficient mismatch on the cascade comb decimation filter can be represented as a gain error, which implies that for the overall structure of Figure 5, the gain errors of the comb filter in each path can be considered as the path mismatch of the N-path integrator. Eventually, these mismatch ratios will be eliminated by the comb filter itself.

## 2.3. N-path comb-filter plus integrator circuit

Figure 6 shows the SC realization of one path of the 4-path comb filter plus integrator with the use of cascade comb decimation filter.

Compared with the case of direct form, this improved N-path comb filter plus integrator not only reduces the number of the clock phases, but also the switched-capacitor elements. Furthermore, the double-sampling circuits used in original structure [1] are all abandoned to prevent the influence of the nonuniform sampling and path gain error [3].

This circuit, however, presents a drawback related with the increment of the amount of opamps in each path and also the introduction of parasitic effects similar to a gain error from the charge transfer process between the two opamps.

# 3. DESIGN EXAMPLE FOR VIDEO APPLICATIONS

In accordance with the specifications given in CCIR-601 which describes studio digital video coding, the chrominance signals  $(C_r)$  and  $C_b$  are sampled at a frequency of 6.75MHz (3MHz  $\times$  2.25) and are coded with 8-bit PCM words. Herein, we choose oversampling rate (OSR) of 36 (3MHz  $\times$  2.25  $\times$  32 = 216MHz) because 32 is a power of 2, for simplification of the decimator. Theoretically, if OSR = 36, it will give a maximum of 70dB SNR, equivalent to 11.5-bit PCM words.

A fully differential balanced circuit for the 4-path multirate second-order SDM has been designed and its behavioral simulation is demonstrated by using SWITCAP2 [4-6].

## 4. SIMULATION RESULTS

Figure 7 shows the Signal to Noise plus Distortion Ratio (SNDR) of the improved 4-path multirate second-order SDM compared with the conventional second-order SDM and the original 4-path multirate SDM, where the curves were obtained by simulation with Matlab [7], and if the OSR of the conventional second-order SDM is 36, a good matching can be

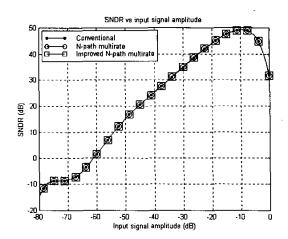


Fig. 7 SNDR comparison of models without coefficient mismatch

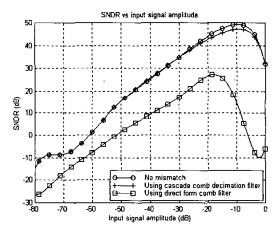


Fig. 8 0.4% coefficient mismatch on the whole Npath comb filter plus integrator

observed. Figure 7 also indicates that the peak SNDR for N-path multirate SDM is 50dB (equivalent to 8-bit PCM).

Figure 8 shows the comparison of the improved model and original model when mismatch exists on the whole N-path comb filter plus integrator. It is clear that by using the cascade comb decimation filter the improved N-path multirate SDM has excellent performance in terms of mismatch insensitivity.

The output spectrum of the circuits for the proposed SDM and the original N-path multirate SDM are compared in Figure 9 with -10dB input amplitude and with 0.4% coefficient

mismatch effects on the whole N-path comb filter plus integrator.

When mismatch exists on the N-path comb filter plus integrator, the aliasing causes a raise of the noise floor in the baseband, as shown in Figure 9. Moreover, multirate SDM tends to generate limit cycles at frequencies of f<sub>s</sub>/2N±if<sub>in</sub> where fin is the input frequency. Due to mismatch, these limit cycles will also fold back into the baseband and cause tones at ifin as if they were harmonics of the input frequency  $f_{\rm in}$ . Note that these tones are originated from the time-varying nature of the structure rather than its nonlinearity [8]. When a comb filter is applied, because of the existence of notches at f/2N, the noise floor in the baseband will have apparent improvement since the effect of the aliased component is negligible, as well as, the tones at ifin. However, in addition, due to the fact that the coefficient mismatch effects occur on the comb filter itself, the notches can not locate exactly at  $f_s/2N$  and therefore it can not efficiently remove the aliased components and limit cycle

With the use of cascade comb decimation filter, the coefficient mismatches on the comb filter will be transferred to the path mismatch of the N-path integrator and will be neutralized by the comb filter itself. Hence, the improved N-path multirate SDM becomes mismatch-insensitive.

In order to illustrate the mismatch effects, Monte Carlo simulation for 200 samples has been performed on the proposed SDM. Typically, the mismatch ratio for capacitors can be controlled within 0.4%. Herein, supposing that the mismatch ratio is described by Gaussian Distribution and supposing that the standard deviation  $\sigma$  is equal to 0.2%. Also these mismatch ratios are applied on the whole N-path comb filter plus integrator. Then the simulation results from Figure 10 show that  $\Delta SNDR$  are less than 1.13dB within  $\sigma$ , 3.06dB within  $\sigma$  and 4.83dB within  $\sigma$ , respectively. It clearly indicates that the circuit is mismatch-insensitive.

# 5. CONCLUSIONS

N-path multirate SDM performance has been reviewed in this paper. Furthermore, how the coefficient mismatch on the comb filter affects the performance of the SDM has also been analyzed. An improved architecture is consequently proposed in the paper, obtained by using cascade comb decimation filter, where the coefficient mismatch on the comb filter is transferred to the path mismatch of the N-path integrator. Eventually, these path mismatch effects are contrarily eliminated by the comb filter. In the same way of the original model, the cascade comb decimation filter is also combined with the N-path integrator to allow the comb filter and the integrator to operate at low sampling rate. Furthermore, while retaining all the advantages from the original structure, this improved architecture has given up the need to use doublesampling technique to prevent the influence of the nonuniform sampling and path gain error. A Monte Carlo simulation has verified the efficiency of this improved model with the use of cascade comb decimation filter.

## 6. REFERENCES

[1] Fan Lou, Seng-Pan U, and R.P.Martins, "N-path Multirate Sigma-Delta Modulator for High-Frequency Applications," accepted by IEEE Int. Conference on Electronics, Circuits and Systems, Sep. 2002

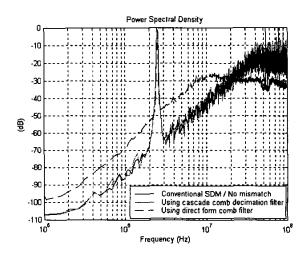


Fig.9 Output spectrums with 0.4% coefficient mismatch on the whole N-path comb filter plus integrator by using cascade comb decimation filter versus direct form of comb filter

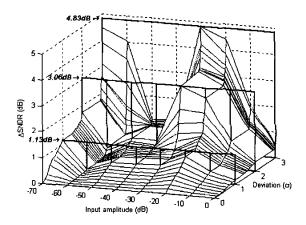


Fig. 10 Monte Carlo simulation shows  $\Delta SNDR$  within different deviation  $\sigma$ ,  $2\sigma$  and  $3\sigma$ , where  $\sigma$ =0.2%

- [2] R.Khoini-Poorfard, and D.A.Johns, "Mismatch effects in time-interleaved oversampling converters" *IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. 429-432, 1994
- [3] J.J.F.Rijns, and H.Wallinga, "Spectral Analysis of Double-Sampling Switched-Capacitor Filters," *IEEE Trans. Circuits and Systems*, vol. 38, no. 11, pp. 1269-1279, Nov. 1991
- [4] S.C.Fang, Y.P.Tsividis, and O.Wing, "SWITCAP: A switched-capacitor network analysis program. Part I: basic features" *IEEE Circutis Systems Magazine*, vol. 5, no. 3, pp. 4-10, Sep. 1983
- [5] S.C.Fang, Y.P.Tsividis, and O.Wing, "SWITCAP: A switched-capacitor network analysis program. Part II: advanced features" *IEEE Circuits Systems Magazine*, vol. 5, no. 4, pp. 41-46, Dec. 1983
- [6] K.Suyama, S.C.Fang, and Y.P.Tsividis, "Simulation of mixed switched-capacitor/digital networks with signal-driven switches" *IEEE J. Solid-State Circuits*, vol. SC-25, no. 6, pp. 1403-1413, Dec. 1990
- [7] MATLAB, Optimization Toolbox User's Guide Version 5, MathWorks, Inc., May 1997.
- [8] R.Khoini-Poorfard, L.B.Lim, and D.A.Johns, "Time-interleaved oversampling A/D converters: theory and practice" *IEEE Trans. Circuits and Systems*, vol. 44, no. 8, pp. 634-645, Aug. 1997