Design Considerations of SC Analogue Multirate Filters with Multistage Implementation

Cheong Ngai [1], Rui P. Martins [2]

1- Computer Studies Program,
Macau Polytechnic Institute
Rua de Lu Gonzaga Gomes, Macau, China
E-mail-ncheong@umac.mo

2- Faculty of Science and Technology,
University of Macau
P.O.Box 3001, Macau, China
E-mail-rtorpm@umac.mo (on leave from IST, Portugal)

Design of multirate filters with multistage implementation are well-known method in digital system [1]. Hence, the goal is both the minimization of computation rate and reduction in storage requirements. In the implementation of the digital filter, the multistage structures can significantly reduced computation to implement the system, reduced storage, simplified filter design. The methodology also has been developed in analogue circuits. However, it has the lack of design procedure to implement a circuit properly and clearly. This paper will discuss the considerations involved in the design of multistage decimator and interpolator systems, including the choice of the number of stages I, the decimation or interpolation ratios M_i or L_i at each stage, the filter requirements, corresponding circuit topology and the actual filter designs at each stage.

The concept of using single stage to implement a sampling rate conversion system can be applied to the case decimators, as shown in Fig.1. It will be assumed that a function $H(z)$ has been obtained, which meets give desired performance speciications and that a SC decimator is to be synthesised to realise.

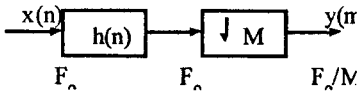

Fig. 1 Single Rate Single Stage Implementation of a SC Analogue Decimator.

There are two alternation menthods of designing multirate circuit, named as directly (single stage and multirate) [2][3] and indirectly (multirate and multistage) [4]. For a directly method, the multirate SC implementations of sampling rate conversion is based on the prototype filter specification, shown as Fig. 2. The decimator order should be the same as the prototype's.

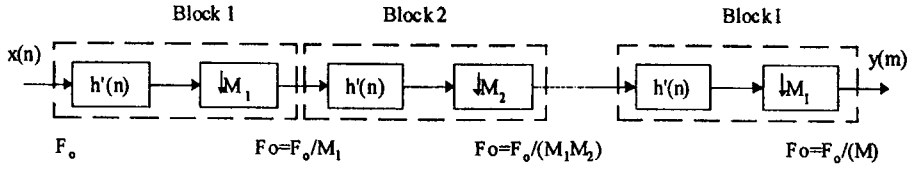

Fig. 2 Multirate and Single Stage implementation of SC Analogue Decimator.

For the indirectly method, designers need to determine the number of stage and corresponding order at each stage shown as Fig. 3. The order of a decimator only concerns with the selected stage and decimating factors. It means the decimator order may be greater than prototype, and for the single stage implementation, the overall z-transfer function of the prototype filter that meets the specified baseband and anti-aliasing filtering characteristics, separately

For a prototype of z transfer function H(z),

$$H(z)=k\prod_{i=1}^{D}\frac{(1-2r_{oi}\cos(\theta_{oi})z^{-1}+r_{oi}^{2}z^{-2})}{(1-2r_{pi}\cos(\theta_{pi})z^{-1}+r_{pi}^{2}z^{-2})} \quad (1)$$

where k is a gain factor, D is numbers of cascade biquads, and modified z-transfer function for multistage implementation with overall decimation factor M can be expressed as

$$\bar{H}(z)=k\prod_{i=1}^{S}\prod_{j=1}^{D_i}\frac{(1-2r_j\cos(\theta_j)z^{-I_j}+r_j^{2}z^{-2I_j})}{(1-2r_j\cos(\theta_j)z^{-T_j}+r_j^{2}z^{-2T_j})} \quad (2)$$

where I gives the sequence of the decimator stages from the input $I=1$ at the stage to the output at this stage $I=S$, S and D_j are the number of stage, number of cascade biquad building block in the I stage, respectively. The normalized delay periods I_j are determined by $T_i=M(F_s/F_i)=\prod_{j=1}^{i}M_j$, the decimation factor M will be a lowest common multiple of a few smaller integer numbers that will been applied in the

multi-structure as a new blocks decimation factor. If the total decimation ratio M can be factored into the product $M = \prod_{i=1}^{S} M_i$, and M_1 , M_2 ,..,M_S respectively, represent the decimation ratio in each stage. It should be apparent that the number of possible topologies and damping types combinations is quit for a large decimating factor M in the decimator.

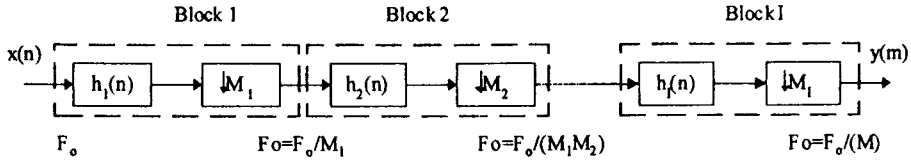

Fig. 3 Multirate and MultiStage implementation of a SC Analogue Decimator.

There are a large number of trade-offs involved in the design of multistage decimator and interpolator systems, including the choice of the number of stages I, the decimation or interpolation ratios M_i or L_i at each stage, the corresponding circuit topology and the sequence of the building blocks in the cascade, the specific sensitivity requirements and the gain distribution strategy, etc. The optimum sequence of the corresponding topology at the building block level synthesis is obtained according to the next design rules: a) Decompose the overall ripple of a filter in different values by ascending order to reduce the decimator order. b) Implement the first stage with the largest multiple decomposed from the decimating factor M and decompose M in prime factors by descending order in order to minimize the speed requirements of the amplifiers.

A simple example is illustrated the procedure of multistage implementation by means design of a 6^{th} order lowpass SC filter , with reduction of the sampling frequency from 10kHz at the input to 1KHz at the output with the maximum passband ripple of 0.15 dB, the cutoff frequency fc=0.1 kHz, and minimum rejection of 75 dB above 0.5 kHz.

After scaling for maximum signal handling capability and normalizing with respect to the unit capacitance values, the decimator presents a and a total area close to 130 capacitor units for the complete circuit, selected from nine different solutions (M_1 M_2 and M_3 in the same damping types and building block topologies). The conclusions are briefly summarized in Table I. From this table it can be observed that, in general, the capacitance reduction potential increases with the order of the transfer functions. It can also be seen that the total capacitance varies with the topologies and damping types selections. For example, almost a 50% reduction in total capacitance was observed for this approximation by using optimal combination.

Table I Comparisions of Some Multistage Implementations of a 6^{th} Lowpass Filter with M=6

Multistage (3 stages)			
M_1	M_2	M_3	Total C
1	6	1	165.96
2	3	1	266.95
3	2	1	164.43
6	1	1	156.76
1	3	2	130.21
3	1	2	218.28
1	2	3	146.87
2	1	3	243.52
1	1	6	148.45

References:

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