Selection Topology of IIR Multirate SC Decimating Filters with Statistical Model

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The design of a multistage and multirate circuit is one of important method that allows designers to designate a SC decimator rapidly and exactly [1]. The properties of multistage implementation are completely determined by the independent building blocks that usually include one of following structures: externally and internally [2], cascaded building block and ladder structure. The recent research efforts have attempted to exploit a given topology library of functional units, which is a process of choosing the types of structural modules from the design library to implement behavioral operations, not only enhances performance, but also saves capacitance area. This paper is to evaluate the performance of three basic SC decimator topologies by means of a compiler ISCMRATE [3]. We consider a design example that refers to an 3rd order lowpass SC decimator, with reduction of the sampling frequency from 10kHz at the input to 2.5Khz at the output. The maximum passband ripple is 0.60 dB up to the cutoff frequency of 0.1 kHz, giving a minimum rejection of 60 dB above 0.5 kHz. The maximum capacitance spread and total capacitor area of the different solutions for designing a SC decimator are briefly summarized in Table I.

Table I Comparison between the Alteration Methodologies for a 3rd Order SC Lowpass Decimating Filter (M=4)

Types	**Externally**						**Internally**	**Ladder**
Damping	E			FD		FB	FD	—
M_1, M_2	1, 4	2, 2	4, 1	4, 1	1, 4	—	2, 2	4
Total-C	134.4298	108.3713	111.7101	100.6294	711.8619	—	37.9355	36.0034
C-Spread	51.0907	53.1716	57.5904	51.0907	425.5310	—	6.0983	7.1218

To retain the specified gain at low sampling frequencies F_s, to reduce the sensitivities and for ease of realization, the decimating factors should be as large as possible. However, the rejection bandwidth for the required suppression of aliasing must be greater than the double cutoff frequency, it may not be very large.

The larger decimating factor can minimize the GBW values of the amplifiers required in a circuit, but the an disadvantage of produing the unwanted band aliasing that becomes even more significant as the decimating factors increases. The nominal frequency response of the SC decimator block will be affected by the decimating factor, as illustrated in Fig.1 (a) (b).

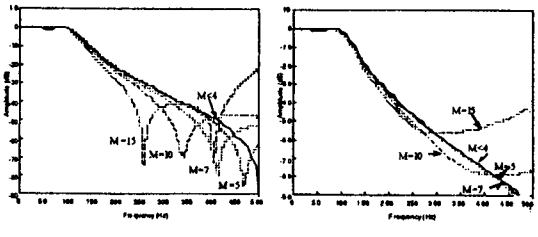

Fig. 1 Computer Simulated Amplitude Response (M=4, 5, 7, 10, and 15) (a) Externally (b) Internally and Ladder.

We can also observe that the frequency response is close to meet the desired specification in the low decimating factor, but its essentially produce umwanted aliasing frequency components, both passband and stopband sensitivities are relatively increase with decimating factors. espescially in the case, the stopband sensitivities (M>7, single rate implementation) are signficantly worese that those for the decimators (M>4, multirate implementation). Under typical non-ideal values of the amplifiers dc gain (from 60 dB to 120 dB), nominal frequency response of the SC decimator is shown, respectively, in Fig. 2 (a) (b) and (c). It is clearly shows that each OA we adopted in transistor level synthesis should have a much larger dc gain (> 80 dB) in order to achieve an expected nominal frequency response.

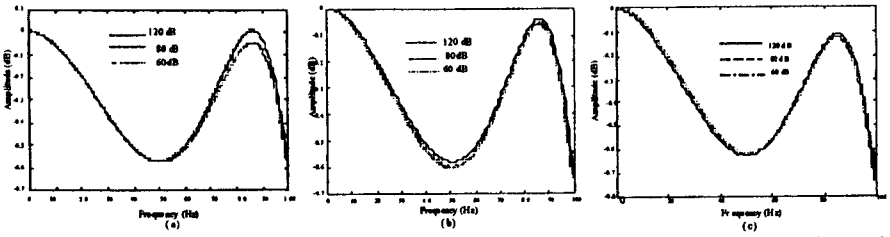

Fig. 2 Computer Simulated Amplitude Response (M=4) (a) Externally (b) Internally (c) Ladder.

The nominal frequency response of the SC decimator can be also be affected by capacitance mismatch errors demonstrated in Fig.3, which shows the passband amplitude response is more affected by variations of the loop capacitors than by variations of input capacitors for all the building blocks. There is a relativity large deviation passband amplitude response in variation of capacitor in cascade biquad blocks compared to the later that exhibit superior sensitivity performance over the former and hence making them attrctive for the reliazation of highly selective filtering responsees.

Based on above analysis results, a statistical model of topology selection is obtained according to the following design criteria: a) The basic building block such as externally and internally cascaded building block, ladder structure may implement a circuit with the different capacitor ratios. To minimize capacitance spread and total capacitor area, an exhaustive investigation is given, when filter order is low, a statistical models of topology should approach, when filter order is very large. In order to minimize contribution to sensitivity in stopband and passband due to cascade sections, the proper design should select a higher order blocks as one stage with ladder or internally cascade structures. b) The optimum topology sequence in multistage implementation should be externally cascaded, internally cascaded, and ladder structure, since decomposing M in prime factors by descending order and the later may be restricted to moderate decimating factors. The decimating factors in each building blocks or stages should not be too large based on the corresponding cutoff frequency Fs, and there are not two or more adjacent structures of internally cascaded using the same damping type (E damping or FB damping).

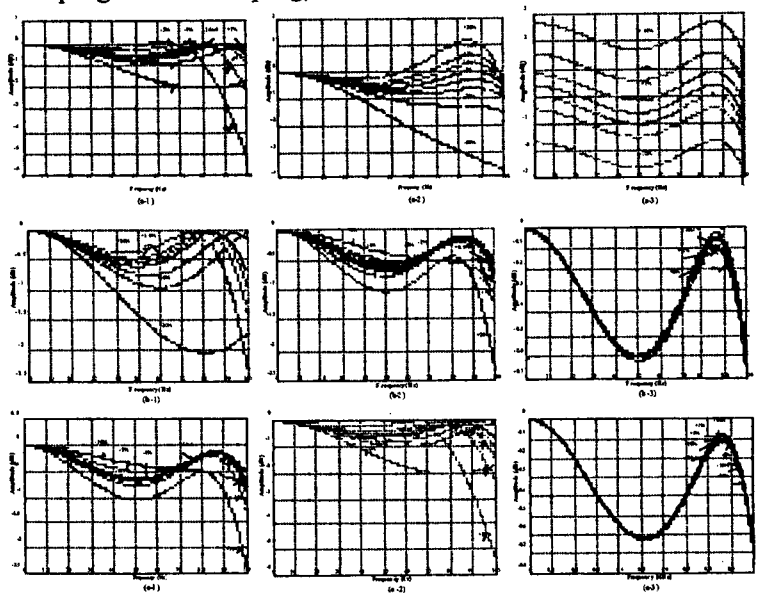

Fig. 3 Computer Simulated Variability of the Amplitude Response in (1) Externally : Variation in (a-1), (a-2) Capacitors in Recursive Loop (a-3) Capacitor in Input Branches. (2) Internally : variation in (b-1), (b-2) Capacitors in Recursive Loop. (b-3) Capacitor in Input Branches. (3) Ladder: Variation in (c-1), (c-2) Capacitors in Recursive Loop.(c-3) Capacitor in Input Branches.

References:

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