

INTERACTIVE SC MULTIRATE COMPILER APPLIED TO MULTISTAGE DECIMATOR DESIGN

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ABSTRACT

This paper proposes an interactive architecture compiler for SC multirate circuits that allows the automated design from frequency specifications to building block implementation, here applied to the design and synthesis of multistage SC decimators. The compiler provides a library of different topologies that comprises a few independent multi-decimation building blocks. New building blocks defined by the users are also available for design of a specific stage. A design example of a 7th order SC decimator illustrates the efficient synthesis of the corresponding resulting circuits that achieve the required anti-aliasing amplitude responses with respect to the speed requirements of the operational amplifiers and also the minimum capacitance spread and total capacitor area.

I. INTRODUCTION

While computer-assisted tools for the design of digital circuits with multirate technique have already attained a considerable degree of maturity, there are fewer tools for the engineers working on the analog portion of the decimator and interpolator chips [1-5]. Here there is an important need to provide designers with computer-aided tools for designing of Switched Capacitor-SC multirate circuits, that usually consist of a program for automatic synthesis of a analogue multirate circuit, making use of the available architectures and techniques to optimize the implementation of a circuit. The compiler should present in its structure the following three major levels of hierarchy: a) System level synthesis; b) Building block level synthesis; c) Simulation (Functional, Electrical) and layout.

The system level synthesis will generate a filter prototype from the frequency specifications. The building block synthesis will allow selection and search of the appropriate interconnection of the different building blocks in order to obtain a specific functionality. The simulation and layout synthesis comprises the simulation of the circuit followed by the layout design that will be determined by an adequate selection of a library of cells including previously designed operational amplifiers-OA's, switches and arrays of capacitors [6]. To implement SC multirate circuits (decimators and/or interpolators), several architectures and techniques were presented since the early 80's. In conventional designs SC decimators were only implemented based on a standard single building block, like ladder structures or cascaded biquad building blocks [7-8]. Those solutions are usually not suitable and flexible for the implementation of a

higher order complex filter with a large decimation factor. In this paper, we present a computer-aided tool designated as *ISCMRATE* (Interactive Switched Capacitor Multirate Compiler) with three levels of synthesis that can be used in the automated design of multirate circuits from the specifications to layout. The compiler architecture presents for multistage decimator design an improved solution that allows the implementation of mixed architectures comprising a library of topologies including different and independent multi-decimation building blocks. New building blocks defined by the users are also available for design of a specific stage [9]. For optimizing IIR SC decimating circuit performance while simultaneously minimizing silicon area, a set of rules are also presented to select the most suitable steps in programming based on a statistical approach.

II. ISCMRATE COMPILER – GENERAL ARCHITECTURE

The general architecture of *ISCMRATE* for the design of SC multirate circuits is schematically presented in Fig. 1.

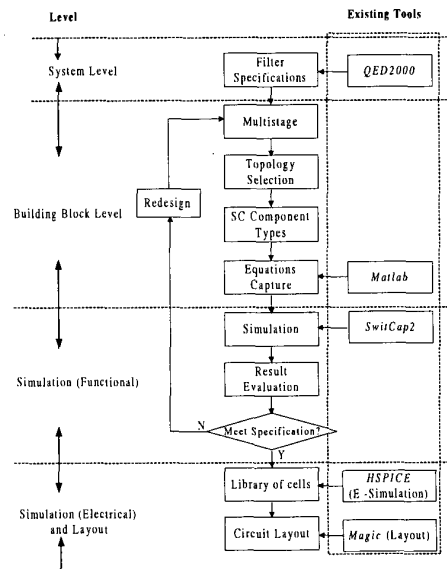


Figure 1. General architecture of the *ISCMRATE* compiler for SC multirate circuits design.

The interactive computer program *ISCMRATE*, which has been developed in around 4500 lines of C++ code and a textual user interface, runs on SUN SPARC workstation. The basic architecture of the program comprehends the system level and the building block level linked to a few existing programs [10-11]. The automated layout generation of the circuit (under development) will allow the selection of the different electronic components (OA's, switches and capacitors) from a library of cells. For the practical feasibility and compatibility of the compiler, the building blocks in each stage are therefore determined independently. The multirate and multistage algorithm of *ISCMRATE* for decimator design is partially shown in Fig. 2. After the selection of a particular topology, a file of component values will be generated for *SWITCAP2*.

```

for (each P in permutations of total decimating factor M )
{
  last_output = terminal;
  for (each stage with decimating factor Mi in P )
  {
    for (each block b with Mi )
    {
      Switch ( block type of b )
      Case externally: build_externally (last_output);
      Case internally: build_internally (last_output);
      Case ladder: build_ladder (last_output);
      Otherwise: new_block: build_new (last_output);
    }
  }
  maximize_dynamic_range ( );
  /* the same output level at each OA's */
  minimize_capacitance_spread ( );
  /* (a) by the capacitances scaling */
  /* (b) by presetting the coupling capacitors */
}

```

Figure 2. *ISCMRATE* - Multirate and multistage independent building blocks algorithm.

III. DESIGN CRITERIA OF MULTIRATE AND MULTISTAGE CIRCUITS AND TOPOLOGY SELECTION

Based on a statistical approach, the optimum decimating factors and ripple, pole-zero assignment of the system level synthesis at the corresponding stages is obtained according to the following design criteria:

- Decompose the overall ripple of a filter in different values by ascending order to reduce the decimator order,
- Implement the first stage with the largest multiple decomposed from the decimating factor M and decompose M in prime factors by descending order in order to minimize the speed requirements of the amplifiers,
- The decimating factors in each building blocks or stages should not be too large (<10), especially in the decimators with internally cascaded or ladder structure.

Then, the optimum sequence of the corresponding topology at the building block level synthesis is obtained according to the next design rules:

- The optimum sequence for organisation of a topology should

include first externally cascaded blocks followed by internally cascaded, and then ladder blocks, since decomposing M in prime factors by descending order implies that the later is restricted to moderate values of the decimating factors,

- Adjacent structures of internally cascaded will not allow two or more blocks with the same damping type (E damping or F damping),

- The selection of preferred circuit topologies is made considering the performance behavior under non-ideal characteristics of the amplifiers, namely the finite dc gain and bandwidth.

IV. AUTOMATED DESIGN EXAMPLE OF A MULTISTAGE DECIMATOR

The performance of the *ISCMRATE* compiler can be illustrated by means of an example of a 7th order lowpass SC filter prototype with input sampling frequency 500 MHz, and decimating factor $M=10$, passband ripple of 0.165 dB, cutoff frequency $f_c=1$ MHz, and minimum rejection of 100 dB above 5 MHz. In order to be possible to implement this prototype filter in CMOS technology, multirate techniques are necessary. Based on these techniques, this prototype can be implemented by means of a multistage decimator. This decimator will reduce the sampling frequency from 500 MHz at the input, to 50 MHz at the output with a multistage implementation. With an overall decimation factor of $M=10$ that can be automatically factored into the product $M=M_1 \cdot M_2$, meaning that only two stages are needed for the implementation of the decimator. The multistage steps followed by the program at the system level synthesis are shown in Fig. 3.

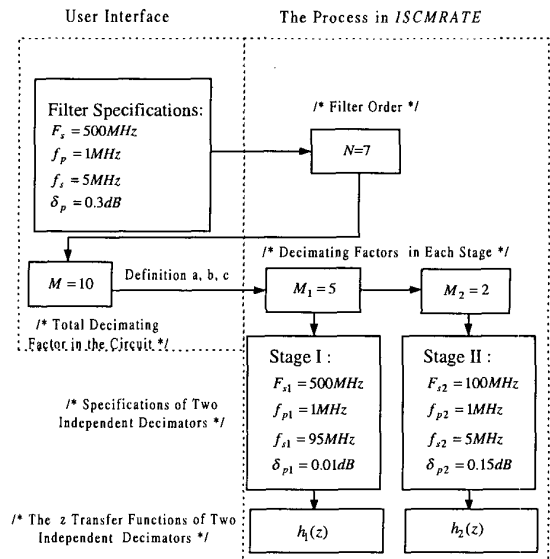


Figure 3. Compiler steps for multistage design decimator at system level in *ISCMRATE*.

The selection by the program of an optimum sequence of topologies allows the determination of an architecture with a 4th order internally cascaded building block with $M_1=5$, followed by a 3rd order ladder structure with $M_2=2$, according to the above design criteria. The corresponding steps at the building block level synthesis are shown in Fig. 4.

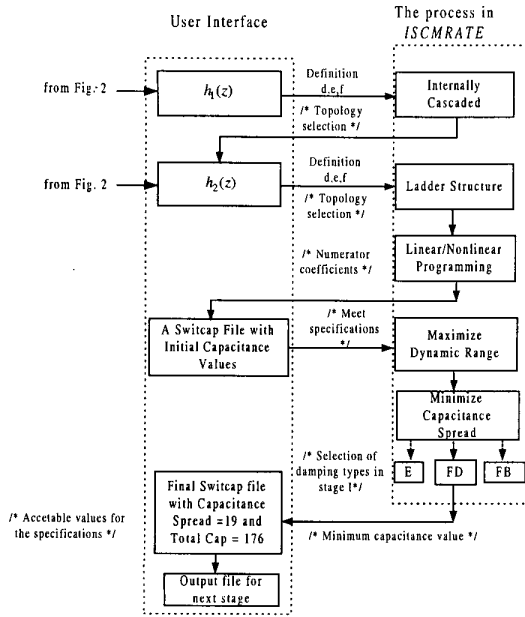


Figure 4. Compiler steps for multistage design decimator at building block level synthesis in ISCMRATE.

After scaling for maximum signal handling capability and normalizing with respect to the unit capacitance values, the decimator presents an acceptable maximum capacitance spread of 19 and a total capacitance area close to 176 capacitor units for the complete circuit, selected from six different solutions (different damping types and building block topologies). The selected overall circuit structure of the SC decimator, automatically designed, is presented in Fig. 5. The compiler enters in simulation and layout synthesis level and generates initially the input file for SWITCAP2, in order to simulate functionally the overall decimators. The nominal passband and overall computer simulated amplitude responses with ideal and finite DC gain amplifiers are shown in Fig. 6 (a), (b) and Fig. 7 (a), (b), respectively. After the functional simulation based on the requirements of the different components, a selection is made from a library of cells (OA's, switches and capacitors) having in consideration the characteristics of each cell (E-simulation and layout). Total automated design in the above case takes around 30 min on a SUN SPARC-5 workstation.

V. CONCLUSIONS

This paper proposes an interactive architecture compiler ISCMRATE applied to the design of multistage IIR SC decimators with large decimating factors. The compiler presents three different levels, namely the system synthesis, the building block selection and simulation and layout. The program allows designers to quickly compute the exact capacitance ratios and realize a predetermined set of design specifications. The example presented shows that the multiple decimating structures can effectively eliminate treacherous aliasing frequency components arising on SC multistage externally cascaded decimating filters and it demonstrates the compiler feasibility and compatibility.

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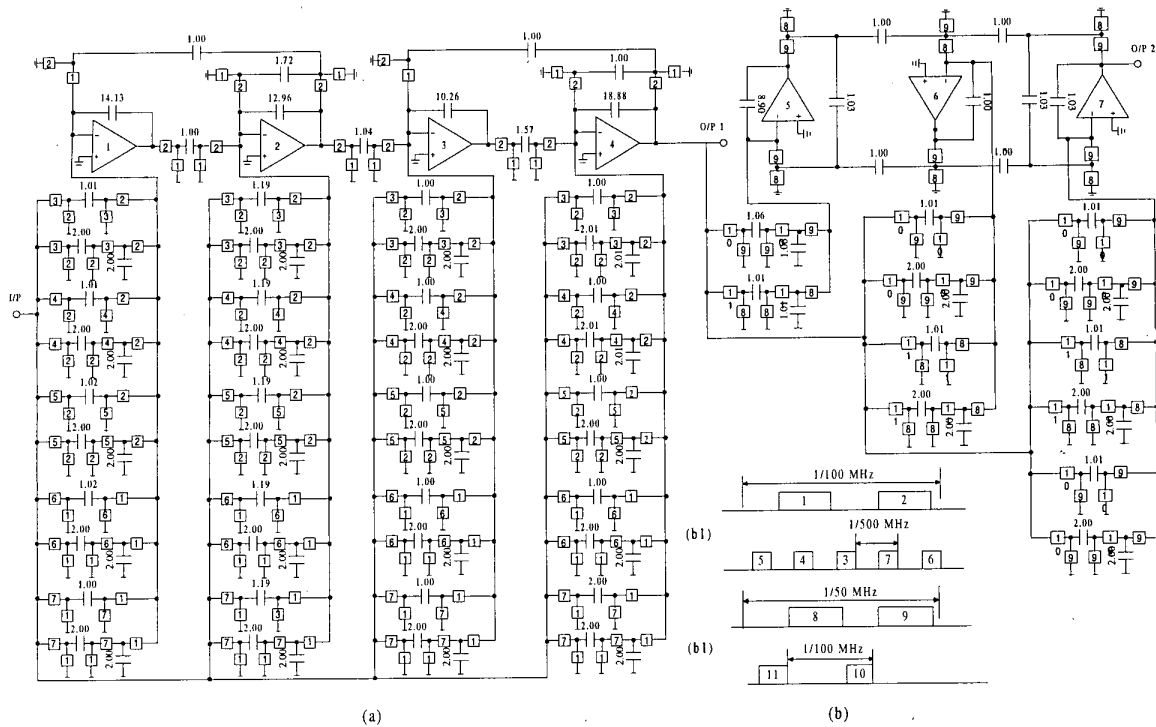


Figure 5. (a) SC circuit. (b) Switching waveforms ((b1) internally cascaded (b2) ladder structure).

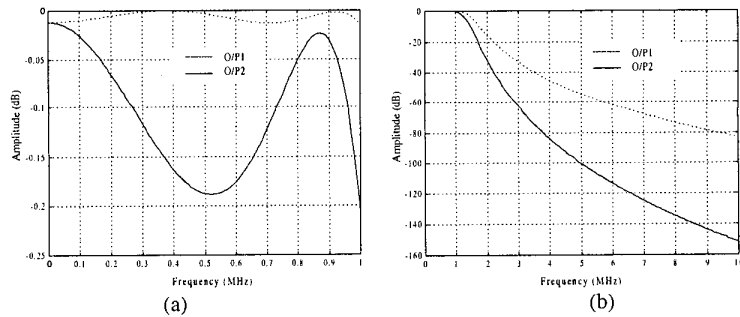


Figure 6. Computer simulated a) passband and b) overall amplitude responses with ideal dc gain amplifiers.

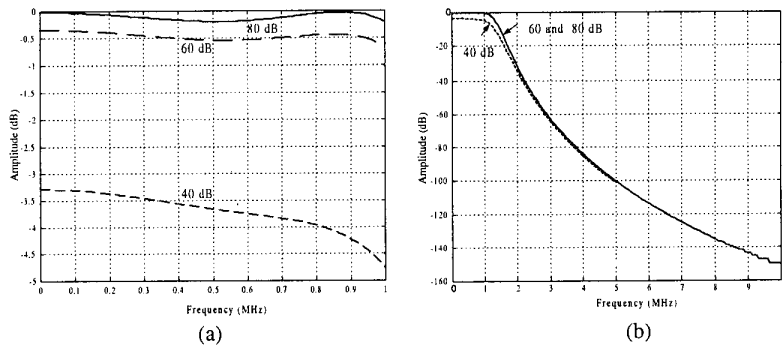


Figure 7. Computer simulated a) passband and b) overall amplitude responses with finite dc gain amplifiers (O/P2).