SYNTHESIS AND DESIGN OF A 7TH ORDER SC LOWPASS DECIMATOR COMBINING EXTERNALLY CASCADED AND LADDER STRUCTURES

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ABSTRACT - This paper proposes a computer-automated synthesis of SC decimators with a high decimating factor based on the statistical approach of the program (ISCMRATE) . This methodology is implemented based on multi-decimation building blocks, such as externally cascaded, internally cascaded or ladder structures and polyphase input networks. The design criteria are given to obtain and evaluate the performance of the corresponding resulting circuits. A design example of a 7th order SC lowpass elliptic decimator with M=10 is given to illustrate the above proposed methodology.

I. INTRODUCTION

IIR SC decimators usually include one of following structures: externally cascaded building block [1, 2], internally cascaded building block [3] or ladder structure [4]. The externally cascaded decimators present a simple structure and are particularly suitable to achieve higher decimating factors, but are known to be quite sensitive to component variations and have additional unwanted aliasing frequency components associated with the intermediate sampling frequencies of the cascade sections. On the other hand, all the blocks of internally cascaded filters and ladder filters work with the same input higher sampling frequency, and lower sampling frequency at the output. The internally cascaded and ladder-based structures allow the implementation of lower sensitivity architectures, but the designing procedure is too complex to implement a high order filter with a large decimating factor. Considered a moderate sensitivity of the lowpass amplitude, the design of the high order filter should comprise the above multi-structures instead of single structure [5]. In this paper, the design criteria of a SC decimator are proposed, and further demonstrate the design procedures of an example.

Firstly, the multistage and multirate SC implementations of sampling rate conversion are obtained from the prototype specification of a filter. Then, the appropriate sequence of pole-zero pairing is based on the selection of Q_p, Q_z factor and f_p, f_z in each building block in order to minimize the capacitance spread and total capacitor area [6]. After then, the corresponding circuit topology is selected considering a few factors, such as the total decimator sensitivity, minimum of the ratio of capacitance spread and total capacitor area, and sufficiently high ratio between the input /output sampling frequencies. The simulation program SWITCAP [7] will verify the frequency response of the decimators. Simplified flow diagram of the methodology for designing an optimum SC decimator based on multi-structures is illustrated in Fig. 1.

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II. MULTISTAGE IMPLEMENTATIONS OF SAMPLING RATE CONVERSION

For simplicity of explanation to design a IIR SC decimator, we consider a design procedure of the example that refers to a 7^{th} order low-pass SC decimator, with reduction of the sampling frequency from 500 MHz at the input to 50 MHz at the output. The maximum passband ripple is 0.3 dB up to the cutoff frequency of 1MHz, giving a minimum rejection of 100 dB above 5 MHz.

The first step in the design of a multistage IIR SC decimating filter is to employ single stage or multistage of sampling rate conversion [8]. Based on statistical approach of our program ISCMRATE , the optimum decimating factors and ripples in each stage are obtained according to the following design criteria:

1) Decompose the overall ripple of a filter by ascending order in order to reduce the corresponding decimator orders.
2) Implement the first stage with one of the largest multiple decomposed from the decimating factor M and decompose M in prime factors by descending order in order to minimize the speed requirements of the amplifiers.
3) The decimating factors in each building blocks or stages should not too large (M>10), especially in these decimators with internally cascaded or ladder structure

In this case, the total decimation factor M=10 can be factored into the product

$$M = \prod_{i=1}^{I} M_i \tag{1}$$

where I =2 for two building blocks. M_1 and M_2, respectively, represent decimation ratio in each stage. For a preliminary experimental demostration of the circuit structure, we may only consider the architecture with M_1=5 and M_2=2, from four posibilities, such as (10, 1), (1, 10), (5, 2), and (2, 5), based on the above conclusion. In the stage 1, the passband ripple is assigned as 0.25 dB and stopband is 95 MHz, the passband ripple in stage 2 should have 0.05 dB and corresponding stopband is 5 MHz.

III. THE SELECTION OF DECIMATOR TOPOLOGIES

After an optimal pole-zero paring strategy, the next step is to select a suitable structure to implement a circuit. The adoption of a particular topology, including the selection of the output terminal and the damping types, is carried out on an evaluation basis. The corresponding topology are obtained according to the following design criteria:

1) The optimum sequence of topology should be externally cascaded, internally cascaded or ladder structure, since decomposing M in prime factors by descending order and the internally cascaded or ladder structures may be restricted to moderate decimating factors.
2) There should not have two or more buiding blocks using the same damping type (E or FB) in the internally cascaded structures.
3) The selection of preferred circuit topologies is mainly related to its performance behavior under non-ideal characteristics of the amplifiers, namely the finite dc gain and bandwidth.

The selection of an optimum topology in this case, has determined an architecture with a 4^{th} order externally cascaded building block with M_1=5, followed by a 3^{rd} order ladder building block with M_2=2 as shown in Fig. 2.

IV.EXAMPLE AND RESULTS

Applying numeral multirate transfer function to lead to the respective matrices, with M_1=5, the modified z transfer function in the stage 1 be written as

$$H_e(z) = k_1 \frac{\sum_{k=0}^{10} n_{1k} z^{-k} \cdot \sum_{k=0}^{2} n_{2k} z^{-k}}{(1+\sum_{k=1}^{2} d_{1k} z^{-5k}) \cdot (1+\sum_{k=1}^{2} d_{2k} z^{-k})} \quad (2)$$

where k_1=1E-4 and whose numeric coefficients are given in Table I.

n_{10}	n_{11}	n_{12}	n_{13}	n_{14}	n_{15}	n_{16}	n_{17}	n_{18}
0.667	2.010	3.986	5.913	7.791	8.369	7.631	5.656	5.656
n_{19}	n_{110}	n_{20}	n_{21}	n_{22}	d_{11}	d_{12}	d_{21}	d_{22}
5.656	1.849	0.604	3.867	2.242	-1.8779	0.8828	-1.9419	0.9497

Table I Coeeficients of the multirate transfer function (2)

and modified z transfer function in the stage 2 be written as

$$H_1(z) = k_2 \frac{\sum_{k=0}^{7} n'_k z^{-k}}{(1+\sum_{k=1}^{2} d'_{1k} z^{-2k}) \cdot (1+d'_{21} z^{-2})} \quad (3)$$

where k_2=1E-3 and whose numeric coefficients are given in Table II.

n'_1	n'_2	n'_3	n'_4	n'_5	n'_6	n'_7	d'_{11}	d'_{12}	d'_{21}
2.4880	0.7438	-3.7568	-0.3929	2.4719	1.1057	3.0928	0.8985	-1.8758	0.8938

Table II Coeeficients of the multirate transfer function (3)

After scaling for maximum signal handling capability, normalizing with respect to the unit capacitance values, the program will generate the final all capacitor values shown a maximum capacitance spread of 20 and a total area close to 250 capacitor units for the complete circuit, the nominal passband and overall computer simulated impulse sampled amplitude responses are shown, respectively, in Fig. 3 (a) and Fig. 3 (b).

V. CONCLUSIONS

This paper proposes the computer automated synthesis of SC decimators with high decimating factors for designing, This methodology is implemented based on multi-decimation building blocks, externally and internally cascaded building blocks. The example clearly shows that design procedure for IIR SC decimator. The circuit will have a moderate sensitivity of the lowpass amplitude response due to the presence of the ladde structures.

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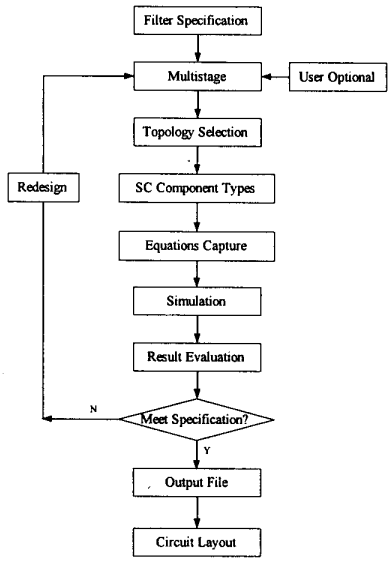


Fig. 1. General computer-aided tool methodology for SC multirate circuits design.

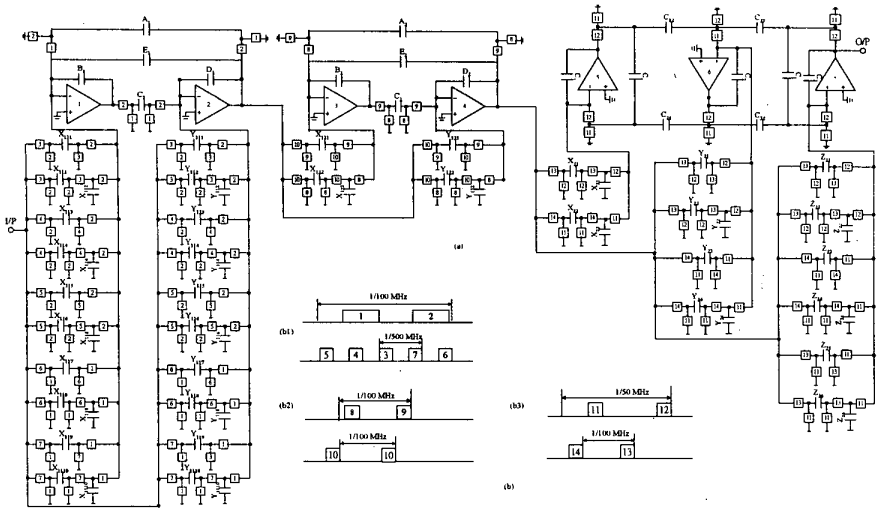
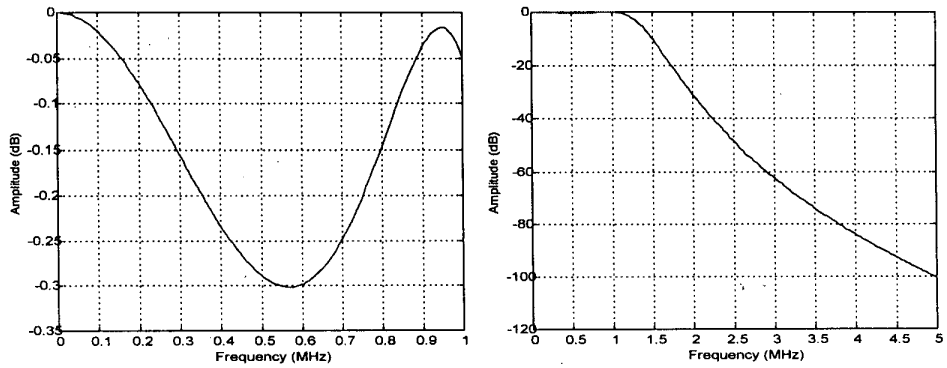


Fig. 2. 7th order SC decimating filter (a) SC circuit with M=10.
(b) Switching waveforms ((b1) and (b2) externally cascaded
(b3) ladder structure).



(a) (b)

Fig. 3. Nominal computer simulated amplitude response of the
7th order SC decimating filter in (a) Passband. (b) Overall.