SYNTHESIS AND DESIGN OF A 6TH ORDER SC LOWPASS DECIMATOR COMBINING EXTERNALLY AND INTERNALLY CASCADED STRUCTURES

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Abstract

This paper proposes an interactive architecture compiler for SC multirate circuits, here applied to the design of multistage IIR SC decimators with large decimating factors M. This methodology is implemented based on multi-decimation building blocks, such as externally cascaded, internally cascaded or ladder building blocks. A computer-based design is carried out to synthesize and evaluate the performances of the corresponding resulting circuits, in order to achieve the required anti-aliasing amplitude responses, to relax the speed requirements of the operational amplifiers, and also to reduce the capacitance spread and total capacitor area. A design example of a 6th order SC elliptic decimator with M=10 is given to illustrate the above methodology.

I. INTRODUCTION

It is generally a goal of the SC circuit designer to optimize circuit performance with IIR SC decimating techniques while simultaneously minimizing silicon area. The SC IIR circuits were obtained by applying the multirate transform to a prototype z transfer function in order to design the corresponding SC circuits. SC decimators usually include one of the following structures: externally cascaded building blocks [1, 2], internally cascaded building blocks [3] or ladder structure [4]. Externally cascaded decimators present a simple structure and are particularly suitable to achieve higher decimating factors, but are known to be quite sensitive to component variations and have additional unwanted aliasing frequency components associated with the intermediate sampling frequencies of the cascade sections. On the other hand, all the blocks of internally cascaded filters and ladder filters work with the same input higher sampling frequency, and lower sampling frequency at the output. The internally cascaded and ladder-based structures allow the implementation of lower sensitivity architectures, but the designing procedure is too complex to implement a higher order or a very large decimating factor filter. To optimize the use of the above architectures, an automated methodology that allows the combination of the above presented structures was recently proposed [5]. The purpose of this paper is to demonstrate the feasibility and applicability of that automated methodology (with some updated features), implemented by an interactive SC multirate compiler, to the design of a SC multistage decimator.

II. AUTOMATED METHODOLOGY FOR SC MULTIRATE CIRCUITS DESIGN

The general automated methodology for the design of SC multirate circuits can be schematically presented, as illustrated in Fig. 1 [5]. This automated methodology has been improved and implemented by an interactive computer program that will be designated as *ISCMRATE* (SC multirate compiler), which has been developed in C language and integrates the different parts presented in [5], namely, a filter synthesis tool - QED [6] together with the linear /nonlinear program tool - MATHPROG [7], the SC circuit simulator - SWITCAP [8], and the layout design program - MAGIC [9].

Based on a set of original specifications in terms of the frequency response, a prototype filter z transfer function is interactively generated by QED followed by a multirate transformation and the selection of the topology [1-4] for signal processing and data conversion. After capturing the set of equations and using linear programming methods, the resulting functional specifications are automatically determined in order to meet the frequency response requirements and the minimum value of the total capacitor area. This process will be followed by an external mixed mode simulation with SWITCAP that will verify the frequency response of the circuit. Finally, the layout synthesis of the filter will be generated based on the text mode output file from MAGIC.

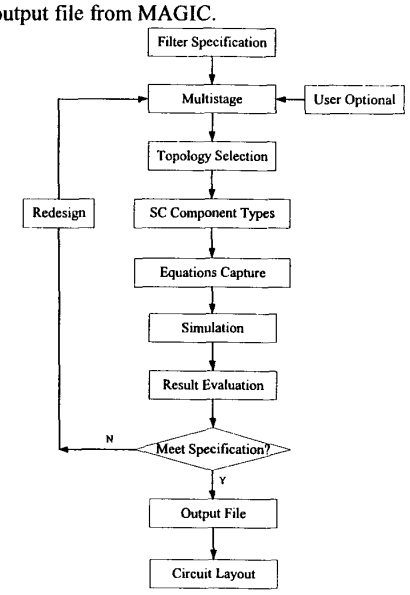

Fig. 1. General computer-aided tool methodology for SC multirate circuits design.

III. *ISCMRATE* COMPILER APPLIED TO THE DESIGN OF SC MULTISTAGE DECIMATORS

A simplified diagram of the proposed methodology for the design of multistage decimators, that is a part of the Interactive SC MultiRATE – *ISCMRATE* compiler, is presented in Fig. 2. An improved version of the previously presented automated methodology [5] has been developed allowing the optimization of the multistage design. When an user inputs a decimation factor M, after the prototype filter synthesis procedure, the biquadratic functions of both the numerator and denominator are fed into the pole-zero pairing module using the most suitable biquadratic functions for SC realization, with respect to the resulting values of the pole and zero Q-factors [10]. After that, a large decimation factor will be decomposed into the lowest common multiples of a few smaller integer numbers by descending order, that will be then applied in the multi-structure as the new blocks/stages decimation factors for multistage design [11]. Then, the appropriate sequences of circuit building blocks will be determined based on the basic circuits, such as externally cascade, internally cascaded, and ladder building blocks. After selection of a SC topology, the numeric equations will be determined based on the corresponding modified z-domain transfer functions. Then, the capacitance values are obtained using a pre-process set of linear or non-linear solutions, which are established to yield reduced capacitor area and low variability of the frequency response with respect to capacitance ratio errors [12]. The designer is also advised to adopt or not an alternative pole-zero pairing strategy, in order to synthesize a new topology [13]. *ISCMRATE* allows at this moment a complete automated procedure from the filter requirements until the selection of the cells layout (OA's, switches, capacitors), producing also an output file of the SWITCAP simulation.

IV. *ISCMRATE* COMPILER –EXAMPLE RESULTS

The performance of the *ISCMRATE* compiler is illustrated by means of a simple example of a 6^{th} order lowpass SC decimator, with reduction of the sampling frequency from 10kHz at the input to 1KHz at the output with the maximum passband ripple of 0.25 dB, the cutoff frequency fc=0.1 kHz, and minimum rejection of 75 dB above 0.5 kHz.

The multistage implementation of this decimator is shown in Fig. 3. The decimator architecture will be determined according with the above presentation. The selection of an optimum sequence topology, has determined an architecture with a 2^{nd} order externally cascaded building block with M_1=5, followed by 4^{th} order internally cascaded building block with M_2=2 as shown in Fig. 4. After scaling for maximum signal handling capability and normalizing with respect to the unit capacitance values, the decimator presents a maximum capacitance spread of 33 and a total area close to 220 capacitor units for the complete circuit, selected from six different solutions (different damping types and building block topologies). The selected overall circuit structure of the SC decimator is presented in Fig. 5. The nominal passband amplitude responses of stage I and stage II are shown in Fig. 6 (a) and Fig. 6 (b), and the nominal passband and overall computer simulated impulse sampled amplitude responses are shown in Fig. 7 (a) and Fig. 7 (b), respectively.

V. CONCLUSIONS

This paper proposes an interactive architecture compiler *ISCMRATE* applied to the design of multistage IIR SC decimators with large decimating factors M. The methodology is implemented based on multi-decimation cascaded building blocks, namely externally and internally cascaded and ladder blocks. The example presented, as the output of *ISCMRATE* compiler, clearly shows that the multiple decimating structures can effectively eliminate treacherous aliasing frequency components arising on SC multistage externally cascaded decimating filters and it demonstrates the compiler performance.

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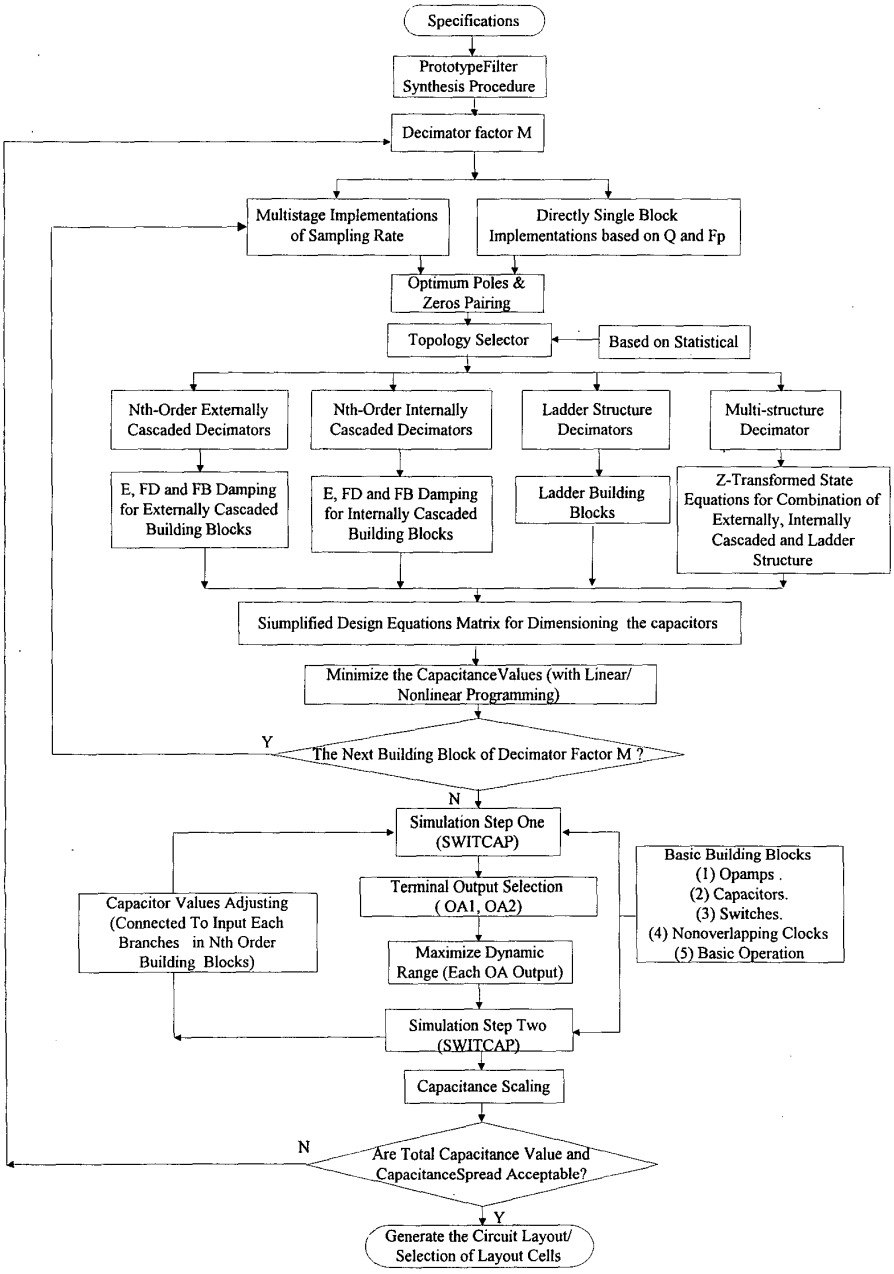


Fig. 2. Simplified flow diagram illustrating the methodology for designing optimum SC decimator based on multi-structures and decimating factor M (*ISCMRATE* Compiler).

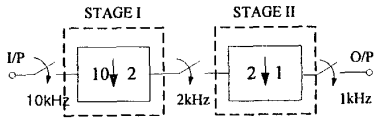


Fig. 3. 6th order multistage lowpass decimator combining an externally cascaded building block (M_1=5) and an internally cascaded building block (M_2=2) (synthesized by *ISCMRATE* compiler).

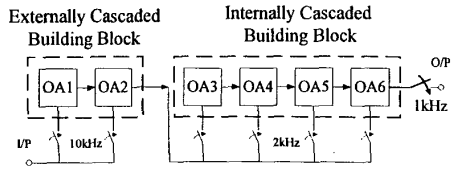


Fig. 4. Simplified architecture for optimum SC implementation.

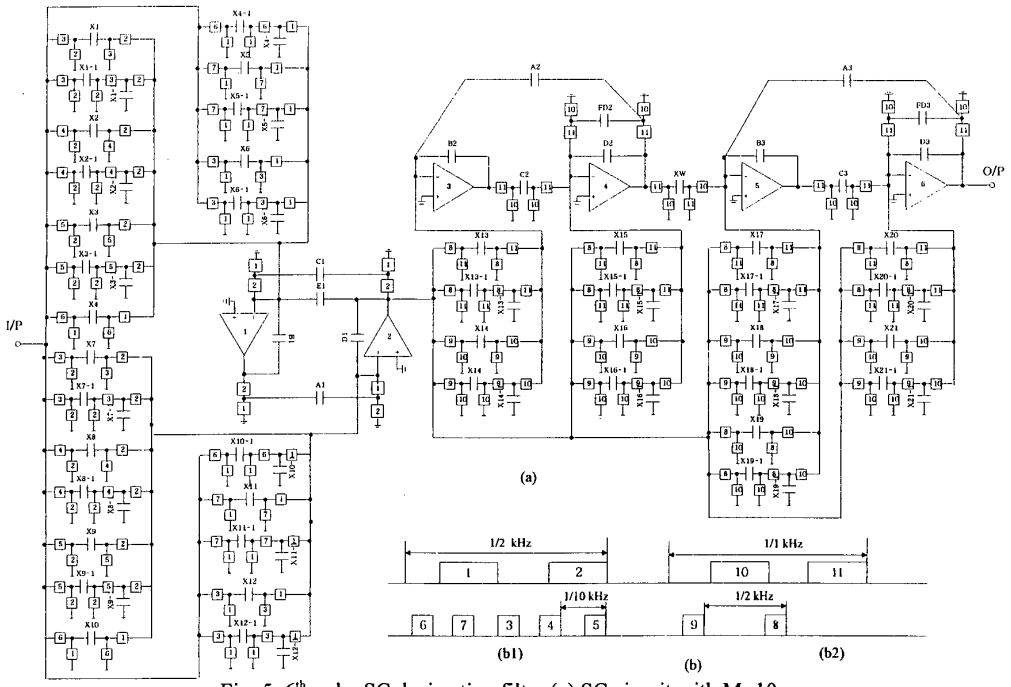
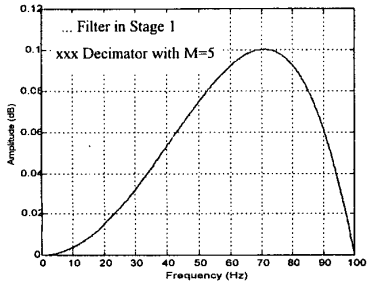
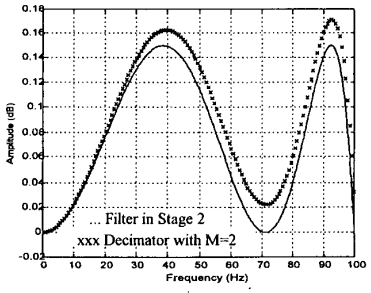


Fig. 5. 6th order SC decimating filter (a) SC circuit with M=10.
(b) Switching waveforms ((b1) externally cascaded, (b2) internally cascaded).

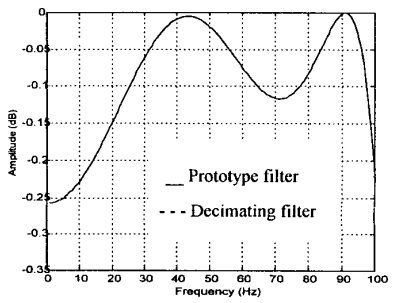


(a)

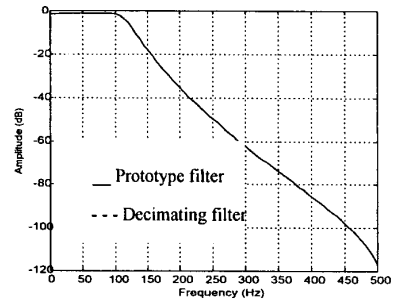


(b)

Fig. 6. Nominal amplitude response of
(a) Externally cascaded block with M_1=5.
(b) Internally cascaded block with M_2=2.



(a)



(b)

Fig. 7. Nominal computer simulated amplitude response of the 6th order SC decimating filter.
(a) Passband. (b) Overall.

(a)