Automated Design of SC Multistage Sampling Rate Converters Using Linear/Non-linear Programming

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Abstract-The automated design of SC multistage sampling rate converters is described. The optimum implementation of the circuit is obtained by linear / non-linear programming models and the capacitor values of the circuit are optimized to their minimum. The design of n-th order decimators is based on the different architectures using externally cascaded, internally cascaded and ladder structures. A design example is given to illustrate the proposed methodology.

I. INTRODUCTION

The design of Decimators and Interpolators [1], [2], [3] is one of the fascinating areas of multirate signal processing because it has wide attractive applications in telecommunications and video processing. Usually the building blocks for n-th order SC IIR decimator design are externally cascaded, internally cascaded [4], [5], and [6] or ladder structures [7]. In that type of design a large number of capacitor values need to be determined, which implies that a non-automated design procedure is only suitable for lower orders or one particular type of building blocks. This paper will present an automated methodology that combines the advantages of the different structures to meet the required specification. This automated approach can be easily extended to the design of more complex high order filters, sufficiently high ratio between the sampling frequency and the maximum signal frequency of interest. The method is relatively fast and an accurate frequency response can be obtained.

The strategy for decimation, pole-zero pairing and an appropriate sequence of different building blocks (ladder, internally or externally cascaded) has been determined in order to improve signal handling capability and minimize capacitance spread. In the large majority of cases, the linear equations for the transmission factors of the input polyphase network are obtained and solved for optimum values. Linear/ non-linear programming methods have also been used, e.g. the simplex method.

II. MODELING OF THE CIRCUIT

The automated methodology for designing a multistage n-th order IIR SC decimator is presented in Fig.1. A computer program that allows the different choice between the circuit architectures for a given frequency response specification was designed in C language and it includes the following parts:

1. Input specifications.
2. Prototype z-transfer function analysis.
3. Modified z-transfer function analysis and circuit architecture.
4. Best solution obtained with a linear/non-linear programming model.
5. Frequency response output simulation.
6. Automatic feedback procedure for dynamic range and capacitance values optimization.
7. Circuit layout.

Parts 1 and 2 are implemented using the QED program for Unix [8]. The types of filter supported by QED include IIR Lowpass, Highpass, and Bandpass Filters with orders up to 80 being the user interface as presented in Fig. 2 and Fig 3.

Part 3 is programmed for the determination of different circuit architectures based on the already referred building blocks. The automated procedure can even allow the use of different types of the above mentioned building blocks for the implementation of a specific modified z- transfer function. A design example combining the basic SC IIR building blocks (Externally cascaded and/or internally cascaded and/or ladder structure) will be presented next.

Part 4 allows the implementation of a linear / non-linear system model with a linear / non-linear programming tool designated Mathprog [9] for obtaining an optimum solution.

Parts 5 and 6 are implemented using the simulation tool Switcap II [10] allowing the calculation of computer simulated amplitude responses.

Part 7 (under development) will implement the interface between Switch II circuit description and the layout of the circuit based in a library of cells.

The main goals of the automated design procedure (e.g. the maximization of the gain-bandwidth, the mini-mization of capacitance spread and capacitor area) and the performance parameters that are design objectives can be interchanged among each other. A design trade-off between the multiple performance and the parameters can then be implemented and the objectives above refereed can be written down as:

$$\text{Minimize } C=\sum_{i=1}^{n}\sum_{j=1}^{m} c_{ij}$$

Where C is the total capacitance area in the circuit, n is the Operational Amplifier-OA number in the circuit, m is the number of capacitor numbers in each OA block and c_{ij} are the normalized absolute capacitor values.

For a linear mode (e.g. externally/internally cascaded building blocks), we can define

$$\sum_{i=1}^{N}\sum_{j=1}^{M} a_{ij}x_{ij} = b_j$$

Where the constraints are

j=1,2,...,N (filter order) and

i=1,2,...,M (total number of capacitors)

and a_{ij} are the coefficients of the capacitor variables, x_{ij} are the capacitor variables of the circuits, and b_j are the numerator coefficients of the modified z-transfer function.

For a non-linear mode (e.g. ladder structure), is possible to define

$$\sum_{i=1}^{N}\sum_{j=1}^{M} a_{ij}\prod x_{i'j'} = b_j$$

where i', j' will be the arbitrary combination of capacitors.

III. CIRCUIT IMPLEMENTATION

For internally & externally cascaded SC IIR decimation building blocks, system models are linear and they can be optimized by linear programming to improve the efficiency of the automated procedure. For ladder structures, it is

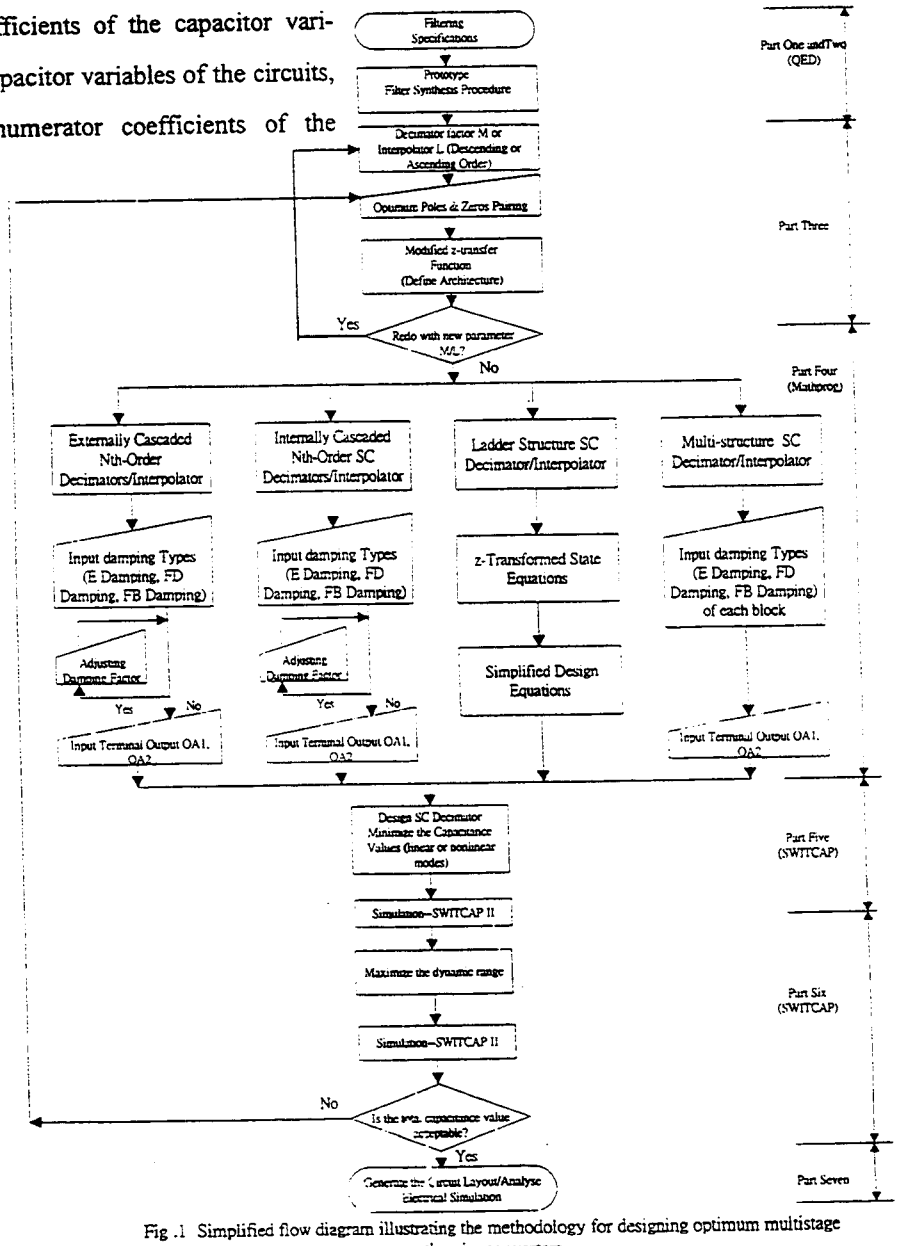
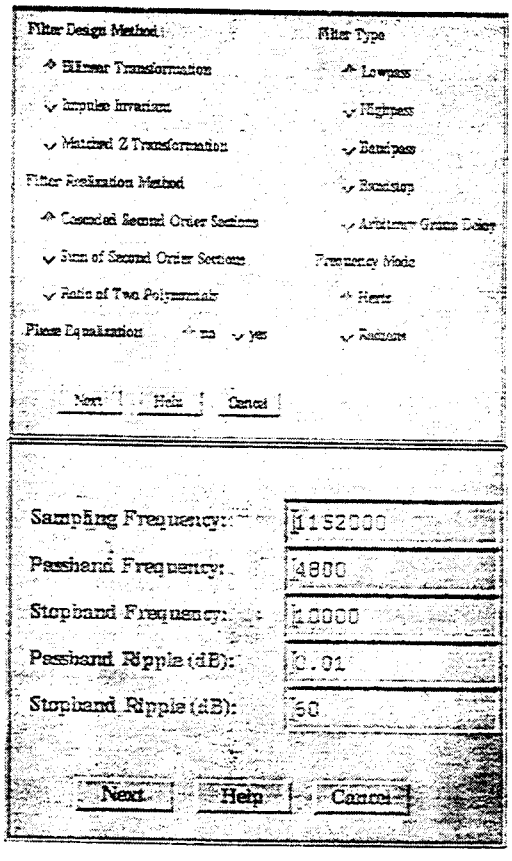


Fig .1 Simplified flow diagram illustrating the methodology for designing optimum multistage n-th order converters.

necessary to apply a non-linear model due to the non-linearity of that type of structures. In order to design a CAD program to solve flexible cases of SC IIR decimation a combination of the 2 programming models together with the specified model of decimation can be used. That program will have the following features: dynamic n-th order of the circuit, dynamic M decimation factor and different types of circuit block connections.

IV. DESIGN EXAMPLE

A Cascaded 6-th Order SC Elliptic Lowpass Decimator with M=6, cut-off frequency f_c =4800Hz and input sampling frequency MFs=1.152MHz is presented as a design example obtained with the methodology presented before. The input specifications of the decimator are presented using the interface window given in Fig.2 and the amplitude response of the prototype z-transfer function in Fig.3. The overall design includes a 4-th order internally cascaded filter with M=2 and followed by a 2-nd order externally cascaded filter with M=3. The circuit architecture and nominal computer simulated response are presented in Fig.4 and Fig.5 respectively. The capacitance values of externally cascaded and internally cascaded blocks are listed in Table I after maximum signal handling and normalizing with respect to the unit capacitance value.



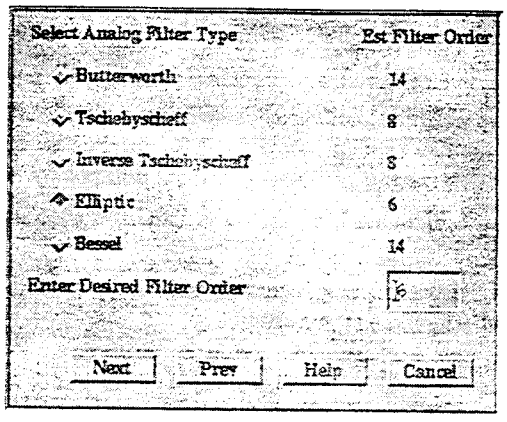


Fig.2 Input specifications of the 6-th order decimator.

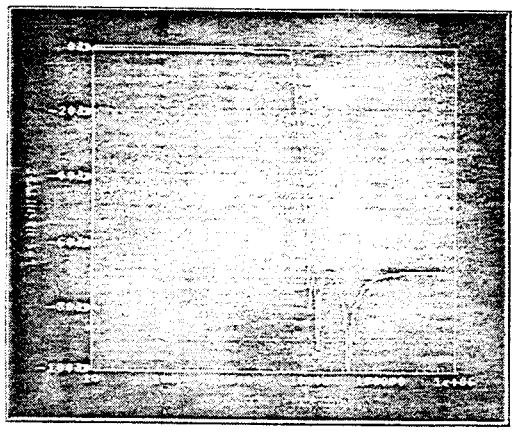


Fig.3 Amplitude response of prototype decimating filter.

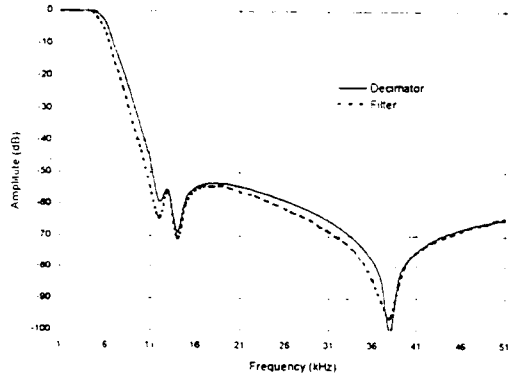


Fig.5 Nominal computer simulated amplitude response.

V. CONCLUSIONS

An automated method has been presented which combines the different types of IIR SC decimator building blocks together with optimization of total capacitance values and capacitance spread. The derivation of the design plans has been largely automated by means of a modeling environment using linear/non-linear programming to obtain the value of the capacitors.

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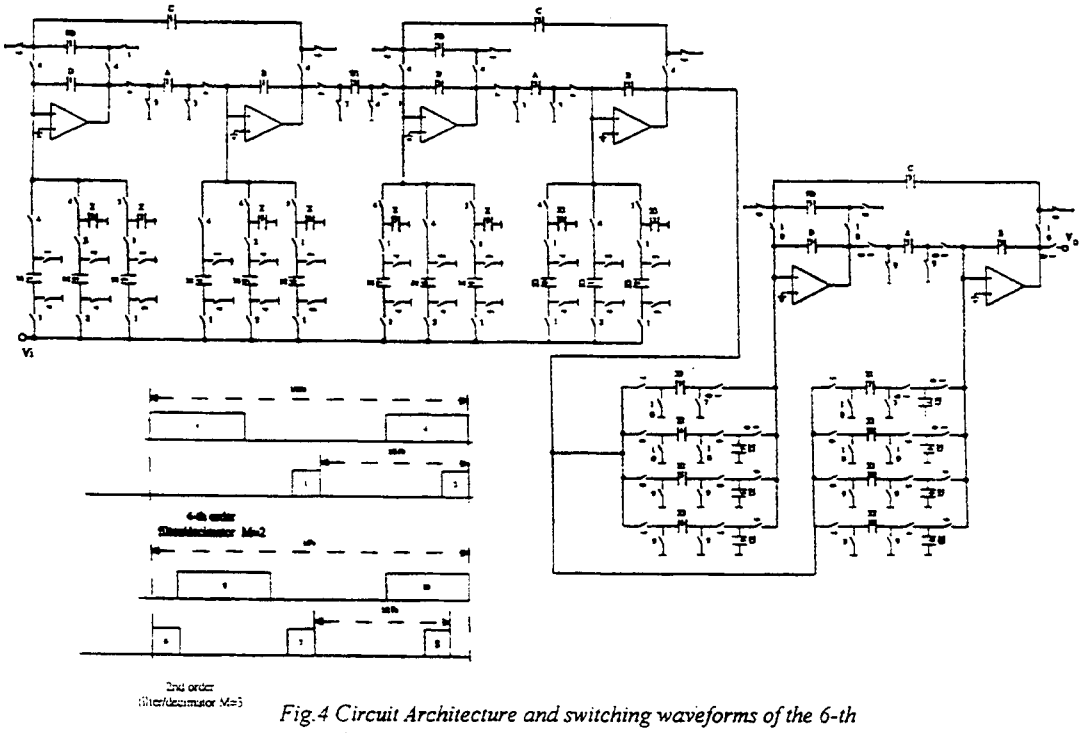

Fig.4 Circuit Architecture and switching waveforms of the 6-th order cascaded lowpass SC decimating filter with M=6.

4-th order				2-nd order	
OA1	OA2	OA3	OA4	OA5	OA6
A1=4.10	B1=10.11	A2=5.01	B2=10.60	A3=9.10	B3=10.20
C1=4.50	D1=12.10	C2=5.71	D2=15.00	C3=2.10	D3=6.07
E1=0.00	FD1=7.50	E2=0.00	FD2=4.70	E3=0.00	FD3=2.20
FB1=0.00	W12=1.60	FB2=0.00		FB3=0.00	
X1=3.00	X4=3.00	X7=8.01	X10=7.60	X13=9.20	X17=2.804
X2=4.70	X5=1.00	X8=5.07	X11=1.00	X14=4.20	X18=6.10
X3=0.00	X6=0.00	X9=7.00	X12=0.00	X15=1.00	X19=5.00
				X16=0.00	X20=1.00

Table I Capacitance values of the 6-th order decimator.