16.4 A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration

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Wireless communication systems and Ethernet networks call for moderate-resolution GS/s energy-efficient ADCs. While previous work [1] shows that the multi-bit per cycle SAR ADC can achieve low power due to various hardware reduction techniques, there are still a few limitations that restrain this architecture. First, the pre-charge slows down the logic and the DAC settling, especially during the MSB conversions. Second, unlike the offset among sub-channels of interleaving SAR ADCs, which can be easily calibrated in the background at the ADC backend [2], the offsets of the comparators in multi-bit SAR ADCs lead to a large sub-ranging error. Such offset is often calibrated in the foreground [1][3] but cannot track voltage and temperature (V&T) variations. This paper presents a 1-then-2b/cycle SAR architecture which removes conventional pre-charging and simultaneously minimizes the logic circuitry complexity to that of a 1b/cycle SAR. The comparator offsets are calibrated in the background without any extra phases or input references. With 2× time interleaving, the prototype achieves 2.4GS/s using a 0.9V supply in 28nm CMOS, leading to a 25.3fJ/conv-step Walden FoM at Nyquist input.

Figure 16.4.1 shows the overall ADC architecture, which consists of two interleaving channels. First, the differential input signals are sampled onto the top-plate of the DAC arrays through a common-clock-bootstrapped technique. A capacitive interpolation technique is adopted to reduce one DAC array, and a self-time-loop circuit generates a clock signal with four pulses to trigger the comparators. Three comparators are used together right after the sampling but give only 1b resolution. Next, a register secures this decision and feeds it to both DAC arrays to perform switching for the upcoming multi-bit operation. The architecture then resolves 7b with 3 more 2b/cycle comparisons along with 2 switching phases. Offset calibration is running in the background, which tracks the V and T variation on the comparator offsets. The other channel works with an identical sequence in an interleaved manner. The decoder deciphers both channels output codes, which are later combined by a multiplexer.

Multi-bit SAR ADCs often need extra pre-charging phases and DAC switching to generate reference-embedded residual voltages ($V_{in}\pm V_{ref}/4$, for a 2b/cycle example) for multi-bit comparisons. Such pre-charge not only increases the design complexity but also induces larger delay. Especially for the first MSB segment, the MSB capacitors need to shift up/down, which occupies a long period before the 1st comparison. Previous work [3] adds extra reference DACs and a 4-input comparator to resolve this issue but this requires extra redundancy cycles to correct the intermediate mismatch error. Such a solution can lead to diminishing returns on the speed for moderate resolution designs since there are only a few cycles. Here, a 1-then-2b/cycle SAR removes pre-charging with a simple logic arrangement. Figure 16.4.2 shows the residue voltage, the segment DAC (example of DAC1,P) and the corresponding control logic of the 1-then-2b switching scheme. The DAC is segmented into 4 sections to simplify the SA control. After the first comparison, 1b decision feeds to a dynamic register-mux and directly controls the SA switching without any extra pre-charging logic. The remaining multi-bit switching cycles pass through the same register circuit with multiple-comparator feedback, meaning that the logic circuit is now as simple as a 1b/cycle SAR ADC. Compared with the conventional 6b 2b/cycle architecture, the extra 1b comparison in the 1-then-2b architecture induces only a small speed penalty as it is done right after the sampling and able to save all of the pre-charging phases. Furthermore, in order to avoid a wide DAC layout and a large top-plate parasitics (that reduces the full swing of this design due to the top-plate sampling), the unit-capacitor structure is modified to shrink the total width of the conventional design by half, which also helps reduce the top-plate parasitic.

Frequently, background calibration requires extra cycles or injected signals [4], which increase overhead. Here, with the calibration fully embedded in the ADC, extra input references or calibration cycles are not necessary. Figure 16.4.3 illustrates the concept of the calibration scheme. After sampling, all of the comparator inputs are identical. Even though the first comparison only resolves 1b, it is highly undesirable to add gating on the clock signal of the comparators. First, it degrades the speed and increases the design complexity. Second, saving the power of two comparisons is quite small and extra clock signals may lead to diminishing returns. Instead, the first comparison not only gives one bit resolution but it is also used in the background offset calibration. Since 3 comparators have a common input, their outputs should be the same in the absence of offset mismatch. The target of the calibration engine is to align all the 3 comparator outputs by feeding back calibration voltages ($V_{cal,P/N}$) to the extra calibration transistor pair at the comparator input. As one comparator is utilized as reference, only two comparator offsets need calibration which also further saves hardware. It is worth noting, as Fig. 16.4.3 illustrates, that the calibration can only be activated when the input is within the offset of the two comparators, and the $V_{cal,P/N}$ only updates during the sampling phase. An R-2R DAC is adopted to provide the calibration voltages and to avoid leakages.

Figure 16.4.7 shows the ADC core with on-chip background offset calibration fabricated in 28nm CMOS. The ADC full swing is $0.9V_{pp}$ with a 0.63V input common-mode voltage, and the total input capacitance is ~64fF including parasitics. The power consumption is 5mW from a 0.9V supply operating at 2.4GS/s while the calibration consumes ~370μW. Figure 16.4.4 illustrates the measured SNDR and SFDR versus the input frequencies where the SNDR stays above 40dB up to the Nyquist input (Chip 4). Figure 16.4.4 also shows the frequency spectrum after calibration at the near-Nyquist tone, and also reports the performance of multiple chips at Nyquist input. The SNDR of the prototype is mainly limited by noise. The maximum DNL/INL in chip 4 are -0.49/-0.57 LSB (limited by the accuracy of the split capacitor), respectively. The worst performing chip (#3) is used to demonstrate the robustness of the calibration. Figure 16.4.5 shows that the ADC with calibration works under a wide range of temperature, input common-mode and supply voltage variation. Figure 16.4.6 summarizes the ADC performance and compares it with the state-of-the-art. With a single channel running at 1.2GS/s, it achieves >40dB SNDR at Nyquist input with 7b quantization and working at less than 1V supply voltage.

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References:
[1] C. H. Chan, et al., "26.5 A 5.5mW 6b 5GS/S 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS," *ISSCC*, pp.466-467, Feb. 2015.
[2] Ying-Zu Lin, et al., "A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with fast reference charge neutralization and background timing-skew calibration in 16-nm CMOS," *IEEE Symp. VLSI Circuits*, pp. 1-2, June 2016.
[3] H. K. Hong, et al., "A Decision-Error-Tolerant 45 nm CMOS 7b 1 GS/s Nonbinary 2b/Cycle SAR ADC," *IEEE JSSC*, vol. 50, no. 2, pp. 543-555, Feb. 2015.
[4] L. Kull, et al., "A 3.1mW 8b 1.2GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32nm digital SOI CMOS," *ISSCC*, pp. 468-469, Feb. 2013.
[5] M. Miyahara, et al., "22.6 A 2.2GS/s 7b 27.4mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers," *ISSCC*, pp. 388-389, Feb. 2014.

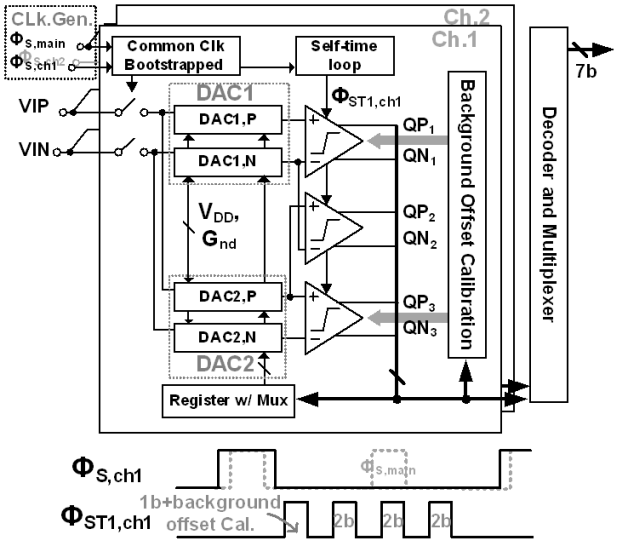


Figure 16.4.1: Overall 2× interleaved 1-then-2b/cycle SAR ADC architecture.

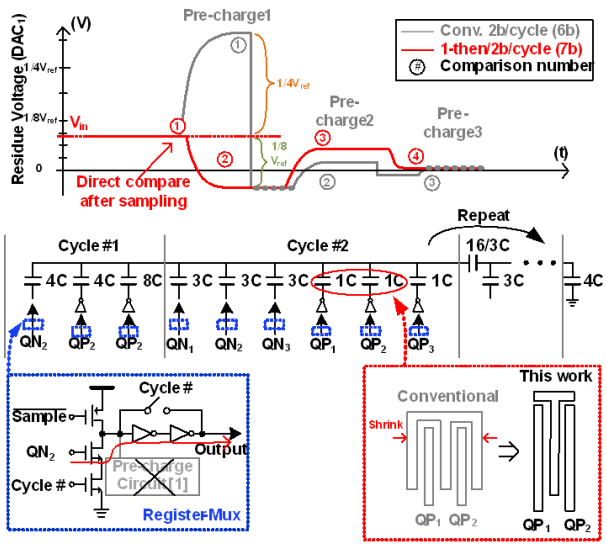


Figure 16.4.2: Residue voltage, DAC array and logic control of DAC1.

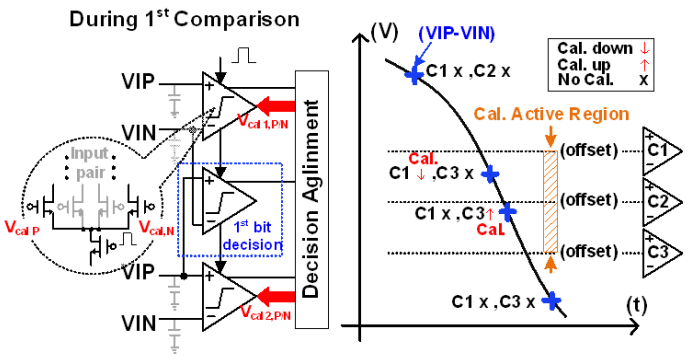


Figure 16.4.3: Concept of background offset calibration (left) and calibration with different input voltages (right).

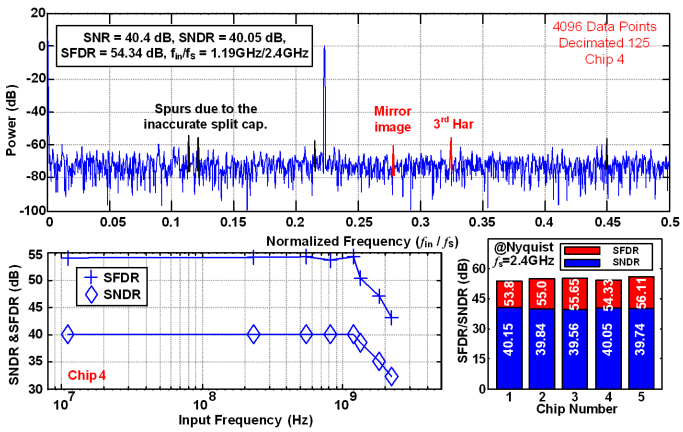


Figure 16.4.4: Spectrum with near Nyquist input (decimated 125×), measured SFDR and SNDR vs. input and SNDR/SFDR @ Nyquist input for 5 samples.

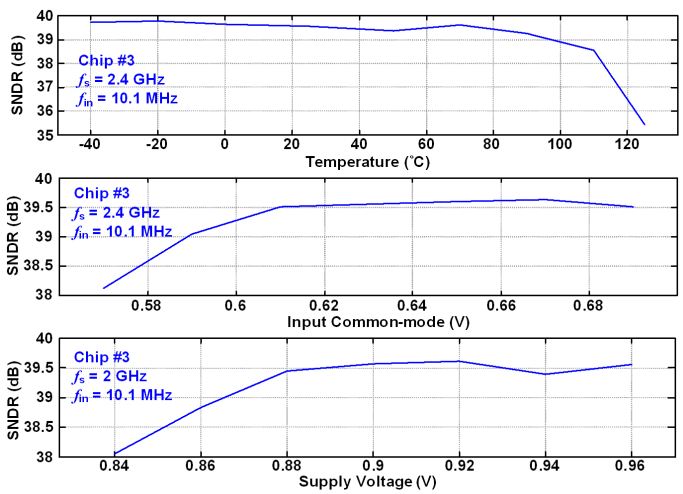
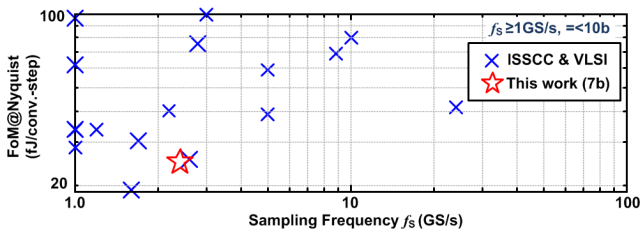


Figure 16.4.5: Measured SNDR with low-frequency input under temperature, input common-mode and supply voltage variation.



Publication	ISSCC'14 [5]	JSSC'15 [3]	ISSCC'13 [4]	This work	VLSI'16 [2]
Architecture	Folding Flash	2b/cycle SAR	SAR	2xTI 1-2b SAR	4xTI SAR*
Technology	40nm	45nm	32nmSOI	28nm	16nm
Supply (V)	1.1	1.25	1.0	0.9	0.95
Resolution	7b	7b	8b	7b	10b
f_S (GS/s)	2.2	1.0	1.2	2.4	1.6
SNDR@Nyq(dB)	37.4	40.8	39.3	40.05	50.3
Input Cap. (F)	300f	600f	128f	64f	N/A
Power (mW)	27.4	7.2	3.06	5.0	8.2
FoM@Nyq. (fJ/conv.-step)	205.7	80	34	25.3	19.23
DNL/INL	0.6/0.6	0.4/0.5	0.79/0.91	0.49/0.57	0.62/0.81
Area (mm^2)	0.052	0.016	0.0015	0.0043	0.023
Offset Cal.	No need	Foreground	Background	Background	Background

*Need Timing-skew calibration (offchip)

Figure 16.4.6: Benchmark and table of comparison with state-of-the-art ADCs.

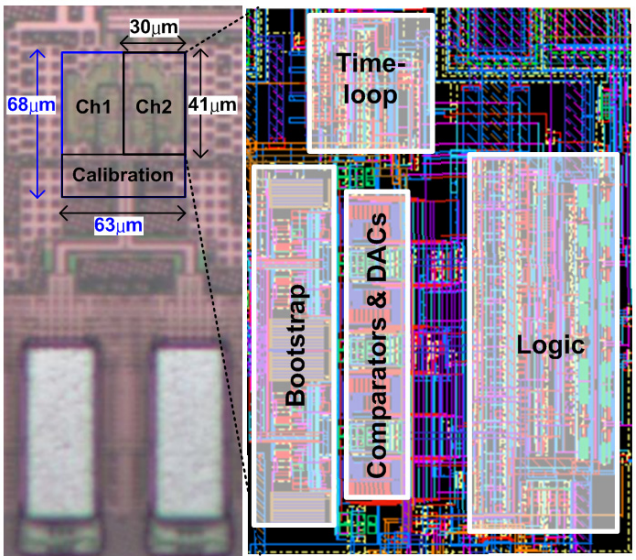


Figure 16.4.7: Chip microphotograph and close up layout view.

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