A 94-dB DR,105-Hz Bandwidth Interface Circuit for Inertial Navigation Applications

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***Abstract*— This paper presents a fully differential high-resolution analog interface circuit to apply in an inertial navigation system. By integrating an anti-aliasing filter and a second order sigma-delta modulator into a single chip, the interface circuit can achieve high-resolution with low power consumption. The prototype fabricated in a 0.25 µm CMOS process achieves a dynamic range (DR) of 94 dB, a SNDR of 83.4 dB over the bandwidth of 105 Hz, where the total power consumption is 363.2 µW at 1.6 V supply. Based on the simulation results the sigma-delta modulator block achieves a SNDR of 101 dB while consuming a power consumption of 43 µW, which yields a Walden Figure of Merit (FoM) of 1.7 pJ/conv-step and a Schreier FoM of 157 dB.**

I. INTRODUCTION

To achieve high-resolution with low bandwidth sigma-delta (ΣΔ) modulators are widely utilized in inertial and force sensing applications, such as, accelerometers and gyroscopes, etc. [1]. In the micro-mechanical accelerometer application since the most mechanical bandwidth is below 1 KHz, sigma-delta ADCs can effectively reduce noise to achieve high resolution by employing a high oversampling ratio (OSR).

Interface circuits can be categorized at the architecture level as either force-feedback closed loop [2][3] or open loop [4][5]. The closed loop interface circuit offers low noise and high linearity. However, it consumes significant power preventing its wide use in navigation application systems. On the other hand, the open loop interface circuit has low power consumption, but the performance is quite poor due to the noise generated by the analog interface front-end circuit [4]. Therefore, the motivation arises to design an interface circuit that achieves high resolution when compared with closed-loop interface while operating at low power.

Technology downscaling allows the integration of the anti-aliasing filter (AAF) and the ADC into a single chip achieving a good trade-off between performance and power consumption. Besides, it has extensive application since the interface area consumption is smaller than before.

This work presents a fully differential high-resolution ΣΔ open loop interface circuit for inertial navigation systems. To satisfy an application requirement we utilize a second order active RC anti-aliasing filter to remove the out-band noise with a cut-off frequency of 105 Hz, followed by a second order sigma-delta modulator. Experimental results of a prototype fabricated in 0.25 µm CMOS demonstrate the effectiveness of the proposed structure. The total power consumption of the proposed circuit is 363.2 µW and it achieves a SNDR of 83.4 dB.

The organization of the paper is the following: It presents the overall interface circuit structure in Section II and its respective implementation in Section III. Section IV summarizes the measurement results and, finally, Section V concludes the paper.

II. OVERALL SYSTEM STRUCTURE

Although inertial navigation systems use a high-resolution ADC chip the front-end filter limits the overall system resolution. It is easy to obtain such a low-pass filter with external capacitors and resistors before the ADC. However, its implementation suffers from poor performance and excessive power consumption. In order to optimize the overall performance, we propose the integration of the anti-aliasing filer and a sigma-delta modulator into a single chip, as illustrated in Fig. 1 that exhibits the block diagram of the proposed interface circuit.

Since the signal bandwidth of the accelerometer sensor is from 1 Hz to 400 Hz, it is necessary a second order RC low-pass filter is implemented to cut off the out-band noise. Moreover, a second order ΣΔ modulator will lead to a SNDR of 100 dB.

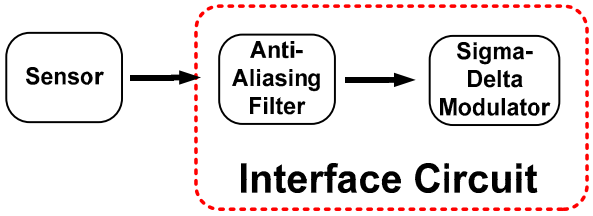

Fig. 1. Block diagram of the proposed interface front-end structure

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The proposed interface circuit allows low power consumption while achieving high resolution with reduced chip area becoming attractive for several applications.

III. Interface Circuit Implementation

A. Anti-Aliasing Filter

A passive filter when compared with its active counterpart is more robust to the loading variation caused by the impedance. A second order active RC filter has its cut-off frequency f_0 determined by the combination of resistance and capacitance as follows,

$$f_0 = \frac{1}{2\pi\sqrt{C_1 C_2 R_2 R_f}} \tag{1}$$

requiring large values of capacitors and resistors to achieve a low value that meets the requirement of a low bandwidth.

Since the front-end thermal noise limits the overall system performance, as illustrated by (2), it imposes a small value of resistor. However, a small resistor implies a very large capacitor for a constant f_0. Considering the trade-off between R and C, we can choose R_2 and R_f as 135 KΩ and 18 KΩ, and C_1 and C_2 as 10 nF and 100 nF (implemented off-chip), respectively.

Fig. 2 shows the architecture of the second order active RC low-pass filter, utilized in the front-end of the interface circuit as an AAF. C_1 and C_2 are off-chip due to their large area. For the thermal noise we can obtain the expression,

$$V_n = 4K_b TR \tag{2}$$

where V_n is the thermal noise contribution from the R, K_b is the Boltzmann's constant, T is the Kelvin temperature, and R is the resistance.

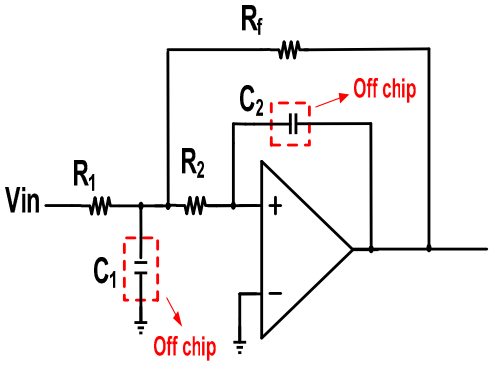

Fig. 2. Anti-Aliasing Filter architecture (C_1 and C_2 are off-chip).

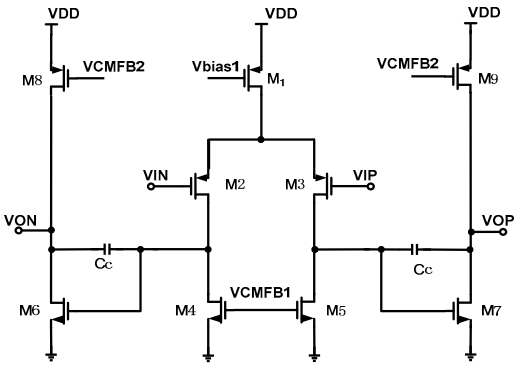

Fig. 3. Circuit implementation of op-amp.

B. Sigma-Delta Modulator

High-resolution application systems widely utilize sigma-delta modulators benefiting from their oversampling and noise shaping, where the latter allows high resolution in a certain frequency domain. To achieve a target SNR, a second order ΣΔ modulator employing a reasonable OSR is the optimum choice allowing good system stability.

The choice of an OSR=250 satisfies the SNR requirement of this sigma-delta modulator. Fig. 3 demonstrates the circuit implementation of op-amp in the first integrator, which achieves a dc gain of 45 dB and a GBW of 1 MHz, while drawing 4 μA bias current. Fig. 4 exhibits the circuit implementation of the second order discrete-time (DT) ΣΔ modulator, in its single-ended version for simplicity. Cascaded integrators in feed-forward (CIFF) configuration with input signal feed-forward topology reduce the output signal swing in the integrator and minimize the performance degradation due to coefficient variations [6]. Moreover, the implementation of a passive adder in this feed-forward structure allows low power consumption. The utilization of a 1 bit quantizer minimizes the digital filter complexity and avoids the need of linearization techniques in the digital-to-analog converter (DAC) feedback.

Initially, all noise sources of a DT ΣΔ modulator include the quantization noise, thermal noise, DAC mismatches, and other noise. Thermal noise is the dominant noise source in a DT ΣΔ modulator, which is equivalent to 45% of the total noise [7]. In the design of the DT ΣΔ modulator, the thermal noise of the first integrator is critical, because it will not be noise shaped and it appears directly at the output of modulator.

Thermal noise is an essential factor defining the sampling capacitor value of the first integrator, since the main sources of the thermal noise in the first integrators are "on" resistances of the switches. Moreover, the $R_S C_S$ network establish a low pass filter that imposes a colored noise spectrum across the capacitor. Multiplying the thermal noise by the square of the transfer function of the $R_S C_S$ filter, it can eliminate R. After calculation, the thermal noise becomes (3),

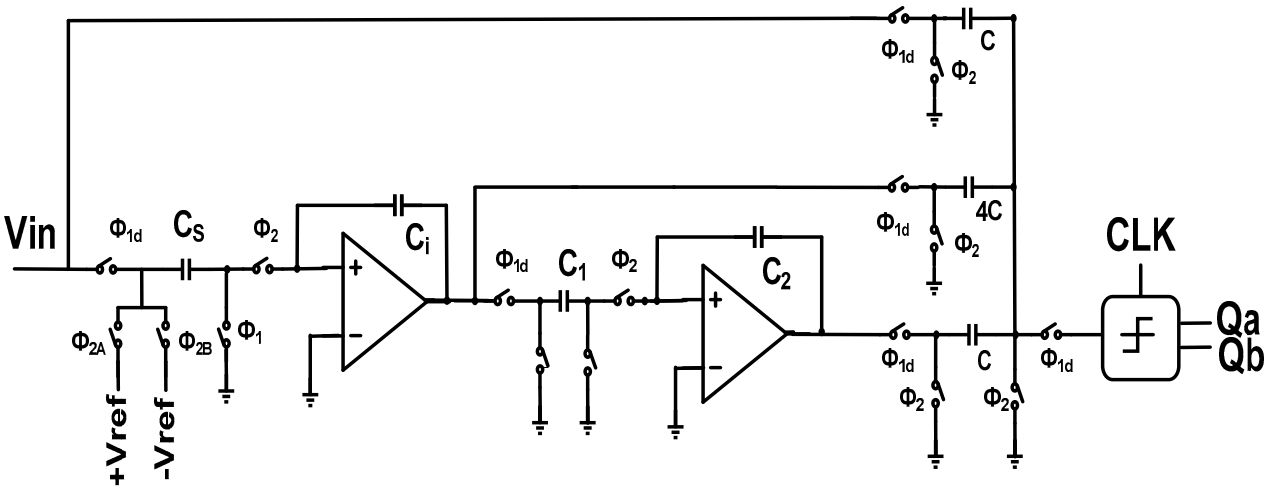

Fig. 4. Circuit implementation of the Discrete-Time ΣΔ modulator.

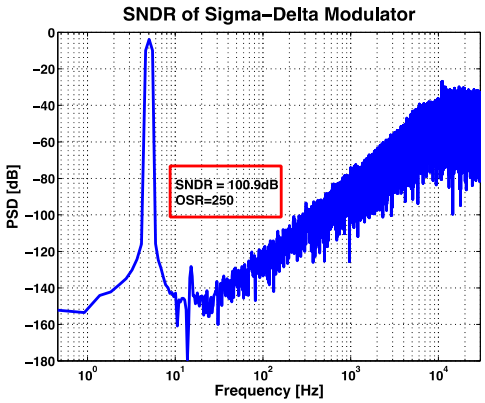

Fig. 5. FFT plot of the ΣΔ modulator (Simulation Results).

$$P_{KT/C} = \frac{4KT}{C_S OSR} \tag{3}$$

where $P_{KT/C}$ is the power of the thermal noise and C_S is the sampling capacitor of the first integrator. Considering that 85% of the total modulator input-referred thermal noise is coming from the modulator front-end, the estimation of the value of its sampling capacitor is 1.1 pF. Due to 10% process variations for the capacitors, the sampling capacitor considered for this design is 1.22 pF.

Since the thermal noise contribution of the second-stage sampling capacitors is a small portion of the total thermal noise budget their values are smaller. Fig. 5 exhibits the simulation FFT plot of the ΣΔ modulator with transient noise, the SNDR is 101 dB for an OSR of 250.

IV. Measurement Results

The interface circuit fabricated in a standard 0.25 µm CMOS process has a supply voltage of 1.6 V. The AAF is a second order active RC low-pass filter with off-chip capacitors in the front interface circuit, which achieves a bandwidth of 105 Hz. After the AAF, a second order sigma-delta modulator is next with an OSR of 250.

The chip microphotograph shown in Fig. 6 includes the total core occupying an area of 0.032 mm^2, where the sigma-delta modulator resides in 0.027 mm^2. Fig. 7 illustrates the measured AAF frequency response (compared with simulated result). The measured cut-off frequency (-3dB) is 105 Hz, which matches well with the simulation result (106 Hz).

Fig. 8 depicts the measured FFT plot of the interface circuit output, the peak SNDR and SNR are 83.4 dB and 88 dB, respectively, with a signal bandwidth of 105 Hz. Furthermore, the measured SNR and SNDR versus input amplitude at 5.4 Hz with a 60 KHz sampling clock are illustrated in Fig. 9, which achieves a DR of 94 dB.

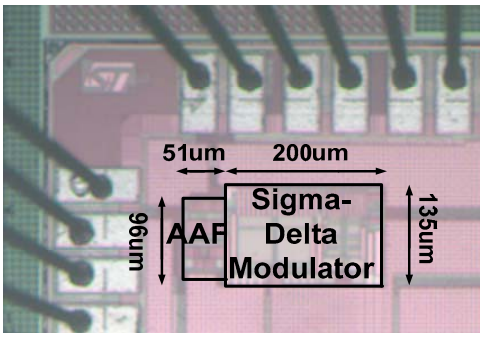

Fig. 6. Die microphotograph of the chip.

Table I summarizes and compares the overall measured performance with state-of-the-art analog interface circuit. The measurement results show that the interface circuit with active RC filter can achieve a DR of 94 dB and a SNDR of 83.4 dB over the bandwidth of 105 Hz, while the power consumption is 363.2 µW. For the sigma-delta modulator, the simulation result shows the SNDR is 101 dB while consuming only 43 µW power consumption. Further, the circuit exhibits a Walden FoM (FoM_W) of 1.74 pJ/conv-step and a Schreier FoM (FoM_S) of 157 dB.

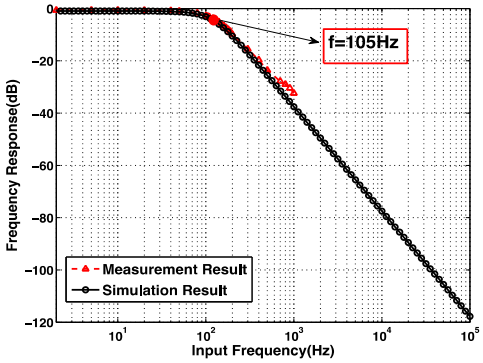

Fig. 7. AAF frequency response (measurement & simulation).

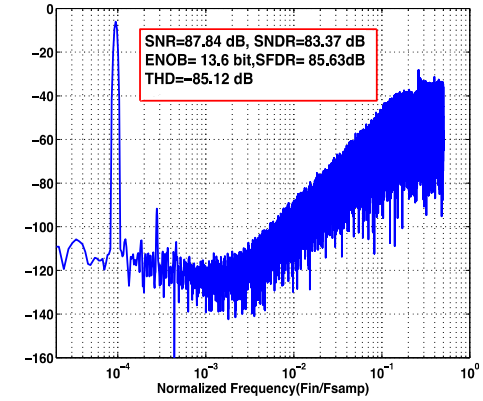

Fig. 8. Measured FFT of the overall interface circuit.

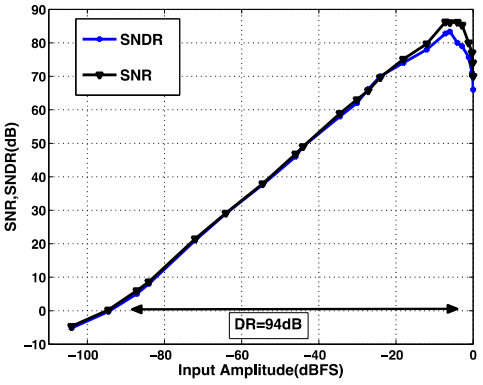

Fig. 9. Measured SNR, SNDR versus input amplitude of the overall interface circuit.

V. CONCLUSIONS

This paper presented a fully differential analog-to-digital front-end interface circuit with a DR of 94 dB with an open loop structure, which can operate at 1.6 V supply voltage. The fabricated interface circuit integrated an anti-aliasing filter and a second order sigma-delta modulator into a single chip to achieve high-resolution with low power and area consumption. Measurement results show that the system works well and in line with the simulations.

ACKNOWLEDGMENT

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TABLE I. BENCHMARK WITH THE STATE-OF-THE-ART

Parameter	**[8]**	**[9]**	**[10]**	**This Work**
Technology	0.15um	0.5um	0.13um	0.25um
Structure	With Gm-C	With Gm-C	With RC	With RC
Supply(V)	1.6	2.5	1.5	1.6
Area(mm^2)	1.02	0.567	0.2	0.032
Power(mW)	0.096	0.06	1.6	0.363
Bandwidth(Hz)	2000	10	1M	105
Samplilng Rate(KS/s)	320	20.48	37500	60
ENOB(bit)	10.34	13.67	9.6	14
SNDR(dB)	65.3	84.1	58.9	83.4
DR(dB)	68.2	80	60	94
FoM_S (dB)	141.4	132	147	148.6

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