A 0.011mm^2 60dB SNDR 100MS/s Reference Error Calibrated SAR ADC with 3pF Decoupling Capacitance for Reference Voltages

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Abstract - **This paper presents a calibration scheme for reference error caused by signal dependent switching transient in a high speed SAR ADC. The scheme has a little hardware overhead, which is not dependent on the type of the input signal and is able to run in the background without interrupting the ADC's normal operation. The calibration along with the SAR ADC are implemented in a 65 nm CMOS and the measurement results show that the proposed scheme effectively improves the SNDR of an 11b SAR ADC by ~9 dB. The calibration allows the placement of only 3 pF decoupling capacitance in the reference voltages. The prototype achieves 100 MS/s sampling rate with a total power consumption of 1.6 mW at a 1.2 V supply. Plus, it exhibits a 59.03 dB and 60.4 dB SNDR at Nyquist and low input frequency, respectively, yielding a Walden FoM@Nyquist of 21.9 fJ/conv.-step. The total core area is 0.011 mm^2 which includes the decoupling capacitor.**

I. INTRODUCTION

The SAR ADC has been adopted in a wide range of resolution and sampling rate specifications due to its well-known of excellent energy efficiency. Despite several practical issues directed the attention to the ADC's interface, such as the input buffer [1] and reference buffer [2][3], in terms of the particle realization of the SAR ADCs, it is still hard to maintain simultaneously a good energy efficiency in both the ADC core and interface circuitries. This paper focuses on the reference errors due to switching transients in SAR ADCs.

The Capacitive DAC (CDAC) is commonly used in SAR ADCs and its fully dynamic feature allows SA conversion exhibiting the best energy efficiency. As the SAR ADC relies on the CDAC to perform the binary-searched feedback, the advanced switching techniques [4][5] were explored to reduce the switching energy of the SA conversion, which indeed also relaxes the burden derived from the reference voltages. Several high speed SAR ADCs achieved excellent FoM, where supplies are adopted as the reference voltages [4][5]. This option provides low output impedance and maximizes the overdrive voltage of the switches thus benefiting the design at high speed. The low output impedance of the reference voltages can support fast recovery during the switching transient. Nevertheless, once the supply is shared with other circuit blocks (such as in the SoC), the interference can degrade the performance significantly and a better isolation is necessary. While, the supply voltage often contains a 60Hz noise which requires a LDO to suppress along with others low bandwidth noise.

Since the switching noise in a high speed SAR ADC is usually in the GHz range, a reference buffer is required to attenuate it in practice. However, such buffer implies a trade-off between the output impedance and the power consumption, to achieve a fast switching transient. Alternatively, a large number of decoupling capacitors (several Pico pF) is often introduced to suppress the switching noise as well as the ripple of the reference voltage, imposing large area if a deep-trend capacitor [6] is not available. In advanced deep submicron technology, a large decoupling capacitor occupying a large area is highly undesirable as the cost of the die area is extremely high.

In this paper, we demonstrate a calibration scheme for the conversion error caused by the reference ripple during the switching transient. The errors are detected and fixed in the digital domain. The detection circuit is embedded in the SA conversion and requires just a small modification of the conversional SAR ADC leading to less hardware overhead. The experimental results of a 65 nm CMOS prototype demonstrate the effectiveness of the proposed calibration method. The SNDR is improved from 49.89 dB to 59.03 dB at Nyquist and achieves up to 60.4 dB at a low frequency input. Benefiting from the calibration, only a 3 pF (6.8% of the total ADC area) decoupling capacitance is needed for the reference voltages, and the total power consumption is 1.6 mW at 100MS/s from a 1.2V supply. The Walden FoM is 21.9 fJ/conv.-step.

This research work was financially supported by Research Grants of University of Macau (MYRG2015-00088-AMSV) and Macao Science & Technology Development Fund (FDCT) with project code number FDCT/055/2012/A2.

II. ADC Architecture

The proposed reference error correction technique is demonstrated in a conventional 11b SAR ADC whose overall architecture is depicted in Fig. 1. It consists of a bootstrapped sample-and-hold front-end, a self-time loop, a capacitive DAC array, a comparator, a SAR controller and an adder for reference error correction. The SAR operation is similar to [5], which performs the binary-search approximation with V_{cm}-based switching. Two simple modifications of the ADC are made to enable the proposed calibration scheme. 1) The threshold of the comparator is configurable. 2) One extra cycle is inserted to detect the reference errors. The signals EN_Cal and $Cal_{P/N}$ indicate whether the calibration is triggered and the polarity of the error, respectively. Finally, the outputs pass through an adder to correct the error. The detail operation of these two modifications will be introduced in section IV.

As the switching of the leading bits cause larger reference ripples [3], their reference and settling errors are expected to be calibrated with the proposed scheme. The total array capacitance is 768 fF for matching consideration. A synchronous time loop with ~600 ps for each bit cycling is designed where the time allocation for the comparison and logic processing versus the DAC settling is set to be 3:2. Besides, an extra 30 Ω resistance is added between the off-chip references to the 3 pF decoupling capacitor to model the finite output impedance from the reference sources.

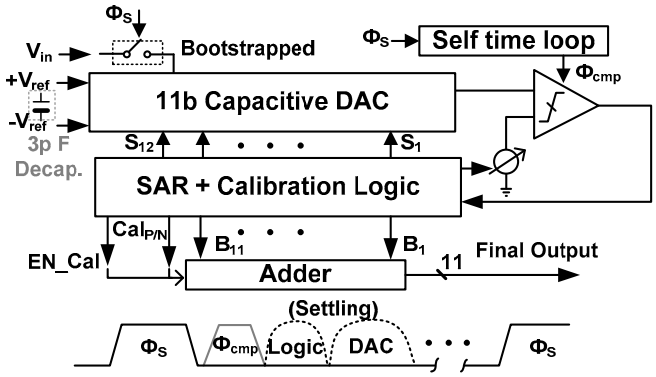

Fig.1. Overall ADC architecture.

III. Background and Proposed Calibration Scheme

A. Reference Ripple Error

Fig. 2 (a) indicates the switching energy corresponding to each output code in an 11b SAR ADC built with a binary-weighted DAC. As shown in Fig. 2 (b) the switching energy required for each bit cycling is code-dependent, therefore, the reference ripple due to the switching transient is signal-dependent. Obviously, the reference errors in leading bits can significantly affect the conversion accuracy, while the errors from the rest of the LSBs are comparatively relaxed. Since much smaller capacitors are charged or discharged, the reference error referred to the DAC's output is quite small and the recovery time can be much shorter.

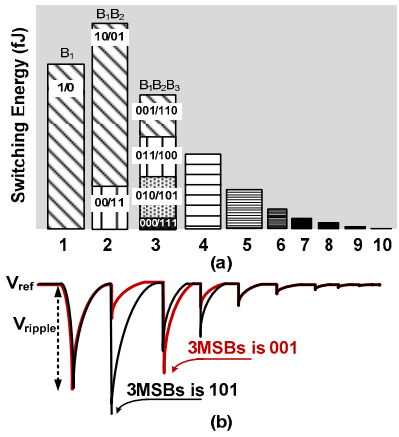

Fig. 2. (a) Switching energy v.s. digital outputs of an 11b SAR ADC. (b) Reference ripple during switching transients.

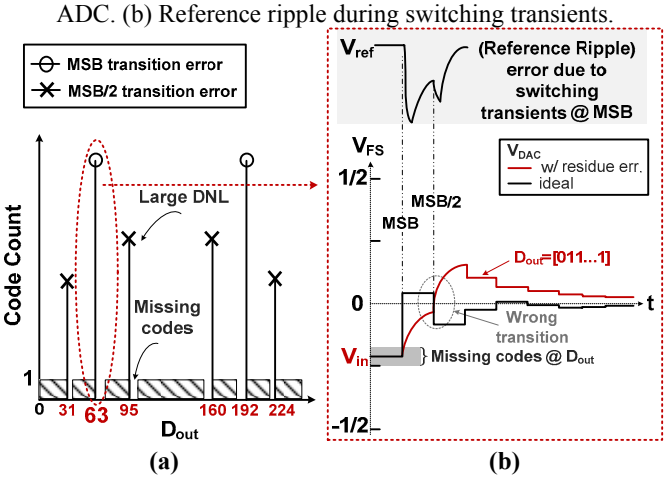

Fig. 3. (a) Code histogram of an 8b example with reference error. (b) Signal behavior of the DAC's output.

The code-histogram of an 8b example, including the reference errors from the first 2 leading bits, is plotted in Fig. 3 (a). There exists both bunch of missing codes and large hits at the digital outputs corresponding to the transition points of the MSB and MSB/2. The signal behavior of the DAC's output (V_{DAC}) during the successive approximation is also depicted in Fig. 3(b). Since V_{in} is smaller than the comparison threshold "0", the MSB is set to "0". Correspondingly, the MSB capacitor is charged to V_{ref} for the next bit comparison. As a large capacitance needs to be charged and the impedance of the V_{ref} node is not infinity, it causes a large reference ripple. Since this ripple cannot recover before the next comparison, it will result in a wrong transition as well as a comparison result error at MBS/2 at the given time. Ideally, the V_{DAC} should be smaller than the comparison threshold but due to previous decision error now V_{DAC} is still above "0", which leads to a decision on the rest of the bits to be all equal to "1" and V_{DAC} can never converge back to within 1/2 LSB of the comparison threshold. Due to the reference errors certain ranges of V_{in} have the same digital representative which explains why there is a large hit at D_{63} and some adjacent codes are missed. Such errors are not possible to be recovered by any post-signal processing scheme since the code at large hit cannot be separated to represent their corresponding sampled inputs. To correct the error in the digital

domain, error detection and some analog circuit modification are implemented that will be detailed in the next subsection.

B. Proposed Calibration Technique

The concept of the proposed reference error calibration scheme is depicted in Fig. 4 (a). If those large hits due to single dependent reference ripple can be separated, then by shifting them back to their corresponding digital outputs, the missing codes should be recovered. The code-separation can be easily implemented during the SAR conversion by inserting an additional error-detection step and a threshold level. As shown in Fig. 4 (b), the first 3b cycling performs the normal SAR conversion, and the 4th cycle (supplementary) is utilized to detect whether the final residue will cross the comparison threshold "0" or not. The operation can be realized by simply discharging the rest of the bits to V_{refn} and then performing the comparison. If $V_{DAC} > 0$ that indicates the reference error does affect the previous comparison, and the V_{DAC} will converge to a new threshold for the rest of the bit cycling. If $V_{DAC} < 0$, implying no occurrence of comparison error, the ADC resumes its normal conversion.

In order to detect both positive and negative reference ripple error, a complementary threshold V_{dn} and V_{dp} are required which can be easily accomplished in a differential operation by flipping the reference input polarity of the comparator. Besides, note that V_{dp} and V_{dn} do not need to be accurate or being match each other ($V_{dp} = -V_{dn}$), since its value only determines the error correction range. The sufficient design margin can guarantee the expected calibration accuracy. The correction range is

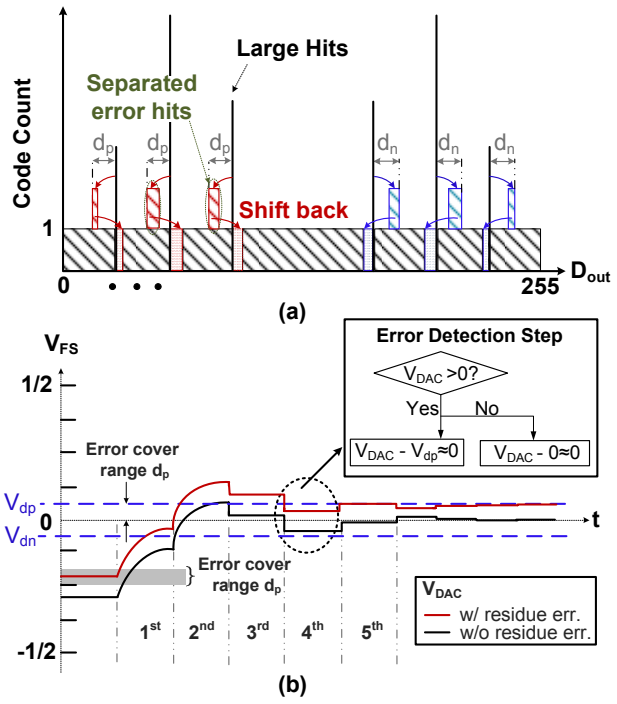

Fig. 4. Proposed calibration. (a) Calibration concept in output code histogram. (b) Signal behavior of the DAC's output during calibration.

correlated with the bit assigned for error detection. If the m^{th} bit is set as the error detection step, the maximum error covering range can be up to $1/2^{m-1}$% of the full-scale V_{FS}.

If a reference error is detected, the DAC will converge to a new threshold. Such output code has a constant offset between its ideal value. The code offset can be easily obtained by measuring the mean of the output code separately between the normal and the new threshold. Then a shifting operation can be done in the digital domain after obtaining the offset value. In order to implement the above functions, the ADC will simultaneously generate two signals for digital processing: 1) EN_Cal. to signalize whether the calibration is triggered. 2) $Cal_{P/N}$ to indicate the ripple error polarity.

C. Design Consideration

According to post-layout simulations the reference error limited the conversion SNDR to 50 dB and the maximum reference ripple is ~120mV (5% of V_{FS}). Therefore, the error-detection step is set at the 5th cycling that can tolerate 6.25% error of V_{FS}. The thresholds V_{dp} and V_{dn}, which are originally set as ±75 mV could vary about 15% under the Monte Carlo simulations. As mentioned before, the code-separation does not rely on the matching among the thresholds, which only affects the error coverage range. Once enough margin (larger than the error range in all conditions) is allowed to V_{dp} and V_{dn}, the reference error can be effectively corrected in the digital domain.

IV. Measurement Results

The proposed reference error calibration was implemented in an 11b 100MS/s SAR ADC fabricated in a 65 nm 1P7M digital CMOS process. Fig. 5 shows the die microphotograph; the active area is 0.011 mm^2 where the decoupling capacitors of the reference voltages only occupy 6.8% of the total area. Fig. 6 illustrates the output code histogram before and after calibration. Before calibration, there are large hits and gaps near the leading bit transition points. The maximum DNL and INL are 10 /-1 LSB and 6.39/-9.63 LSBs, respectively. After calibration, the glitches are removed as shown in Fig. 6 (b). The DNL and INL improved to 1.28 /-0.97 LSBs and 1.05/-0.84 LSBs, respectively. Measured FFTs plotted at near Nyquist input frequency with and without calibration are shown in Fig. 7. The SNDR before calibration is 49.89 dB, which is improved to 59.03 dB after calibration. The ADC performance is limited by the SNR which is caused by the small reference error during the LSBs cycling. Fig. 8 shows the measured dynamic performance across different input frequencies. The SNDR remained above 59 dB until the Nyquist input and the ERBW is higher than 65 MHz. The ADC achieves a SNDR of 60.4 dB at low frequency input (~ 20 MHz). Table I summarizes and compares the overall measured performance with state-of-the-art high speed and high resolution SAR ADCs. The total power consumption is 1.6 mW at 100 MS/s from a 1.2 V supply, where the analog and digital blocks consume 825 µW and 774 µW, respectively. This work exhibits a FoM of 21.9 fJ/conv.-step @Nyquist. Though the FoM of this work is not the best among the others, it is at 65 nm

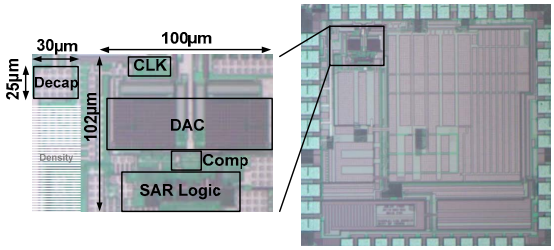

Fig.5. Die microphotograph of the ADC.

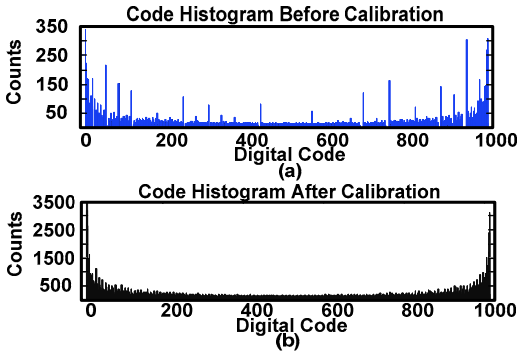

Fig.6. Measured ADC output code histogram (a) before calibration (b) after calibration.

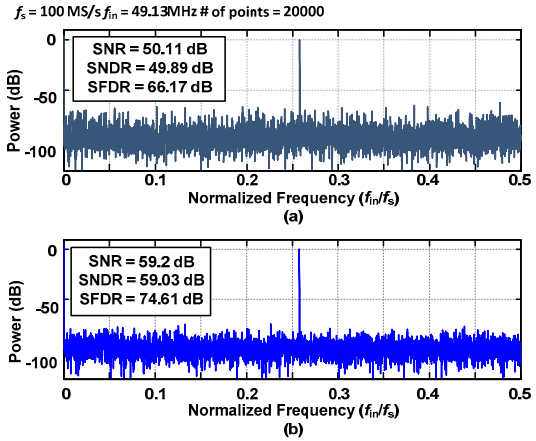

Fig.7: Measured spectrum output of ADC (decimated by25) (a) before calibration (b) after calibration.

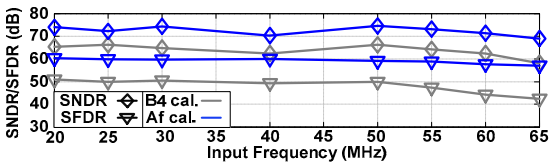

Fig.8. Measured SFDR & SNDR vs. input frequencies.

with only practical 3 pF decoupling capacitor in reference voltage. The reported area includes the decoupling capacitor.

V. Conclusions

This paper reports a reference error calibration for a conventional high speed and high resolution SAR ADC. The proposed solution relaxes the stringent transient requirement of reference voltages in SA operation which is usually traded with the placement of a large number of decoupling capacitances. Also, if a reference buffer is used, it is not necessary to provide low output impedance for fast transients. Thus, the buffer can be designed with low power dissipation. The calibration is simple to be implemented in SA operation and the error correction is an easy addition in the digital domain. The measured results demonstrate that the SNDR can be improved by ~9 dB in an 11b SAR ADC with only a 3 pF decoupling capacitor for reference thus leading to a small area of 0.011m^2.

TABLE I. SUMMARY OF PERFORMANCE AND BENCHMARK WITH STATE-OF-THE-ART

	ISSCC '10 [8]	ISSCC '12 [9]	A-SSCC '13 [2]	ISSCC '16 [7]	This work
Architecture	SAR	SAR	SAR	SAR	SAR
Technology (nm)	65	40	40	28	65
Resolution (bit)	10	10	10	12	11
Sampling Rate (MS/s)	100	80	50	100	100
Supply Voltage (V)	1.2	1.1	1.1	0.9	1.2
Power (mW)	1.13	5.54	0.47	0.35	1.6
ENOB @Nyquist	9	8.71	9.18	10.41	9.51
SFDR (db) @Nyquist	66.9	65.12	68.16	75.42	74.61
Area (mm^2)	0.026	0.08	0.0114	0.0047	0.011*
Decoupling (F)	N/A	N/A	N/A	N/A	3p
FoM @Nyq. (fJ/conv.step)	22	178	16	2.63	21.9

* including the decoupling capacitor for the reference voltages

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