A 21.4 MHz G_m-C Bandpass Filter in 0.8 μm Digital CMOS With On-chip Frequency and *Q*-factor Tuning

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Abstract: A G_m-C 4th order bandpass filter with on-chip automatic frequency and *Q*-factor tuning is realized in 0.8 μm digital CMOS. The filter operates at nominal 21.4 MHz center frequency but can also be tuned to cover the frequency range from 15 to 30 MHz. It occupies 0.48 mm^2, and at 5 V supply it dissipates 15 mW, achieves 62 dB signal-to-noise ratio in the passband, –43 dB intermodulation distortion and a 3rd order intercept point of 24 dBm for a 3 Vpp input overdrive signal.

1. Introduction

High-frequency continuous-time filters employing ladder-based Gm-C structures are often used in radiocommunication applications [1]. However, because of the large tolerances of the basic elements (g_m's and C's) as well as the parasitic effects that adversely affect the filter *Q*-factor, an automatic tuning scheme must be implemented on-chip as part of the complete filter system. Various solutions have been reported for automatic tuning of continuous-time filters, e.g. [2-8]. Some of the most popular are based on the master-slave approach which allows the filter to operate continuously but which can only be as accurate as the achievable matching of the circuit components across the silicon chip. Here, we employ instead a direct tuning system based on the successive approximation algorithm to correct both frequency and *Q*-factor related errors [9]. While frequency tuning is carried-out against a precise external reference signal, *Q*-factor tuning is accomplished by a simple peak detection mechanism. The complete tunable filter system has been realized in a 0.8 μm digital CMOS process. Experimental results demonstrate the performance of the system at nominal 21.4 MHz center frequency as well as within the full tunable range from 15 to 30 MHz.

2. Filter Architecture

The implementation of the 4th order Butterworth bandpass filter is based on the G_m-C simulation of a doubly terminated coupled resonator LC ladder prototype filter. Two capacitively coupled resonators have identical capacitance and inductance values and hence their resonant frequency is the same. Inductors are simulated using gyrators formed by two equal-valued transconductors with negative feedback and $L = C/g_m$, whereas the termination resistors are realized by transconductors with direct input-output connection and $R = 1/g_m$. The G_m-C structure is given in Fig. 1. Simple differential pairs with folded cascode output stages are used for implementing the transconductors with acceptable linearity-speed trade-off [10]. The transconductors that simulate the inductors and terminating resistors are biased separately for allowing, respectively, independent frequency and *Q*-factor tuning. Capacitors are formed by associations of metal-poly unit capacitors for digital process compatibility.

3. Tuning System

Frequency Tuning: Center frequency tuning is carried-out by adjusting, one at a time, the two grounded resonators with identical resonant frequency. For this purpose each single resonator is first isolated from the filter and then the appropriate transconductance values are adjusted through the DC bias currents of the differential pairs. The circuit that generates and corrects the center frequency errors is based on the mixed analog-digital frequency-locked loop schematically illustrated in Fig. 2. The successive approximation control circuit of the loop updates the digital input of the current DAC and which, in turn, changes the bias

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control circuit of the loop updates the digital input of the current DAC and which, in turn, changes the bias current of the transconductors to bring the phase error signal within the required limits. Once the filter tuning has been completed the final digital word applied to the DAC is kept in a simple memory RAM and the reference frequency is disconnected from the filter input. The final adjusted resonant frequency may deviate from the nominal frequency mainly due to the flip-flop settling time and comparators offset. This can be as low as ±0.05% and represents a good trade-off between the filter tuning precision and the complexity of the auxiliary tuning circuitry.

Q-factor Tuning: The filter Q-factor is strongly dependent on parasitic elements and phase shifts associated with the transconductors. First, the non-zero conductance, g_o, at the output of each transconductance causes the Q-factor of the simulated inductor to be one half of the DC gain of the transconductors used in the gyrator. In the present design the transconductors have nominal values of $g_m = 647$ S and $g_o = 1.75$ S which correspond to an equivalent Q-factor of only 185 for the simulated inductor. More important is the effect of high-frequency phase shifts due to the internal poles of the transconductors. Assuming that each of the two transconductors of the gyrator have a small phase lag $e^{-j\phi}$, then at the nominal 21.4 MHz center frequency this yields a parallel negative resistance [10]. To cancel out this effect a positive resistance R_{comp}, simulated also by an OTA, is placed in parallel with the gyrator. Therefore, the correct value of Q is obtained by adjusting R_{comp} such that the parasitic equivalent negative resistance is canceled and the nominal value of R_S is also adequately corrected. During center frequency tuning this compensation OTA must simulate, by default, a constant and small enough positive resistor to guarantee the stability of the resonator.

The auxiliary circuit for Q-factor tuning, conceptually similar to the circuit for center frequency tuning, comprises two peak detectors and one comparator. The two peak detectors provide the necessary amplitude measurements for the input and output signals, whereas the comparator provides the error signal used to control, again by successive approximations, the bias current of the OTA which simulates the compensating resistor.

Tuning Circuits: The complete filter and tuning system is represented by the simplified block diagram of Fig. 3. The comparators used for squaring sinusoidal signals during frequency tuning and for comparing the rectified amplitude voltage during Q-factor tuning are based on a simple differential pair optimally designed to operate within the filter frequency range up to 30 MHz and resolve signal levels as low as 10 mV corresponding to a gain of –34 dB with respect to the nominal 500 mV amplitude. This latter condition is necessary because during frequency tuning the gain of the filter at the nominal center frequency may be quite low until the Q-factor is properly adjusted.

For implementation of the peak detectors at 30 MHz a VHF full-wave rectifier with low pass filtering is employed, consisting of a simple differential pair with the common source loaded with a capacitor of few pF [5]. This is formed by the gate to substrate capacitance of an MOS transistor which has much higher capacitance density than the metal-poly capacitor structures available in digital CMOS. Despite its reduced linear operating range this is good enough for amplitude rectification in this specific application.

Two equal 7-bit DACs are used for adjusting the bias currents of the transconductors according to the tuning algorithm. It is based on a compact segmented architecture with maximum transistor ratio of 1:16. One such current DAC is used for center frequency tuning while the other is used for Q-factor tuning. The currents range from 6 μA to 24 μA giving an incremental resolution of 0.14 μA.

The controller employs a sequence detector which defines the sequential steps for center frequency tuning (firstly) and then Q-factor tuning. It reads the output from the counter decoder, detects the single initial state as the start or stop for the center frequency tuning and Q-factor tuning, and then generates the corresponding control signals for the complete tuning system. This includes isolating a single resonator during center frequency tuning, (re)connecting the two resonators during Q-factor tuning, and disconnecting the reference signal from the filter input upon completion of the full tuning cycle. A switch-tail ring counter activates the 7 bits, starting from the MSB down to the LSB, for the phase and amplitude

comparison used, respectively, for center frequency and Q-factor tuning. This has the advantage of changing only one bit at a time and thus requiring a rather simple decoder.

4. IC Implementation and Results

The complete filter and tuning system has been integrated in a 0.8 μm single-poly CMOS technology. An additional filter section, without tuning, together with the auxiliary current DAC and phase and amplitude-detection blocks are also implemented separately on-chip for testability purposes. The chip microphotograph is shown in Fig. 4. The main filter and automatic tuning system are seen in the bottom-half of the chip whereas the upper-half contains the various sub-circuits, including a resonator filter section, for independent testing and characterization. The active area of the complete filter and tuning system is 0.45 mm^2, 55% of which is taken up by the poly-metal capacitors. The area occupied by the tuning system alone, including the digital control section, is merely 0.125 mm^2 which indicates its suitability for realizing self-tunable integrated filter systems with little overhead costs for tuning.

The overall amplitude response of the filter after tuning is shown in Fig. 5. The measured center frequency at 21.394 MHz is within ±0.014% of its nominal value of 21.4 MHz whereas the –3 dB bandwidth of 750 kHz indicates a deviation of about 5% from the nominal value of 715 kHz. At the nominal center frequency of 21.4 MHz the filter guarantees a minimum of 50 dB attenuation above 28 MHz and below 18 MHz. The tunability operation of the filter is demonstrated in Fig. 6, showing the detailed passband responses for the untuned filter (curve A), the nominal filter tuned at 21.4 MHz (curve B), and the filter tuned at 15 MHz (curve C) and at 30 MHz (curve D), respectively corresponding to the lower and higher frequencies of the specified tunability range. By continuously varying from 300 mV to 5 V peak to peak the amplitudes of two test tones at frequency $f_1 = 21.3$ MHz and $f_2 = 21.5$ MHz, we obtained the measured power of the input, output, and the 3rd order intermodulation products yielding an IP3 of +24 dBm relative to a 50 Ω resistance. Other experimental results that illustrate the performance of the filtering system are summarized in Table I.

5. Conclusions

This paper described a 21.4 MHz G_m-C bandpass filter system with on-chip automatic frequency and Q-factor tuning. Integrated in a 0.8 μm CMOS digital technology the complete system occupies an area of 0.48 mm^2. At 5 V supply it dissipates 15 mW, achieves 62 dB signal-to-noise ratio in the passband and exhibits –43 dB intermodulation distortion and IP3 of +23 dBm, referred to 50 Ω.

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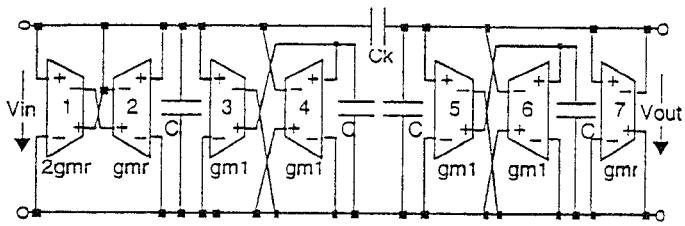

Fig. 1. G_m-C bandpass filter structure.

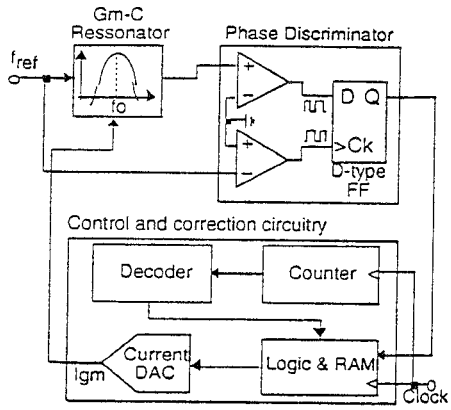

Fig. 2. Mixed analog-digital loop for center frequency tuning by successive approximations.

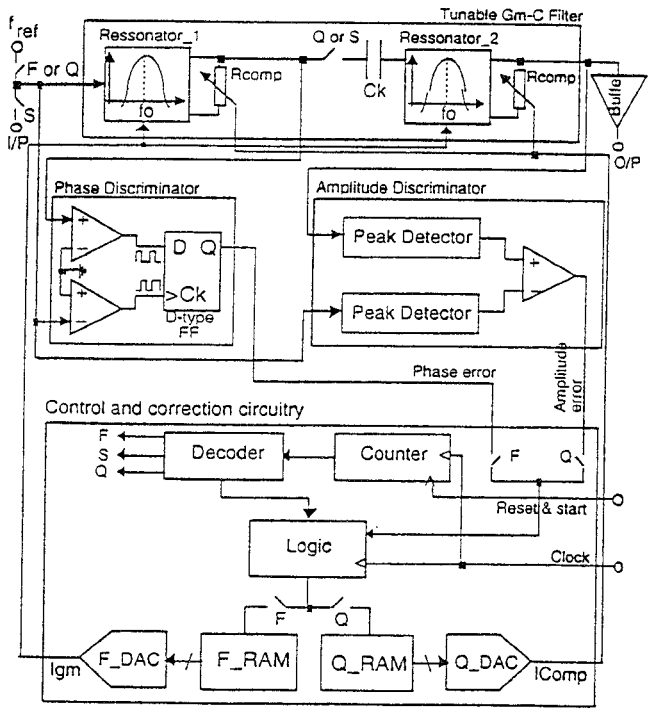

Fig. 3. Simplified block diagram of the tunable G_m-C filter system.

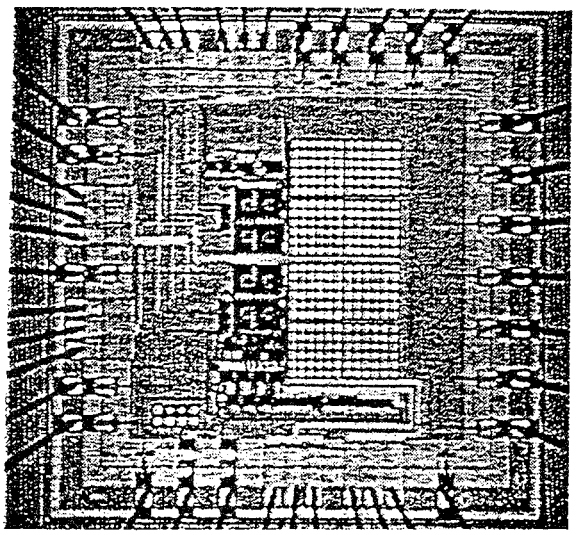

Fig. 5. Microphotograph of the 0.8 μm CMOS prototype chip.

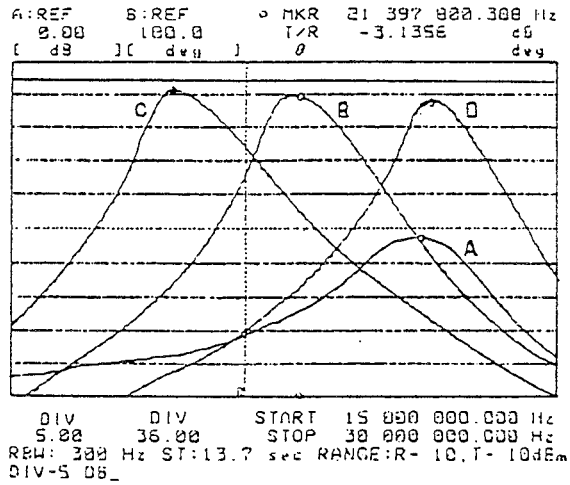

Fig. 6. Filter tunability in the frequency range from 15 to 30 MHz.

Active Area of Test Chip	0.8 mm^2	Passband SNR	62 dB
Area of Tunable Filter System Alone	0.45 mm^2	Passband PSRR	–53 dB
Center Frequency	21.397 MHz	Output Voltage Swing (linear range)	1.4 Vpp
–3 dB Bandwidth	750 kHz	Power Dissipation @ 5 V	15 mW
Passband Gain	> –3 dB	Center Frequency Tuning Range	15 – 30 MHz
Quality Factor @ 21.4 MHz	28.5	Quality Factor Tuning Range	5 – 30
Stopband Attenuation at f < 18 MHz or f > 28 MHz	–50 dB	Intermodulation Distortion at 0.7 V single-tone amplitude	–43 dB
Startup Tuning Time	3.6 msec @ 30 kHz Clk	IP3	23 dBm @ 3 Vpp

Table I. Measured characteristics of the G_m-C bandpass filter system.