A High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller

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***Abstract*—This paper presents a 4-channel power electronics (PE) controller front-end interface with input signal conditioning and analog-to-digital (A/D) conversion functions for different power electronics system applications. The proposed front-end is composed of a 4-channel continuous-time (CT) and discrete-time (DT) hybrid sigma-delta modulator (H-ΣΔM) embedding an input programmable-gain (PGA) in the first CT stage in order to enhance the input dynamic range (DR). The second shared DT stage is designed to utilize multiple-sampling technique with a shared single Op-Amp for low power consumption. This PE controller front-end chip is fabricated with 65 nm CMOS technology. Measurement results show a high dynamic range of 98.3 dB and 84.2 dB SNDR, while achieving a power consumption of 68 µW per channel and a FoMs of 172-179 dB due to the dynamic range boost.**

Keywords—multi-channel sigma delta front-end interface; programmable-gain; integrated PE controller

I. INTRODUCTION

In modern power electronics (PE) systems such as: power quality (PQ) compensators, uninterruptible power supplies (UPS), electric vehicle (EV) charging systems, motor drivers, air conditioning (AC) systems, renewable energy conversion systems, etc. they all require a digital controller like a microprocessor, a digital signal processor (DSP), a field programmable gate array (FPGA), etc. to control on/off of the power electronics switches for the purpose of performing their corresponding functionalities. The large electrical signals of the power electronics systems are converted into small analog signals through voltage or current transducers. Then, a signal conditioning circuit and an analog-to-digital (A/D) converter is required in order to adapt to the input voltage range of the digital controller, for further processing the digitalized input signals and perform corresponding control for different power electronics system applications as shown in Fig. 1.

Conventionally, the design of digital controllers is usually based on full input range conditions to avoid analog signal saturation. Unfortunately, in weak sensing input conditions (e.g. light or medium load current conditions in the power electronics side), the digital controller may suffer from a low resolution problem due to the small dynamic range necessary to detect the weak voltage/current, which significantly affects the control system performance. In addition, the signal conditioning circuit (separated printed circuit boards (PCBs) of voltage/current detection), analog-to-digital (A/D) converter and digital controller are usually implemented with multi-PCB boards that occupy a significant estate of the overall controller space. Such discrete PCB level implementation also brings up significant delay in the feedback loop which will affect the loop stability and also the controller performance.

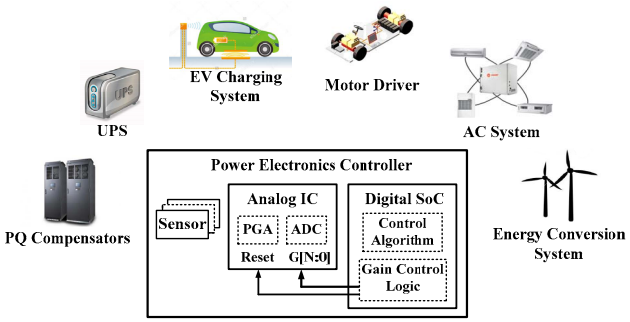

Fig. 1 Integrated PE controller block diagram

In this work, we propose an analog PE controller front-end integrated circuit (IC) with the functions of input signal conditioning, gain programmability and analog-to-digital (A/D) conversion which can substitute the discrete signal conditioning boards and A/D converters for extending the operational range and enhancing the performance of power electronics systems. The proposed front-end is realized with a multi-channel CT/DT hybrid stage-shared ΣΔ modulator. A programmable gain function is embedded inside the first CT stage to achieve a dynamic range (DR) extension. The CT implementation also allows the removal of multi-channel anti-aliasing filter front-ends which are bulky in the traditional controller implemented by discrete components in a multi-PCB level. The second shared DT stage is designed utilizing a multiple-sampling technique with a shared single Op-Amp for the sake of low power consumption. This design achieves not only low power, but also minimizes the area, allowing high input DR and reducing the circuit complexity. Besides, this IC implementation opens the door for the miniaturization of the overall PE controller, reducing its signal processing delay and improving the controlling performance. Moreover, this PE controller front-end IC is generalizable and can be applied to many different PE systems.

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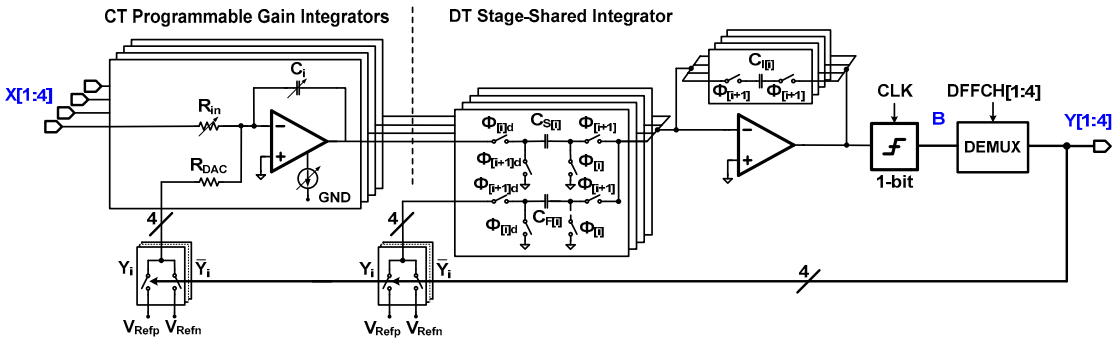


Fig. 2 The proposed multi-channel CT/DT hybrid stage-shared H-ΣΔM

II. System-Level Architecture

A. Integrated Power Electronics (PE) Controller Front-End

A power quality compensator is chosen as an application example for the proposed PE controller front end. Fig. 1 shows an integrated mixed signal PE controller block diagram for controlling the hybrid active power filter (HAPF) for power quality compensation, which is composed of the analog signal conditioning circuit with programmable gain and A/D converter, and the digital control part with a digital SoC. The PE controller implemented in [1] is obtained with many discrete components in a PCB level, which are quite bulky. Here, the analog front-end part that includes the multi-channel anti-aliasing, the programmable gain and ADCs are implemented by the proposed CT/DT hybrid multi-channel ΣΔ ADC as described below.

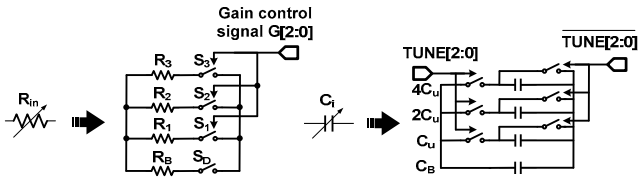
B. Modulator Design Considerations

As referred in [1], a power electronics system requires a 13-bit ADC with 25 KHz bandwidth (for signals detection and PWM) for compensating the voltage and current harmonic distortion to satisfy the international standards [2]. Among various ADCs, the ΣΔ ADC is best known as a power-efficient ADC when low bandwidth with more than 12-bit resolution is required. However, a conventional DT ΣΔM needs higher Op-Amp gain-bandwidth product (GBW) requirements than its CT counterpart, since the settling error of a CT integrator is smaller than a DT integrator [3]. Also, the DT ΣΔM needs a front-end anti-aliasing filter that constitutes another important disadvantage to the overall size of the controller. Alternatively, a CT ΣΔM can be used to reduce power consumption avoiding the anti-aliasing filtering. Then, 4 Channels with CT integrators in the front-end are still necessary, to eliminate switches which otherwise will create aliasing and destroy the anti-aliasing operation of the CT front-end. This hybrid ΣΔM structure combines the initial 4-channel CT integrators and subsequent single shared DT integrator in the loop filter, which offers several important merits when compared with the conventional ΣΔM using only DT loop filters. First, since there is no front-end sampling of the input voltage, signal-dependent clock-feedthrough, charge-injection and aliasing do not exist in the first stage. Second, the CT integrator can average out any signal-dependent glitches coupled into the input of the modulator over the clock period, which greatly reduces the harmonic distortion due to coupling. Third, the input impedance of the first integrator is purely resistive, thereby no electromagnetic interference (EMI) is emitted back to the input pins. Last, the implicit anti-alias filtering (AAF) property of the first CT stage can filter out-of-band-information from the input signal. In addition, further considerations about the die area create a strong motivation to achieve a multi-channel modulator on a single chip to minimize the per-channel area.

III. Circuit Design

A. Proposed Multi-Channel Hybrid Stage-Shared Modulator

Fig. 2 exhibits the proposed multi-channel CT/DT hybrid stage-shared ΣΔM prototype mainly comprising 4 channels of CT integrator in the first stage, a shared second DT stage, a shared single-bit quantizer, a demultiplexer and a 4-phase clock generator. A fully differential architecture is used to reduce the crosstalk and improve the noise performance. The first stage contains 4 parallel channels with CT integrators each of which contains a resistor bank (Fig. 3a) for the implementation of the digitally programmable gain function, and a capacitor bank (Fig. 3b) for tuning the RC time constant that might change with process and temperature variations. The capacitor bank is in the feedback loop, so its value will also affect the noise-shaping performance, which is the reason we choose it just to adapt the PVT variation (+/- 25%). On the other hand, the resistor bank is not in the feedback loop, so we choose this bank (with resistor value changes from 1x to 8x) to implement the gain programmability which will not affect the noise shaping filter when the gain is under programming. The CT front-ends also provide the inherited anti-aliasing function. In the DAC feedback path, excellent linearity can be achieved using a single-bit DAC in combination with nonreturn-to-zero pulses. In the shared DT second-stage, there are 4 sampling capacitors that are used for time interleaving and 4 integration capacitors that are switched subsequently over the 4 phases in order to keep intact the individual channel information. The timing diagram is shown in Fig. 4. For the shared second stage, when one channel is sampling, simultaneously, the other channel is integrating, thereby the quantizer can update the new code in each phase. The memory effect of the Op-Amp does not constitute a significant disadvantage if its input parasitic capacitance is small and the gain is high enough, besides, the 1st stage integrator can also contribute to shape this error. The stage-shared DT integrator requires four 10 MHz clock phases that have a 25% duty cycle generated by a 4-phase clock generator. The modulator digitalizes 4-channel input signals in serial single-bit streams that are packaged into data packets bit by bit and are transmitted in series into the demultiplexer. Each data packet carries one bit of data from



(a) (b)

Fig. 3 (a) Input resistor array for gain programmability
(b) RC time constant tuning capacitor array

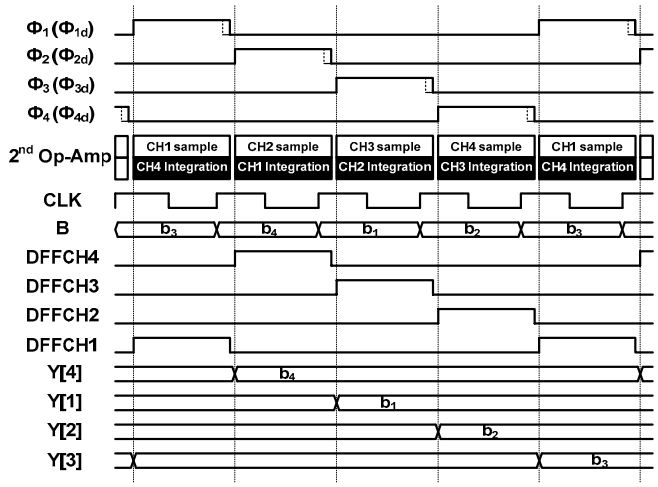


Fig. 4 Timing diagram of the proposed modulator

each channel (b1-b4) as shown in Fig. 4. The demultiplexed 4 channel outputs are fed-back to drive the DACs of the modulator.

B. Programmable Gain Front-End

The input-output gain programmability has been mapped onto switchable binary weighted resistor arrays, as shown in Fig. 3a. A 3-bit gain control bus G[2:0] establishes the gain range for the PGA. Depending on the amplitude of the input signal, the gain is switchable from 1x to 8x. If G > 1 this means that a smaller R_{in} than in the typical situation (with G = 1) is required in order to keep the same current input to the modulator. Furthermore, since the OTA equivalent load also increases, the bias current of the first OTA is also scaled accordingly, plus, the power consumption of the ΣΔM is adjusted efficiently for the corresponding gain requirement.

Considering the ON-resistances R_{SD}, R_{S1}, R_{S2}, R_{S3} of the switches, it is possible to affect the gain of the active RC integrator thus causing a gain error. The transfer function of the active RC integrator can be expressed as,

$$H(s) = \frac{1}{s \cdot C} \cdot \left(\frac{1}{R_B + R_{SD}} + \frac{G[0]}{R_1 + R_{S1}} + \frac{G[1]}{R_2 + R_{S2}} + \frac{G[2]}{R_3 + R_{S3}} \right) \quad (1)$$

When the switches S_1 to S_3 are turned on, the gain control signals G[2:0] have a value '1'. When the switches are turned off, the G[2:0] have a value '0'. We can deduct from (1) that, the resistors R_1 to R_3 need to have higher values than the ON-resistances of the switches in order to minimize the gain error. Here, we add a dummy switch that keep turning on beside the base resistor R_B and keep the size ratio of the switches S_3, S_2, S_1 and S_D as the same as the resistance ratio R_3, R_2, R_1 and R_B. Thereby, the gain of the active RC integrator can be controlled accurately in response to the 3-bit gain control signals G[2:0].

Regarding the resistors' thermal noise contribution in the first active-RC integrator, both the input signal and the DAC feedback signal paths are considered. Each resistor has an equivalent noise source whose single-sided power spectral density (PSD) can be represented as,

$$S_R = 4kTR \quad (2)$$

where k is Boltzmann's constant and T is the absolute temperature. Without considering the amplifier noise, the input-referred thermal noise PSD yields [4]

$$S_{noise,in}(f) \approx 2\left(S_{R_{in}} + S_{R_{DAC}} \frac{R_{in}^2}{R_{DAC}^2} \right) \quad (3)$$

where the factor 2 before the brackets accounts for the actual fully-differential implementation of the CT integrator. Replacing (2) in (3), the total input-referred noise PSD of the front-end integrator of the CT-ΣΔM can be approximated by,

$$S_{noise,in}(f) \approx 8kT\left(R_{in} + R_{DAC} \frac{R_{in}^2}{R_{DAC}^2} \right) \quad (4)$$

The input-referred in-band noise power (IBN) due to thermal noise can be easily obtained by integrating (4) over the input signal bandwidth, yielding,

$$IBN_{noise} = \int_0^{B_W} S_{noise,in}(f)df \approx 8kTB_W\left(R_{in} + R_{DAC} \frac{R_{in}^2}{R_{DAC}^2} \right) \quad (5)$$

For the lowest gain setting (G = 1), we assume that $R_{in} = R_{DAC} = R$. The IBN due to the thermal noise can be expressed as,

$$IBN_{noise,G=1} \approx 16kTB_W R \quad (6)$$

For large gains (G > 1), $R_{in} = R/G$ and $R_{DAC} = R$ is required. In this way the input is amplified but simultaneously the noise contribution of the input resistor is reduced. The IBN after programmable gain amplifying can be represented by,

$$IBN_{noise,G>1} \approx 16kTB_W R \cdot \frac{G+1}{2 \cdot G} \quad (7)$$

Moreover, the factor (G+1)/2G is always smaller than 1 owing to G > 1. As an example G = 8, the input is amplified by 8x times (~18dB gain), while the noise factor is reduced to (G+1)/2G = 9/16 = ~ -5dB, which will boost the dynamic range by 23 dB. This happens by considering only resistors' thermal noise contribution, other circuit non-idealities will also limit the boost but the above results are still significant as demonstrated by the measured dynamic range presented next.

IV. Measurement Results

The proposed 4-channel CT/DT hybrid stage-shared sigma delta modulator, including a gain programmability function and 4-phase clock generation, was fabricated in a 1P7M 65 nm CMOS process (Fig. 5), and occupies an active chip area of 0.03 mm^2 per channel. The measured spectra with a 4.8 KHz sinusoidal signal at around −2 dBFS input magnitude is shown in Fig. 6a, with the PGA not activated, and Fig. 6b, with it activated. The modulator achieves 84.2 dB peak SNDR and 95

dB spurious-free DR (SFDR) for a signal bandwidth of 25 KHz and a sampling clock rate of 10 MHz.

The measured SNDR versus various amplitudes of the input signal with typical cases of the programmable gain is shown in Fig. 7. The SNDR peak moves to the left as the front-end gain increases. As expected, the proposed modulator provides a DR of 86.2 dB (14-bit) for G = 1, which is boosted by the programmable gain function to a DR of 98.3 dB (16-bit). To verify the effectiveness of the multi-channel technique, the crosstalk between channels is measured by applying two sinusoidal input signals at around −2 dBFS magnitude to channel 1 and channel 2 with 4.8 KHz and 2.2 KHz, respectively. The crosstalk was measured to be around -98 dB as shown in Fig. 8. Powered by a 1 V supply the modulator only consumes 68 µW at G = 1 and 356 µW at G = 8 per channel, resulting in an overall FoM_S of 172–179 dB. Table I summarizes the measured performance and the comparison with some recently reported works and the key advantages of ours are underlined.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	This work	**[5]**	**[6]**	**[7]**	**[8]**
Process [nm]	65	65	65	130	350
Architecture	**Hybrid (CT/DT) embedded PGA**	CT	Separated PGA + DT	Separated PGA + CT	Separated PGA + CT
Gain range	0 to 18 dB	0 dB	0, 12 dB	20, 40 dB	20, 40 dB
B_W [KHz]	25	24	10	10	10
DR [dB]	86.2 @ G=0 dB 98.3 @ G=18 dB	88	78.5 @ G=0 dB 92.8 @ G=12 dB	96 @ G=20 dB 106 @ G=40 dB	76.4 @ G=20 dB 95.7 @ G=40 dB
SNDR [dB]	**84.2 @ G=0 dB**	85	77	76	49.6
Power/Ch. [µW][a]	**68 @ G=0 dB**	121	71.6	234	1900
FoM_W [fJ/conv.][b]	**102.6 @ G=0 dB**	173	618.7	2269	38502
FoM_S [dB][c]	**172 @ G=0 dB 179 @ G=18 dB**	171	159.9 @ G=0 dB 174.2 @ G=12 dB	172.3 @ G=20 dB 182.3 @ G=40 dB	143.6 @ G=20 dB 162.9 @ G=40 dB
Area/Ch. [mm^2]	**0.03**	0.6	0.34	2.3	0.4

[a] The performance of power include the PGA power.

[b] $FoM_W = Power/(2 \cdot B_W \cdot 2^{ENOB})$, where ENOB = (SNDR-1.76)/6.02.

[c] $FoM_S = DR+10 \cdot \log_{10}(B_W/Power^*)$, where Power* is the average power of various gains situation.

V. CONCLUSIONS

This paper presented an integrated power electronics controller front-end circuit, which was based on digitizing sensor analog output using a proposed multi-channel stage-shared CT/DT H-ΣΔM technique with gain programmability function. The main advantages of the proposed approach over the traditional DT system are the savings in power and silicon area. Experimental results show that the dynamic range can be highly enhanced by the action of gain programmability.

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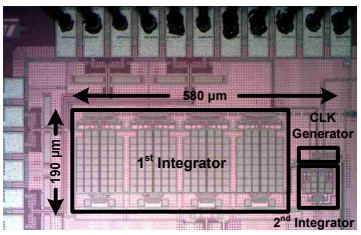
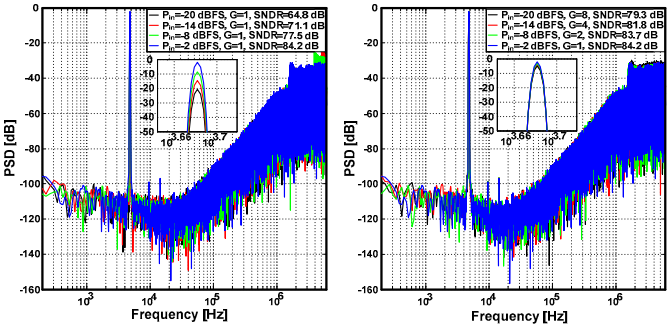


Fig. 5 Die microphotograph



(a) (b)

Fig. 6 Measured output spectrum in 4 different input amplitude (a) with PGA (G=1x); (b) with PGA (G=1x to 8x)

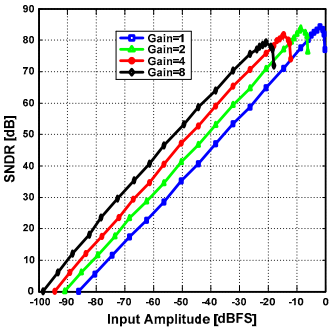


Fig. 7 Measured SNDR versus input signal in four PGA gain settings

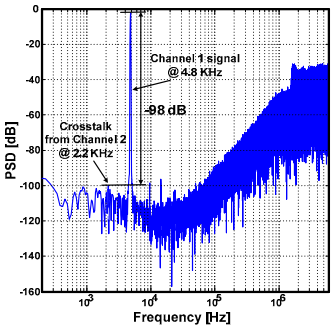


Fig. 8 Crosstalk performance between two channels

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