A Digital LDO with Transient Enhancement and Limit Cycle Oscillation Reduction

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***Abstract*—A digital low dropout regulator (D-LDO) manages to operate at low voltage and scale with process. But, the tradeoff between current efficiency and transient response speed limits its applications. In this work, a coarse-fine-tuning technique with burst-mode operation is employed to advance this trade-off. Once the output voltage under/overshoot is detected, the power MOS array changes with ×16 unit size at 500 MHz sampling frequency for a fixed time, comparing with ×1 size and 50 MHz in steady state. The limit cycle oscillation (LCO) in steady state is reduced by a feed-forward compensation zero with negligible power and area overheads. The proposed D-LDO is simulated in a 65 nm CMOS process, achieving a 60 mV voltage undershoot and 0.36 ps FOM of speed with a 60 μA quiescent current, and mode-1 LCO in steady state.**

Keywords—Low dropout regulator (LDO); digital control; coarse-fine-tuning (CFT); burst-mode; limit cycle oscillation (LCO); feed-forward path; compensation zero.

I. INTRODUCTION

The analog LDOs can achieve fast transient response and good ripple immunity at high input voltages, e.g. 1.2 V [1], [2], while the digital LDO (D-LDO), firstly brought out in [3], recently draws significant attention for its low-input voltage and process scalability. As shown in Fig. 1, a conventional D-LDO consisting of a comparator, a serial-in parallel-out bi-directional shift register (S/R), and a PMOS array acting as the power transistors. The comparator is used to sense the difference between the output voltage V_{OUT} and the reference voltage V_{REF}, while the S/R plays the role of an integrator to minimize the loop steady-state error. Since only one power MOS can be turned on/off per clock cycle for a typical S/R operation, the transient response can only be accelerated by a higher sampling frequency F_S. Nevertheless, this will inevitably undermine the steady-state power consumption.

Several previous works have been proposed to tackle this issue, which can be categorized into two schemes: asynchronous and synchronous. 1) The asynchronous schemes ([4] and [5]) manage to advance this trade-off, but the inherent sensitivity to PVT variations limits its applications [6]. 2) The synchronous schemes ([7]–[9]) demonstrate improved transient speed, with multiple counting per step and dynanic sampling frequency. And the quescient current is ensured by lowering F_S at the steady state. But the low F_S operation results in a longer charging/discharging on the output capacitor C_{OUT} once an inherent ripple exists on the control word *WORD*. This ripple is known as limit cycle oscillation (LCO), and incites large, unfavorable output voltage V_{OUT} variation. Therefore, it is necessary to achieve fast transient, high current efficiency and low LCO simultaneously.

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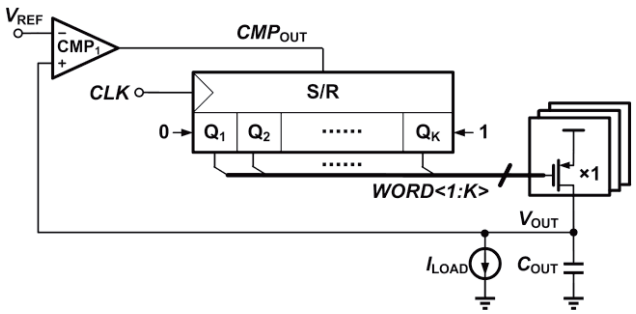

Fig. 1. Simplified schematic of the conventional S/R based D-LDO.

In this work, a D-LDO with coarse-fine tuning (CFT) and burst-mode techniques has been used for fast transient response and low quiescent current. And a feed-forward path is proposed for LCO reduction. This paper is organized as follows. The principles of the proposed techniques are discussed in Section II. Then, the circuit implementations and simulation results are given in Section III, and a conclusion is drawn in Section IV.

II. OPERATION PRINCIPLES

A. Coarse-fine-tuning (CFT) D-LDO

The simplified schematic of the proposed CFT D-LDO is shown in Fig. 2. The PMOS array is divided into the coarse and fine sections, where the unit in the coarse section provides N times strength of that in the fine one. These two sections are controlled by independent S/Rs, with the control words *CRS* and *FINE* indicating the respective numbers of PMOS to be turned off. The combined control word *CMB* is thus defined as:

$$CMB = N \times CRS + FINE \,. \tag{1}$$

The operation principle of this CFT D-LDO is depicted in Fig. 3. In steady state, the D-LDO works at the fine-tuning mode, with ×1 counting per step and low F_S (the gray curves). When V_{OUT} exceeds under/overshoot detection boundaries (V_{REF_H} and V_{REF_L}) under certain disturbances, the coarse-tuning will be triggered, where the coarse section takes over the D-LDO with *FINE* held constant. In this scenario, the ×N

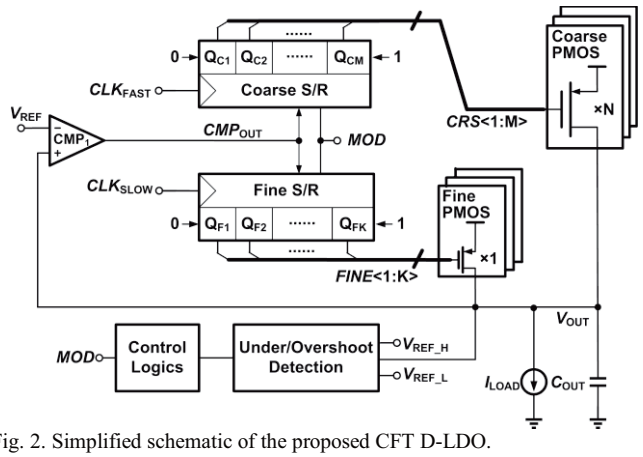

Fig. 2. Simplified schematic of the proposed CFT D-LDO.

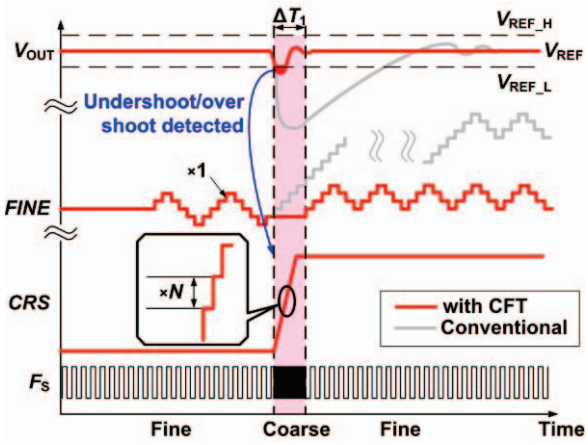

Fig. 3. Illustration of the transient response of the proposed CFT D-LDO.

counting per step in each clock cycle boosts the open loop gain of the D-LDO, allowing it to be quickly regulated to a nearby *CMB* desired. For further improvement, a higher F_S is employed in the coarse-tuning as well. After that, for higher accuracy and lower power consumption, the coarse-tuning is disabled while the fine-tuning is re-activated to regulate the D-LDO to V_{REF} with the exact desired *CMB*. Here the coarse-tuning will only last for fixed ΔT_1 duration, regarded as a burst-mode operation.

B. LCO reduction

Once the counting operation is kept active in steady state, LCO exists due to the inherent quantization error. In previous works, LCO could be eliminated by deactivating the counting operation in steady state, e.g. by adding a dead-zone to the comparator [10]. However, this will prevent an instant V_{OUT} detection, and also reduce the output accuracy. In [4], an external freeze signal is used for the deactivation, which may increase the design complexity. To advance this, we propose a technique without the deactivation.

As defined in [11], LCO mode M equals to the period of LCO over two times of the sampling period T_S. Obviously, the smaller M is, the smaller LCO ripple can be expected. Therefore, the targeted M should be 1 to ensure the minimum number of active power transistors in the steady state.

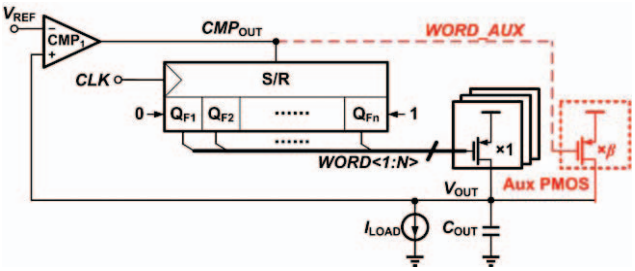

Fig. 4. The D-LDO with LCO reduction feed-forward path.

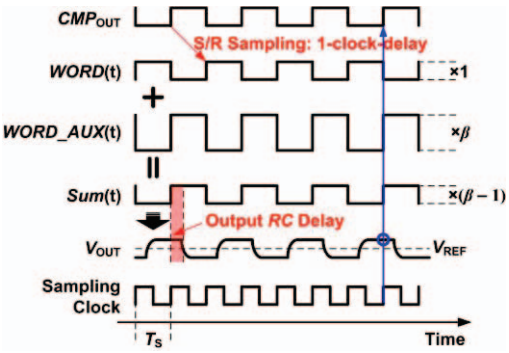

Fig. 5. Conceptual waveforms of a steady-state mode-1 D-LCO.

However, the mode-1 LCO cannot be guaranteed with the conventional D-LDO topology as discussed in [12].

To make $M = 1$, a feed-forward path is inserted to the D-LDO, as the dashed block in Fig. 4. Here the comparator output CMP_{OUT} is directly fed to drive the auxiliary power transistors (Aux PMOS) in parallel with the conventional PMOS array, with identical unit size but β in strength. This feed-forward path bypasses the integrator, and thus adds a zero to the D-LDO loop.

In this work, $\beta = 2$ is selected to achieve minimum LCO mode, which can be intuitively illustrated as in Fig. 5. Once CMP_{OUT} oscillates at a frequency of $F_S/2$ (mode-1), *WORD*(t) will be 1 in strength, $F_S/2$ in frequency, but 180° lagging from CMP_{OUT} because of the sampling operation in S/R. Meanwhile, *WORD_AUX*(t), directly driven by CMP_{OUT}, is in phase with CMP_{OUT} but β in strength. Consequently, the combined word *Sum*(t) will also be in phase with CMP_{OUT} but $(\beta - 1)$ in strength. *Sum*(t) then generates LCO at $F_S/2$ with 180° lagging of V_{OUT}. With a phase lag due to the output *RC* delay, V_{OUT} is sampled, and the comparator output $CMP_{OUT}(t + T_S)$ coincides with $CMP_{OUT}(t)$. With this feed-forward loop, the steady-state mode-1 LCO is achieved.

$\beta > 2$ cases are not considered here because larger β results in larger DC deviation on V_{OUT}. Additionally, $\beta = 1$ is not preferred as a mode-2 LCO is observed in both calculation and simulation. Theoretical analysis in detail can be found in [12].

III. Implementation and Simulation Results

Fig. 6 shows the schematic of the proposed D-LDO with fast transient, high current efficiency, and LCO reduction. The PMOS arrays consist of the coarse, fine, and Aux sections. Comparator CMP_1 senses the difference between V_{OUT} and V_{REF} and outputs CMP_{OUT}, which is used to drive coarse and

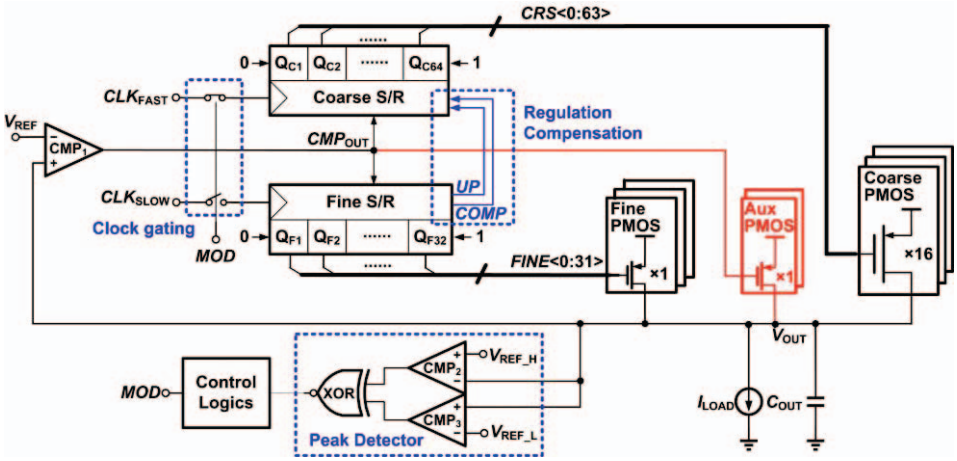

Fig. 6. The schematic of the D-LDO with fast transient, high current efficiency, and LCO reduction.

fine S/Rs, as well as the Aux PMOS. To extend the I_{LOAD} range and boost the loop gain, the coarse array is designed to be 64 PMOS units with ×16 strength. To cover the current gap between two adjacent *CRS* can provide with sufficient margin, the fine array is designed to be 32 PMOS units with ×1 strength. Finally, under $\beta = 2$ principle, the Aux PMOS is in ×2 strength. Obviously, the proposed LCO reduction scheme introduces negligible complexity and power consumption overheads. In addition, it is compatible to the CFT scheme, since it will not degrade the transient performance due to the much smaller Aux strength comparing to the coarse one.

For the under/overshoot detection, a peak detector is implemented with two comparators (CMP_2 and CMP_3) and an exclusive-OR (XOR) gate, which outputs "1" if V_{OUT} is not within the range between V_{REF_H} and V_{REF_L}. The output of the peak detector is fed to a control logic block that generates a mode selection signal *MOD* to determine whether the D-LDO operates in the coarse- or fine-tuning mode. A fast clock CLK_{FAST} = 500 MHz is applied to the coarse-tuning S/R, while a slow clock CLK_{SLOW} = 50 MHz is used for the fine-tuning S/R. These clocks should be readily available for an SoC. The coarse and fine S/Rs can be clock-gated, that saves the quiescent current in both modes, especially in the fine-tuning mode in steady-state. To allow a possible full range *CRS* change during coarse-tuning with sufficient margin, ΔT_1 is designed to be 128 times of the fast clock cycle (256 ns) as burst mode. To prevent the immediate re-entering to the burst mode right after exit, a guard period of ΔT_2 is inserted after the burst mode operation. And, a regulation compensation scheme is employed to provide the desired load current without reactivating the burst-mode [9].

This D-LDO was implemented with a 65 nm CMOS process and its layout is given in Fig. 7. The active area, including coarse/fine/Aux PMOS arrays, S/Rs and logics, is 0.01 mm^2, together with a 0.09 mm^2 on-chip 1 nF capacitors.

The simulated transient waveform of the proposed D-LDO is shown in Fig. 8. As can be seen, 60 mV and 52 mV voltage undershoot and overshoot is achieved, respectively, with 20 ns edge time and 2 to 100 mA load current step. Due to the relatively low F_S applied in fine-tuning, a 60μA of power

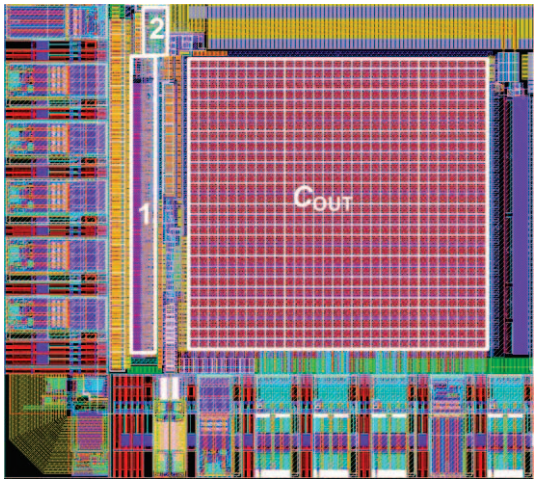

Fig. 7. Layout of the proposed D-LDO: 1) PMOS & S/Rs: 315×25 μm^2, 2) Logics: 70×25 μm^2, 3) C_{OUT}: 310×320 μm^2.

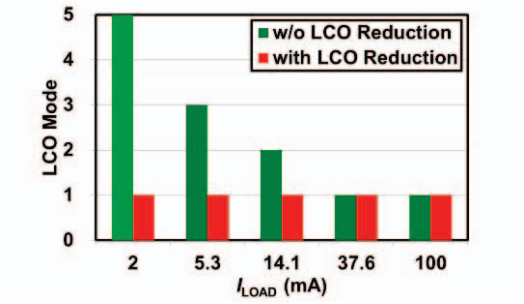

Fig. 9. Simulated LCO modes under an I_{LOAD} range from 2 to 100 mA, with and without the proposed LCO reduction technique.

consumption is simulated at steady state. Thus, a 99.9% peak current efficiency is obtained.

Moreover, with the proposed LCO reduction, a mode-5 LCO is significantly reduced to mode-1 at light load condition as shown in Fig. 8. And thus the output voltage ripple is reduced at steady state. Fig. 9 summarizes the simulated LCO modes with and without the proposed reduction technique, under an I_{LOAD} range from 2 to 100 mA. A full-load-range

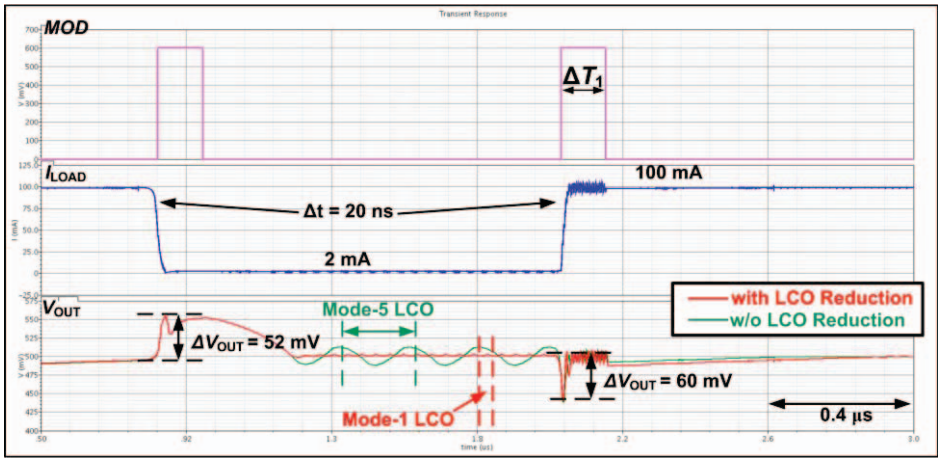

Fig. 8. Simulated transient waveform of the proposed D-LDO.

TABLE I COMPARISON WITH STATE-OF-THE-ART D-LDOS

	[13] 2013	[6] 2015	[7] 2015	This work
Process (nm)	180	110	130	**65**
Active area (mm^2)	0.81	0.04	0.114	**0.01**
V_{IN} range (V)	0.9-1.8	0.6-1.2	0.5-1.2	**0.6-1.1**
V_{OUT} range (V)	0.8-1.5	0.5-0.9	0.45-1.14	**0.4-1**
C_{OUT} (nF)	1000	1	1	**1**
I_Q (μA)	750	32	78	**60**
Peak *I* eff. (%)	99.6	99.96	98.3	**99.9**
Line reg. (mV/V)	N/A	2	N/A	**3**
Load reg. (mV/mA)	N/A	0.3	<10	**0.06**
Edge time (ns)	100	25000	N/A	**20**
Load step (mA)	1-100	80	0.5-2	**2-100**
ΔV_{OUT} (mV)	70	53	<40	**60**
FOM (ps)	5250	0.26	76.5	**0.36**
V_{OUT} ripple(mV)	N/A	4	15*	**3**

*Estimated from the measurement results.

mode-1 LCO reduction is demonstrated here with the proposed technique.

Table I compares the performance metrics between this design and other state-of-the-art works [6], [7], and [13]. In this table, output capacitors have been excluded for all the active area calculations. A widely used figure-of-merit (FOM) of speed [1] is employed as FOM = $C_{OUT}\cdot\Delta V_{OUT}\cdot I_Q/(I_{MAX})^2$, and a 0.36 ps FOM is calculated for this design. As observed from the table, the proposed D-LDO has achieved comparable, or better performances than the recent state-of-the-art works.

IV. CONCLUSIONS

A fully integrated D-LDO with fast transient, high current efficiency and LCO reduction has been proposed and demonstrated in 65 nm CMOS. By boosting the D-LDO loop gain and sampling frequency when voltage under/overshoot is detected, the simulated under/overshoot voltage is <60 mV, under a 2 to 100 mA load step within 20 ns edge time. Additionally, using the burst mode operation, a 99.9% current efficiency is maintained in the steady-state. With these techniques, a 0.36 ps FOM of speed is thereby achieved with negligible power and area overheads. Finally, a CFT-compatible LCO reduction technique is applied to reduce the LCO mode to 1 within the full load range.

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