A High Resolution Multi-Bit Incremental Converter Insensitive to DAC Mismatch Error

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***Abstract*— This paper presents a second order multi-bit incremental analog-to-digital converter with two-phase feedback DAC control logic, insensitive to capacitor mismatches and with enhanced performance in multi-bit implementation. Besides, the proposed technique eliminates the complexity of dynamic element matching and relaxes the Op-amp's settling time. Behavioral simulations show that it can achieve 115.55 dB SNDR at 128 clock cycles using a 7-bit quantizer without dynamic element matching.**

Keywords*— High resolution, incremental converter, multi-bit quantizer, insensitive to DAC mismatch

I. INTRODUCTION

Incremental analog-to-digital converters (ADCs) are widely used in low frequency high resolution instrumentation and sensor applications by offering several benefits: good linearity, easy multiplexing and a simple decimation filter [1]-[3]. Moreover, the reset operation after every conversion generates a finite-impulse-response (FIR) of the input signal, modifying the signal transfer function and removing the sample-hold. In practical applications, like temperature sensing and biomedical acquisition, the incremental converter must be highly efficient in terms of power consumption.

Sharing the same architecture of a sigma-delta modulator, the regular first-order incremental converter needs 2^n clock cycles for an n-bit resolution. Thus, the required sampling frequency is very high and the power consumption by active blocks increases. In order to reduce the required clock cycles in one conversion, it is preferable and more efficient to use high order architectures obtained through the cascade of integrators. However, when the order of the modulator is larger than 2, a stability problem arises that degrades the architecture's performance [4]. Contrary to a single loop structure, two-step architectures [5]−[7] were proposed. But, realistic circuit non-idealities will limit the performance.

On the other hand, a single-bit or a multi-bit quantizer can be utilized in an incremental converter. Conventional structures often use single-bit quantizer since it is inherently linear. However, a multi-bit quantizer can improve the performance by reducing the quantization error. Due to the nonlinearity of the DAC mismatch, dynamic element match (DEM) is necessary. Further, the data weight average (DWA) technique widely used in sigma-delta modulators is not too effective in incremental converters [8]. Also, a smart-DEM algorithm was proposed in [9] but featuring a complicated algorithm.

Then, this paper proposes a two-phase implementation of the DAC – 1^{st} phase with a single-bit conversion followed by a 2^{nd} phase with multi-bit conversion. The resolution is improved by multi-bit implementation without the utilization of a DEM technique. The paper is organized as follows, next Section reviews the transfer function of conventional structures. A novel feedback DAC control logic is proposed in Section III. Simulation results are exhibited in Section IV and Section V concludes the paper.

II. INCREMENTAL CONVERTER - REVIEW

A. Single-bit Incremental Converter

Fig. 1 presents a single-bit L-th order incremental converter. The structure is very similar to a ΣΔ modulator, containing cascaded integrators, a comparator and a two-level DAC, as well as several feed-forward paths. The incremental converter requires resets in the integrators differently from the ΣΔ modulators.

The operation of the converter includes the reset of the integrators' outputs at the beginning of the conversion, followed by the accumulation in the integrator of the difference between the input signal V_{in} and the result of the feedback DAC. Besides the accumulation path, feed-forward paths are used to keep the loop stable. At the end of the N-th clock cycle, the residual voltage V_o at the output of the last integrator will become,

$$V_o(N) = c_1 \cdots c_L \sum_{i_L=1}^{N-1} \cdots \sum_{i_1=1}^{i_2-1} \{V_{in} - D[i_1]V_{ref}\} \quad (1)$$

where, $c_1, \cdots c_L$ are the coefficients along the accumulated path, L is the order of the loop and D is the quantizer output, further, the integrator output $V_o(N)$ is bounded by V_{ref} which is guaranteed by a stable loop. Thus, the estimation of the input is,

$$V_{in} = \frac{c_1 \cdots c_L \sum_{i_L=1}^{N-1} \cdots \sum_{i_1=1}^{i_2-1} D[i_1]V_{ref}}{M} + \frac{V_o(N)}{M} \quad (2)$$

where, M is a constant equals to $c_1 \cdots c_L \binom{N}{L}$. When compared with the ADC transfer function, it can be derived from (2) that the first term of the right side is the estimation of input signal and the second term is the quantization error. In contrast with the estimation of the input signal, the quantization noise is

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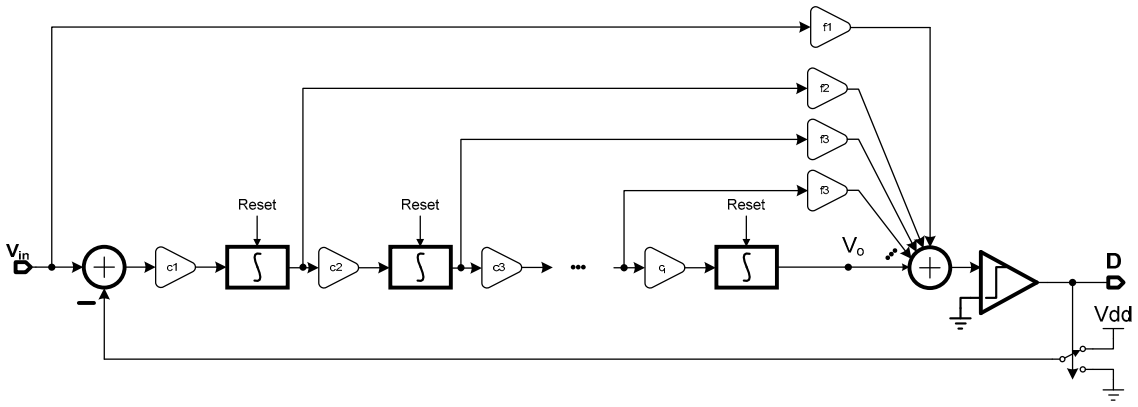

Fig. 1. L-th order incremental architecture.

determined by the integrator output $V_o(N)$, the number of clock cycles, the coefficients along the accumulated path and the order of the architecture. In general, the resolution of the L-th order incremental converter with N clock periods is,

$$R_{Lth} = \log_2(c_1 \cdots c_L \binom{N}{L}) \tag{3}$$

Based on the above, high order architectures with a larger number of clock periods can achieve higher resolution. However, the push for large number of clock periods means that the sampling frequency of the data converter needs to be increased. As a result, the active blocks, like opamps, will consume more power to achieve the settling, and increasing the order of the modulator can also imply high resolution affecting stability. For a high order architecture, the coefficients along the accumulation paths are restricted to values lower than 1 to maintain the stability of the loop. For example, a 4^{th} order incremental structure was implemented in [4] with the coefficients c_1, c_2, c_3 and c_4 equal to 0.25, 0.4, 0.22 and 0.11, respectively. The effectiveness of a high order architecture is attenuated by the loss factor in the signal path, and the impact is as illustrated in Fig. 2, where it can be seen that the resolution is degraded by 8.69 bit.

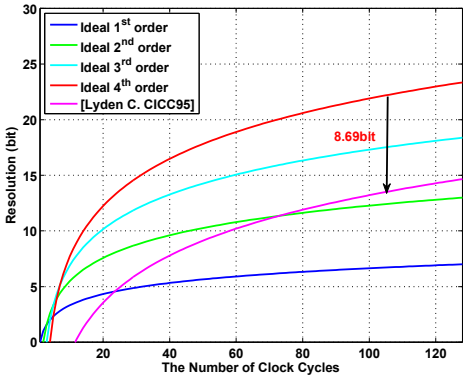

Fig. 2. Relationship between resolution and the number of clock cycles.

B. *Multi-bit Incremental Converter*

In the preceding subsection, it was pointed out that the quantization noise is determined by 4 parameters: the order of the architecture, the coefficients along the accumulation path, the number of clock cycles at one conversion and the final integrator output. Therefore, minimizing the last stage integrator output can achieve higher resolution, because of the smaller residual voltage $V_o(N)$.

Similar to a multi-bit ΣΔ modulator, a multi-bit quantizer instead of a single-bit quantizer can also be used in the incremental converter. With a multi-bit quantizer, the transfer function of a L-th order architecture with N clock periods becomes,

$$V_o(N) = c_1 \cdots c_L \sum_{i_L=1}^{N-1} \cdots \sum_{i_1=1}^{i_2-1} \{V_{in} - D[i_1]V_{refm}\} \tag{4}$$

$$V_{refm} = \frac{V_{FS}}{2^m - 1} \tag{5}$$

where, m is the resolution of quantize. Thus, the estimation of the input signal V_{in} can be described as,

$$\overline{V_{in}} = \frac{c_1 \cdots c_L \sum_{i_L=1}^{N-1} \cdots \sum_{i_1=1}^{i_2-1} D[i_1]V_{refm}}{M} + \frac{V_o(N)}{M} \tag{6}$$

When comparing equations (2) and (6), it can be concluded that the signal-to-quantization-noise-ratio (SQNR) does not increase, unless the residual voltage $V_o(N)$ is reduced. Fortunately, the integrator output swing during the whole accumulation process is smaller, because the feedback DAC can track the input signal more accurately and the difference between them is bounded by V_{refm}. Then, for a L-th order incremental converter with a m -bit quantizer, the ideal resolution is,

$$R_{Lth} = \log_2(c_1 \cdots c_L \binom{N}{L}) + m \tag{7}$$

The above analysis shows that a multi-bit quantizer employed in the incremental architecture can increase the resolution. The effectiveness of the multi-bit quantizer is increased if a higher resolution quantizer is used. However, multi-bit incremental architectures suffer from the nonlinearity of the DAC due to capacitors mismatches.

III. Proposed Multi-bit Incremental Converter

Based on the previous analysis, the resolution of an incremental converter can be enhanced by increasing the number of clock cycles at the cost of power dissipation, increasing the order of the structure but degrading stability, while the utilization of the multi-bit quantizer will impose nonlinearity in the feedback DAC. A multi-bit quantizer is

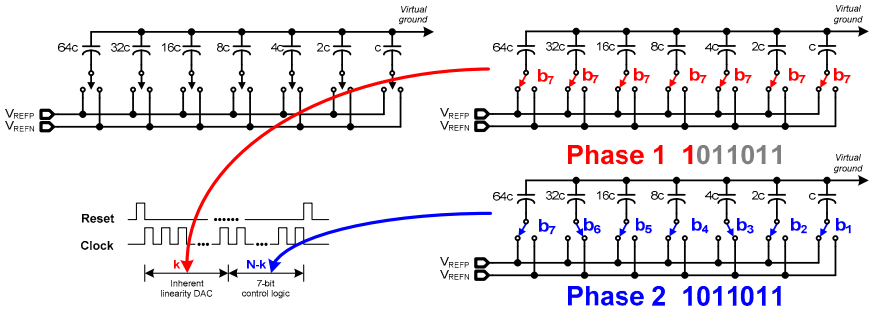

Fig. 3. Two-phase feedback DAC in one conversion.

a potential method to achieve an energy efficient solution because it will not increase the power consumption of the opamps.

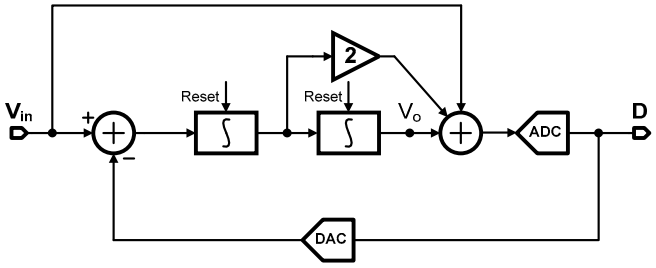

Fig. 4. Second order multi-bit incremental converter.

A. *The Adopted Second-Order Multi-bit Architecture*

Fig. 4 depicts a diagram of a second order multi-bit structure with a low-distortion feed-forward modulator [10]. The SQNR can be improved by using a high resolution quantizer. For example, with a 7-bit quantizer, the SQNR is enhanced by 42dB. When compared with a single-bit quantizer, the required number of clock cycles can be reduced by 11 times for a given resolution.

However, the non-linearity of the multi-bit DAC restricts the performance. Then, the capacitor mismatch needs to be calibrated or corrected. For a ΣΔ modulator, dynamic element matching, such as data weight average (DWA), is an effective method to average the mismatch error. This methodology works well in a ΣΔ modulator but is not effective in the incremental converter because of the weight variants, especially for a smaller number of clock cycles in a single conversion [8]. Therefore, the quantizer used in the previous 2^{nd} order architecture is selected not larger than 3-bit [6], [11], meaning that the benefit of a smaller integrator output is not fully utilized. After analyzing the impact of injected mismatch error, a novel solution is proposed next.

B. *Mismatch of Multi-bit DAC and Proposed Methods*

Depending on the digital output of the quantizer, the DAC mismatch error is injected into the incremental converter in the feedback path. Generally, the various DAC capacitors can be described as follows,

$$C_i = \overline{C_u}(1 + \varepsilon_i) \tag{8}$$

where, the $\overline{C_u}$ is the average value of the capacitors array and the ε_i presents the mismatch error. Moreover, the mismatch error obeys the following equation,

$$\sum_{i=1}^{2^m} \varepsilon_i = 0 \tag{9}$$

where, m is the resolution of the quantizer. Considering the second order structure, the weight of the DAC error caused by the mismatch in j^{th} clock cycle is [9],

$$W_j = N - j \tag{10}$$

Thus, at the end of N-th clock periods, the total injected error can be described as,

$$\varepsilon_{tot} = \sum_{j=1}^{N-1} W_j \times \left(\sum_{i=1}^{D[j]} \varepsilon_i\right) \tag{11}$$

where, $D[j]$ is the code of the quantizer in the j^{th} clock cycle. Therefore, the errors injected at the beginning of the clock cycles have larger weights, and the impact of the injected mismatch error is more significant. Further, this characteristic implies that the performance can be improved by attenuating the impact of the injected mismatch error at the initial phase of the clock cycles.

Based on the previous analysis, a novel two-phase feedback DAC implementation is proposed with the corresponding block diagram exhibited in Fig. 3. In phase 1 (single-bit phase), only 1b MSB code of the quantizer is used to control the DAC capacitor array, and lasts for k clock cycles. For example, if the code is 1011011, all of the capacitors are connected to the supply. In phase 2, the code of the quantizer is fully used to control the DAC capacitors in a multi-bit manner in the remaining $N - k$ clock periods. In conclusion, there is no linearity problem in phase 1, because either the whole DAC array is connected to the supply or to the ground. In phase 2, there are injected non-linearity errors in the loop with a smaller weight. Therefore, the total injected mismatch error is,

$$\varepsilon'_{tot} = \sum_{j=k}^{N-1} W_j \times \left(\sum_{i=1}^{D[j]} \varepsilon_i\right) \tag{12}$$

C. *Number of Clock Cycles - Optimization*

The impact of injected non-linearity is attenuated by the proposed DAC implementation method because the weight of the mismatch error is smaller in phase 2.

However, fewer number of clock cycles for phase 2 would degrade the performance because the residual voltage can't be

reduced significantly without a sufficient number of clock cycles. Besides, like in the sigma-delta modulator, the incremental converter is a system with memory, and the loop only after a few clock periods can reduce the swing of the integrator after phase 2 is turned on.

IV. Simulation Results

Here, the DAC mismatch will be analyzed through the behavioral simulation obtained with MATLAB for the proposed technique with the respective implementation. The plot of the SNDR vs. the number of clock cycles for phase 1 is shown in Fig. 5 (red curve). The performance will not be affected if k is not larger than 114 clock cycles because the residue integrator output voltage after phase 2 is sufficiently small.

Then, the non-linearity induced by the DAC mismatches is injected in the model. The clock cycles k for phase 1 are swept, with 50 times Monte-Carlo (MC) simulations under the capacitor mismatch error of $\sigma = 0.3\%$ for the unit element. Fig. 5 illustrates the simulation result in blue dots (the MC dots) and the pink curve (averaging over the MC simulations). For smaller values of k, the impact of nonlinearity is critical since the DAC mismatch weight contribution from phase 1 is significant. With a larger value of k, the effect of nonlinearity is attenuated and the performance is similar to that of an ideal multi-bit quantizer structure. Further, it can be deducted that if k is chosen between 108 and 114, the SNDR is close to the ideal condition, then, the value of k is selected here with a value of 110.

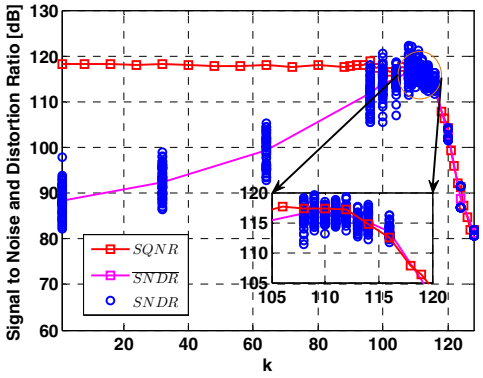

Fig. 5. Monte Carlo analysis for the proposed architecture.

To demonstrate the effectiveness of the proposed architecture, 4 cases are simulated: 1) a conventional second-order model with ideal multi-bit DAC; 2) DAC mismatch error injection but without any DEM; 3) the traditional DWA technique averaging the mismatch error; and 4) the proposed structure without DEM. The simulation results are shown in Fig. 6 and the proposed technique can achieve 115.7dB SNDR which is close to the ideal case.

V. Conclusions

The capacitor mismatch error restricts the performance of a multi-bit incremental converter. This work, after studying the operation principle of the capacitor mismatch error, shows the impact of nonlinearity in a single-loop structure. With the proposed 2-phase DAC implementation methodology, the simulation results confirm that the technique can achieve a

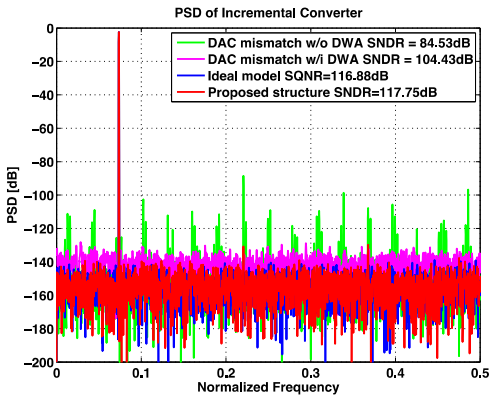

Fig. 6. Power spectrum density of the incremental converter.

SNDR of 115dB at 128 clock cycles using a 7-bit quantizer, with 110 cycles single-bit DAC feedback in the 1st phase and 18 cycles of 7b DAC feedback in the 2nd phase.

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