

# A 2.4-GHz Digitally-Modulated Class-D Polar PA Using Power-Gating, Interactive AM-AM Modulation and a Dynamic Matching Network for Battery Lifetime Extension

Wei-Han Yu, Xinggiang Peng, Pui-In Mak, and Rui Martins<sup>1</sup>

State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, 1- also with Instituto Superior Técnico, TU of Lisbon, Portugal



## System Highlights:

- Dynamic Matching Network(DMN) biases optimum load for Class-D PA at each AM input code
- Class-D PA Power-Gating (PAPG) minimizes leakage current during off-state of each PA unit cell
- DMN improves MN power efficiency by reducing its transform ratio
- Class-D PAPG guarantees the reliability during off-state and enabled 1.5V operation without cascode devices

# **Class-D PAPG Technique**





- PAs • PAPG increased the reliable supply voltage of PA unit cell by 25.0%
- DMN optimum load bias improved DE by 21.2% @ 5.7dB back-off
- DMN improves MN power efficiency is improved by 26.0% from n = 11.4 to 2.6

GND (DMN) Bit AM 16.5 16 15 14 14 14.5 0 2	VDD(PA)	And Post drops - 32% faster 2.5hrs 8 10		<ul> <li>CW PAE :</li> <li>40.7% ave</li> <li>Mode switt</li> <li>52.0%</li> <li>PAE Optimize</li> <li>PAE Optimize</li> <li>Comparison</li>     &lt;</ul>	• CW PAE > 37.0% above 6dB back-off • 40.7% average PAE achieved for 802.11g signal • Mode switching technique extend this number to 52.0% PAE Optimized • Voit & PAE • Voit & PA			
	Operation Th	Comp	arison v	vith Stat	o-of-tho	-∆rt		
		comp						
	This Pout-Opt. Mode	Work PAE-Opt. Mode	R. Hezar et al. JSSC'15 [10]	Y. Yin et al. TMTT'15 [15]	L. Ye et al. ISSCC'13 [11]	P. Madoglio et al. ISSCC'12 [9]	Y. Yoon et al. TMTT'12 [16]	
Frequency	2.4 GHz		2.4 GHz	2.4GHz	2.4 GHz	2.4 GHz	2.4GHz	
Key Techniques	Power-Gated Class-D PA + Multi-Bit DMN + Mode Switching		PWM + Sigma-Delta	Bias Mode Switching	Inverse Class-D PA + Single-Bit DLM	Delay Line + Class-D PA + Out-Phasing	Mode Switching + Single-Bit DLM	
Technology	Standard 65nm CMOS		Standard 45nm CMOS	0.18-µm CMOS	Standard 65nm CMOS	32nm CMOS + Ultra-Thick Metal	0.18-µm CMOS	
Supply Volt. (V)	t. (V) 1.5 °		1.7/1.2	5.6	1.2	1/2.05	3.3	
Peak Pout (dBm)	22.0		23	27	23.3	25.9	23.1	
Peak PAE (%)	4	8.7	47	26.1	38	N/A	42	
Pout,ave (dBm) <sup>b</sup>	16.9 (15.54)	16.3	14.8	22 <sup>d</sup>	16.8	20.0	15.7	
PAE <sub>ave</sub> (%) <sup>b</sup>	34.8 (31.7) °	40.7 °	23	21.3 <sup>d</sup>	21.8	22	18.5	
EVM (dB) <sup>b</sup>	-25.2 (-30)	-25	-29	-26.9	-28	-25	-25	
Leakage Current (µA)	20 (TX + ESD pads)		N/A	N/A	N/A	N/A	N/A	
Impedance Correctability : For direct 1.5-V	$P_{out,ave} = 11.47 \rightarrow 11.86 \text{ dBm}$ $PAE_{ave} = 15.49 \rightarrow 15.91\%$ V AA battery powering, and Pout is >14 dl		No	No nuous operation.	No	No	No	

c : PAE<sub>ave</sub> = 52% by mode-switching from Pout-optimized to PAE-optimized modes under the AA battery test d : Measured with 40-MHz 64-QAM OFDM signal. PAPR is similar, and therefore comparable





# **Measurement Setup & Result** V<sub>PM</sub> V<sub>out</sub> **Result Highlights:**