A 0.45V 147-to-375nW Hardware-Efficient Real-Time ECG Processor with Lossless-to-Lossy Data Compression for Wireless Healthcare Wearables

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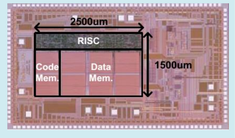
Research Background

ECG data compression processor:
- For data reduction in wireless ECG sensor
- Data storage and power-hungry wireless communication can be reduced
- Power saving in wireless transmitter: $P_{saving}(\%) = (1\text{-}1/CR)\times 100$ where CR is compression ratio
- Reduction in wireless system power if $P_{processor} + P_{tx}/CR < P_{tx}$

Assumptions:
- Wireless module consumes large portion of system power
- Wireless transmitter power is proportional to data transmission amount

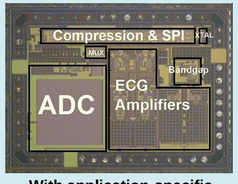
State-of-the-art:

H. Kim et al [TITB'10, EMBC'08,09]



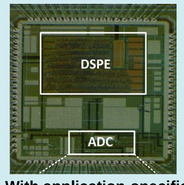
With compression algorithm running in processor

Xin Liu et al. [JSSC'14]



With application-specific compression processor

C.J. Deepu et al. [JSSC'14]



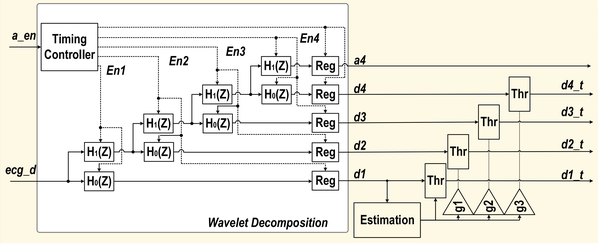
With application-specific compression processor

Provide fixed compression ratio

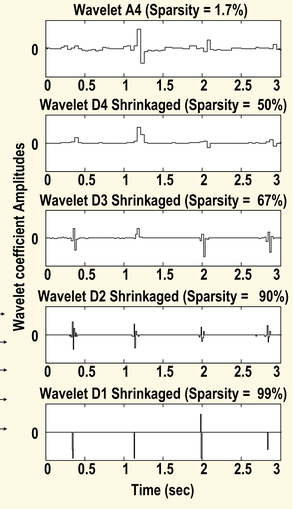
Wavelet Shrinkage

Features:
- Provide sparse representation of ECG
- Increase compression ratio

Optimizations:
- Wavelet is selected by simulation for best balance of accuracy, compression ratio and low computational cost
- Filter coefficients are simplified, reducing 64.4% logic gates in this module
- Thresholds of D2-D4 are scaled from threshold of D1 with preset gains, reducing threshold estimation circuits
- With timing controller, circuit activity is reduced



Wavelet shrinkage architecture



Waveforms of wavelet shrinkage

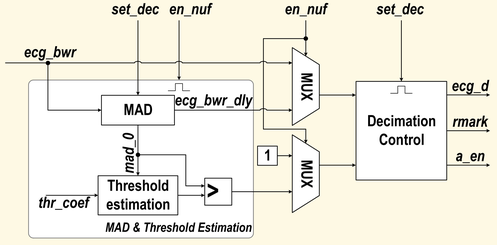
Adaptive Temporal Decimation (ATD)

Features:
- ATD decimates P/T waves (4 to 13.5 Hz) and QRS waves (8 to 27 Hz) with two different rates, for further data reduction
- Reduces circuit activity and processor power consumption up to 56.8%

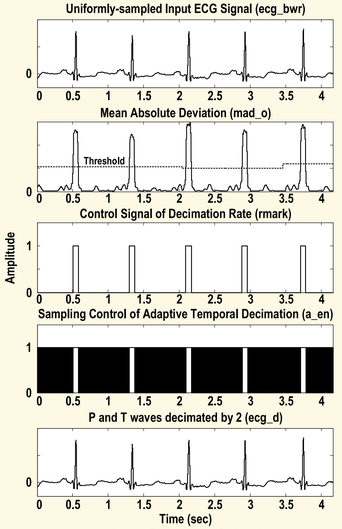
Optimizations:
- Mean absolute Deviation (MAD) for locating QRS waves is robust to noise.

$$MAD(x) = \frac{1}{n}\sum_{i=1}^{n} |x_i - \bar{x}|$$

- Window size of MAD is chosen for low computational cost. MAD architecture is optimized.

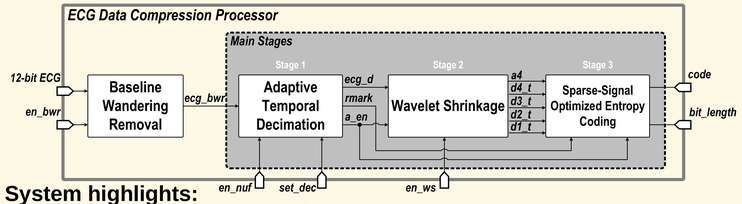


Adaptive Temporal Decimation Architecture



Waveforms of ATD

System Diagram

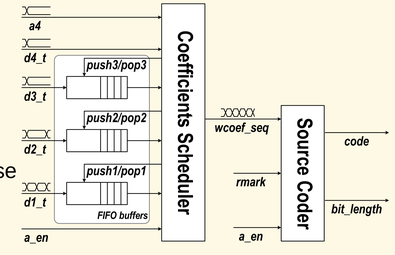


System highlights:
- Scalable compression ratio of 2.89 – 26.91
- Power consumption below 375 nW
- Optimizations in algorithm, architecture and circuit levels
- Underlying digital circuits are customized for energy efficiency at near-threshold regime

Customized Source Coding

Features:
- Optimized for sparse wavelet coefficients
- Compatibility with ATD (the sampling rate of each sample is encoded)

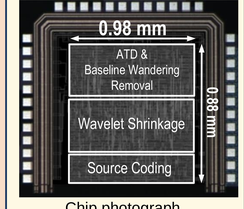
Optimizations:
- Modified Huffman coding (header+offset) to reduce dictionary size
- Combines run-length coding to transmit sparse signal efficiently
- Reduce averaged word length from 13.68 to 3.49 bits



Source coding with modified Huffman and run-length coding

Results and Comparison

- Achieved wide-range of compression ratio
- Low power consumption and high accuracy are achieved



Chip photograph

Comparison with state-of-the-art

	This Work			JSSC'14 Liu et al	JSSC'14 Deepu et al	Tran. CE'11 Chua et al
Verification Level	Experiment			Experiment	Experiment	Simulation
CMOS Tech. (nm)	180			180	350	65
V_{DD} (V)	0.45			0.5	2.4	1
Operation Freq. (Hz)	360 (test case)			250/500	32 k/2 M	24 M
Sampling Rate (Sa/s)	360 (test case)			250/500	256/512	256
BW (Bits)	12			9	12	10
CR	2.89	5.24	26.91	N/A	2.25	2.38
PRD (%)	0	0.12	3.11	0	0	0
Power/Channel (μW)	0.313	0.375	0.147	0.435	0.535	56.6