A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 MASH ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS

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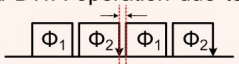
Research Background

Motivations

- **Background**:More opamps and quantizers engaged in MASH ΔΣ modulator
- Improve power efficiency of opamps and quantizers in MASH ΔΣ modulator for wideband applications

Problem statement

- **Poor Power Efficiency**:Vertical opamp sharing in [1], excluding 1st integrator (power dominant)
- **Urgent Timing**:non-overlapping gap of the clock phases for 1st quantizer and DWA operation due to Horizontal sharing

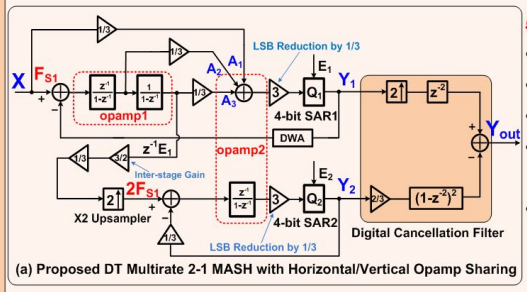


[1] R. Zanbaghi, et al., "A 75dB-SNDR, 5-MHz Bandwidth Stage-Shared 2-2 MASH ΔΣ Modulator Dissipating 16 mW Power," *IEEE Trans. Circuits Syst.I*, vol.59, no.8, pp.1614-1625, Aug. 2012

Proposed Techniques

- **Horizontal/Vertical** Opamp Sharing **firstly both** utilized
- **Split** Adder's working time
  - Extend working time of the 1st quantizer +DWA
  - Fit to 2X operation frequency of 2nd stage for vertical sharing
- **SAR-based**(single comparator) quantizer utilized
  - More power and area efficient
  - Insensitive to comparator offset caused by scaling gain(1/3)
- Boost the OSR of 2nd stage (additional 9dB E2↓) without any power penalty
- Sharing the references of both quantizers

Modulator Architecture

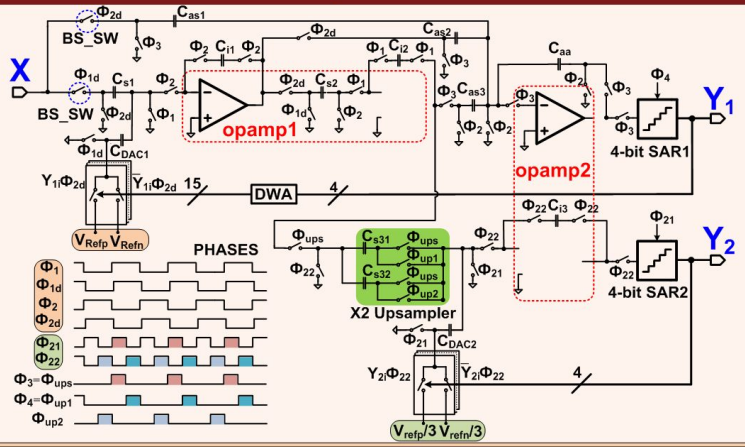


(a) Proposed DT Multirate 2-1 MASH with Horizontal/Vertical Opamp Sharing

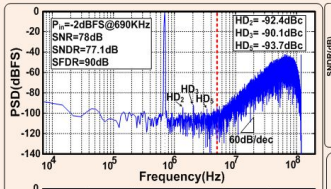
Features:

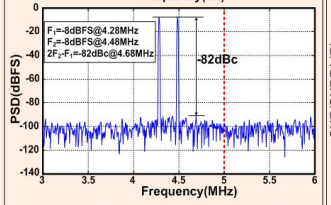
- Horizontal sharing 1st and 2nd Integrator
- Vertical sharing Adder and 3rd Integrator
- Multirate Operating Mode (120/240MHz)
- Gain scaling (1/3) applied in both stages to reduce swing (Dynamic Range↑)
- References shrink by 1/3 to compensate the preceding scaling-gain (LSB reduction by 1/3)

Circuit Implementation

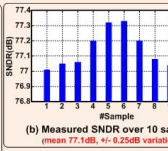


Measurement Results

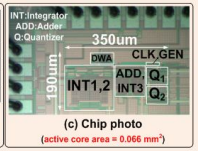




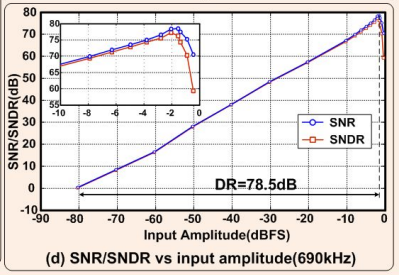
(a) Measured FFT and IMD3



(b) Measured SNDR over 10 samples (mean 77.1dB, +/- 0.25dB variations)



(c) Chip photo (active core area = 0.066 mm²)

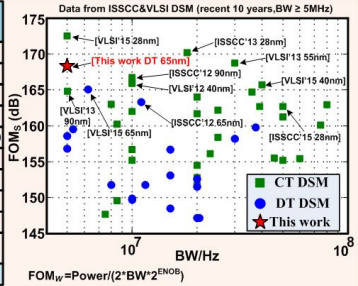


(d) SNR/SNDR vs input amplitude(690kHz)

Comparison with the State-of-the-Art

	VLSI'13 S. Rao	VLSI'15 Z.-J. Chen	ISSCC'15 D.-Y. Yoon	VLSI'15 G.-W. Wei	This Work
Architecture	CT+VCO	NS-SAR*	CT	CT	DT
Technology(nm)	90	65	28	28	65
Supply (V)	1.2/1	0.8	1.2/1.5	0.9/1.8	1.2
BW(MHz)	5	6.25	50	5	5
F_S(MHz)	640	50	1800	432	120/240
DR(dB)	77	N/A	85	83.9	80
SNDR(dB)	73.9	58	74.6	80.5	77.1
Power (mW)	4.1	0.12	78	3.16	4.2
Area (mm^2)	0.16	0.0123	0.34	0.066	0.066
FOM_W (fJ/Conv.-step)	101	14.9	177.7	36.5	69.7
FOM_S(dB)	164.8	165.1	162.7	172.5	167.9

*NS-SAR:Noise-Shaping SAR



FOM_W=Power/(2*BW*2^{ENOB})

FOM_S=SNDR+10lg(BW/Power)