Sub-μW QRS Detection Processor Using Quadratic Spline Wavelet Transform and Maxima Modulus Pair Recognition for Power-Efficient Wireless Arrhythmia Monitoring

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Abstract – This paper describes a power-efficient processor for extracting the timing of QRS complex from digitized ECG, based on the hardware-efficient architecture of quadratic spline wavelet transform (QSWT) and maxima modulus pair recognition (MMPR). The processor succeeds in saving the wireless system's power by 6×.

I INTRODUCTION

The wireless electrocardiogram (ECG) sensor provides a convenient way for long-term monitoring of the health status of the heart. The timing of QRS wave (corresponding to the heart beat) offers fluent information for arrhythmia monitoring. For system power reduction, local data reduction processor is an effective approach, to reduce the power-hungry wireless data transmission. Specifically, this paper reports an ECG QRS detection processor to realize the option of transmitting only QRS timings. This processor measures significant wireless system's power reduction by 6× [1].

II. ECG QRS DETECTION PROCESSOR DESIGN

Fig. 1 shows the block diagram of proposed processor. The key attributes are the Quadratic Spline Wavelet Transform (QSWT) and Modulus Maxima Pair Recognition (MMPR). A 10-bit SAR ADC (over-sampled by 4 to realize an effective resolution of 12-bit fixed point) and a wireless controller are co-integrated on chip to allow real-time verification. Off-chip TI CC2500 wireless module managed by wireless controller can be configured to transmission modes: 1) QRS detection result, 2) raw ECG data or 3) both. The back-end of the system is a PC terminal that displays the digitized ECG signal, QRS complex occurrence and heart rate in real time. The recorded ECG data can be stored for further analysis.

QRS wave is transformed to the shape of Modulus Maxima Pair (MMP) with QSWT for convenience of recognition. By recognizing the zero-crossing point inside MMP, accurate timing of QRS wave can be detected. Fig. 2 shows the wavelet transform (WT) architecture to various wavelet scales. Since the larger scale of wavelet transform coefficients relate to more hardware resource and lower frequency response, wavelet fine scale 3 is selected for its balance of hardware efficiency and detection accuracy, with total 4+8+8 FIR filter taps required for consecutive $H(z)$, $H(z^2)$ and $G(z^4)$. The MMPR consists of feature extraction blocks (zero-crossing point detection, signal peak detection, and threshold estimation) and decision-making state machines. Here zero-crossing point detection compares consecutive samples and output indications of rising and dropping zero-crossing points, relating to downward and upward QRS waves, respectively. The signal peak detection is by differentiation of the input wavelet coefficient followed by the same zero-crossing detection, distinguishing upward and downward peaks respectively. By comparing with threshold TH, the signal peaks are classified to peaks induced by noises and by QRS waves. By averaging the amplitudes of noise peaks and signal peaks, the estimations of noise amplitude (ANPL) and signal amplitudes (ASPL) are decided, respectively. The threshold TH updates with (1).

$$TH = ANPL + \beta(ASPL - ANPL) \qquad (1)$$

The three signals are feed into decision-making state machine for recognition of MMP. The state machine is modeled with states $Seen\_none$, $Seen\_peak$, $Seen\_zero$, $Seen\_opposite$, to represent the MMP shape with a peak, zero-crossing and another peak with opposite direction (peaks should exceed threshold). Every state transition from $Seen\_peak$ finally to $Seen\_opposite$ confirms the MMP.

III. MEASUREMENT RESULTS

The processor (including wireless controller) fabricated in 0.35-μm CMOS occupies 1.03×1.08 mm^2, whereas the ADC occupies 0.25×0.32 mm^2. The entire IC was tested at a single 1.8-V supply. The wireless module TI CC2500 operates at 2.4 GHz with an output power of 0 dBm and the testing distance is 10 m. Fig. 3 shows the chip micro-photograph and the chip testing platform. Fig. 4-5 shows the related signals. TABLE I summarizes the power consumption in the 3 data transmission modes. Since only the QRS wave timing is transmitted in Mode 1, it lowers effectively the system power by 6×, verifying the feasibility of the proposed QRS detection processor. The MIT-BIH arrhythmia database is employed to evaluate the detection accuracy of the processor in real time under wireless acquisition. A comparison with prior arts is given in TABLE II.

IV. SUMMARY AND CONCLUSIONS

This paper reported the architectures of QSWT and MMPR with the chip fabricated and tested. The 300-Hz processor draws only 0.83 μW with good detection sensitivity 99.31% and predictivity 99.70%, which is favorably comparable with the prior arts. Mode 1 with solely the result of QRS detection exhibits 6× reduction of system power over modes 2 and 3.

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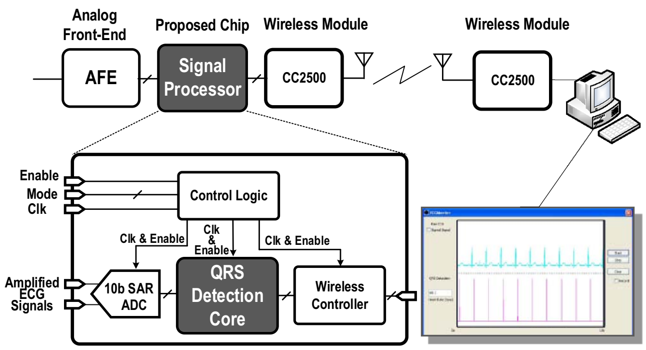

Fig. 1. QRS detection processor for a wireless ECG acquisition system.

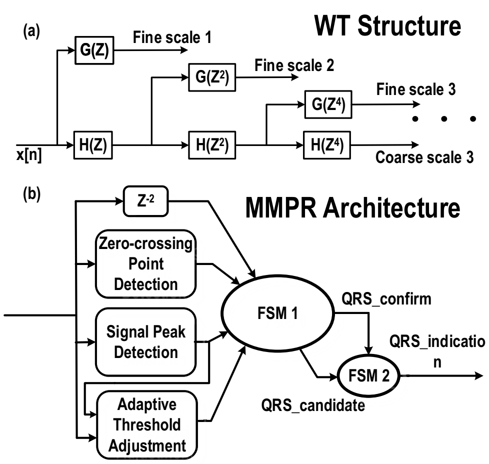

Fig. 2. (a) "à trous" algorithm for WT. Here H(Z) and G(Z) are the low-pass and high-pass QSWT filters. (b) Architecture of MMPR

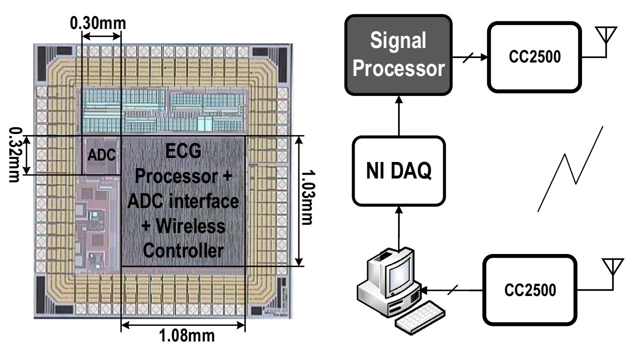

Fig. 3. Left: Photograph of the chip. Right: Testing platform of the chip. National Instruments Signal Acquisition/Generation Board (NI DAQ) for generating analog signal of MIT-BIH arrhythmia database. The reported IC controls the CC2500 transceiver for data transmission. PC receives the ECG data with CC2500, compute heart rate variability data and displays ECG information.

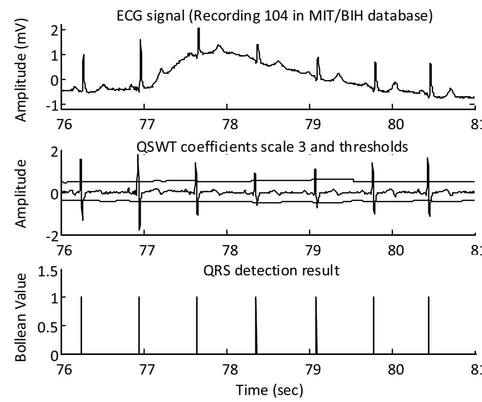

Fig. 4. Signals for QRS detection.

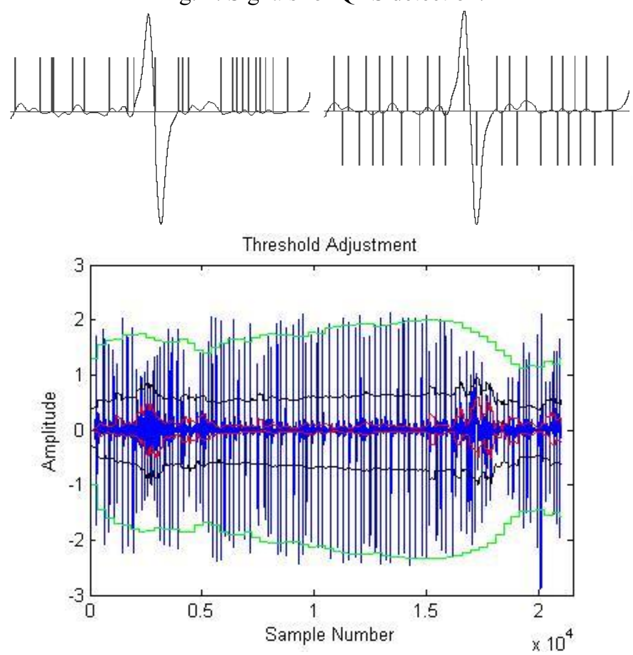

Fig. 5. Upper left: MMP and zero-crossing indications. Upper right: MMP and signal peak indications. Bottom: Threshold adjustment with noise (red), signal (green) estimates and threshold (black)

TABLE I. Power consumption

V_{DD}	Mode *	Power			
		ADC (μW)	Digital (μW)	Wireless TX (mW)	**Total (mW)**
	1	2.36	0.83	1.57	**1.58**
1.8V	2	2.38	1.55	9.37	**9.38**
	3	2.66	1.57	9.37	**9.38**

*Mode 1 stands for sending QRS detection result only. Mode 2 for sending raw ECG data only. Mode 3 for sending both.

TABLE II. Comparison table

Reference	**This Work**	TBCAS [2]	ISCAS [3]	ASSCC [4]	IIT [5]
Type	**Meas.**	Sim.	Meas.	Meas.	Sim.
Se (%)	**99.31**	99.81	95.65	99.63	99.83
Pr (%)	**99.7**	99.8	99.36	99.89	98.65
Area (mm^2)	**1.11**	N/A	0.68	1.1	0.074
Power (μW)	**0.83**	2.7	2.21	176	0.55
Tech. (μm)	**0.35**	0.35	0.18	0.18	0.065
V_{DD} (V)	**1.8**	3.3	N/A	1.8	N/A
Freq. (Hz)	**300**	N/A	500	1 M	1 k