Time-Domain I/Q-LOFT Compensator Using a Simple Envelope Detector for a Sub-GHz IEEE 802.11af WLAN Transmitter

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This paper proposes a hardware-efficient time-domain scheme to digitally compensate the I/Q imbalance and LO feedthrough (LOFT) of a sub-GHz wideband transmitter for the IEEE 802.11af WLAN. A simple envelope detector is the only analog part. The parameters are updated by Least-Mean-Square and estimated efficiently in time domain by using COordinate Rotation DIgital Computer (CORDIC), saving the training time and power consumption. The measured wideband image-rejection ratio (IRR) and LO-leakage-rejection ratio (LRR) are improved from 18.9 to 41.3 dB, and 20.4 to 37.9 dB, respectively.

I. Introduction

IEEE 802.11af [1] is emerged as a low-cost wireless local-area network (WLAN) for opportunistic use of the 10x-wide (54 to 862 MHz) sub-GHz TV bands. In practice, the I/Q imbalance and LO feedthrough (LOFT) of such a wideband transmitter (TX) can highly degrade the output error vector magnitude (EVM), and manifest itself as a dc offset in the receiver (RX) limiting the dynamic range. Hence, a digital-intensive I/Q-LOFT compensator is common, by sensing the impairments with a RX [1]-[2] or an envelope detector (ED) [3]-[4] over the full spectrum. The I/Q imbalance of the RX [1] can inherently limit the correctable image-rejection ratio (IRR) of the TX, while ED in [3]-[4] entails an added-on DSP to perform a 2048-point fast Fourier transform to update the 2D lookup table, being power hungry and slow in the training process. Here, a Least-Mean-Square (LMS) I/Q-LOFT calibration scheme is proposed. It estimates, in the time domain, the impairment parameters, while using COordinate Rotation DIgital Computer (CORDIC) [5] to lower the entailed training time and power consumption.

II. Proposed Time-Domain I/Q-LOFT Calibration Scheme

In order to accurately detect the small envelope signal generated by I/Q imbalance and LOFT, the proposed ED (Fig. 1) senses the envelope of OUT_{DET} with a high voltage gain. The LOFT and I/Q image are mapped to f_{BB} and $2f_{BB}$ in the envelope, respectively. ED output can be modeled as,

$$\mathrm{OUT_{DET}}(n) = |v_{RF}(n)|^2. \tag{1}$$

By minimizing the cost function: $J(n) = E[e(n)e^*(n)]$, where $(\cdot)^*$ represents the complex conjugate. The error term e(n) between the detected envelope and the input is defined as,

$$e(n) = s(n) - I(n)^2 - [\chi(n)][\eta(n)]^T, \tag{2}$$

where $\chi(n) = [\alpha^2, \alpha\cos\gamma, \alpha\sin\theta, \sigma^2, \alpha\sigma\sin(\gamma-\theta)]$ and $\eta(n) = [Q(n)^2, 2I(n), -2I(n)Q(n), 1, 2Q(n)]$. The '1' in $\eta(n)$ accounts for the magnitude of the LOFT. Thus, the vector $\chi(n)$ is trained by LMS algorithm with the step size μ which can be expressed as,

$$\chi(n+1) = \chi(n) + \mu e(n)^*\eta(n). \tag{3}$$

Thus, impairment parameters are calculated as,

$$\alpha = \sqrt{\chi_1}, \theta = \sin^{-1}\left(\frac{\chi_3}{\sqrt{\chi_1}}\right), \sigma = \sqrt{\chi_4}, \varphi = \cos^{-1}\left(\frac{\chi_2}{\sqrt{\chi_4}}\right). \tag{4}$$

Note that only the terms σ^2 in $\chi(n)$ is not correlated to the BB input which implies the HD_3 of OUT_{DET} has most of the projection on σ^2 at the LMS training stage. The timing diagram for the entire calibration is shown in Fig. 2. OUT_{DET} and the delayed BB signal are the input of the LMS algorithm. Two CORDICs operators are exploited to calculate the square root of χ_1 and χ_4 as stated in (4). For hardware savings, the CORDICs are reused twice to calculate the two divisions, arcsine and arccosine.

III. Measurement Results

The TX with a power amplifier was fabricated in 65-nm CMOS. The die photo and performance summary are depicted in Fig. 3, and the measurement setup is depicted in Fig. 4. The spectrum is observed by single-tone measurements. $\chi(n)$ has 15-bit resolution to estimate the impairment parameters. The step-size μ is designed to be 1/128. Updating $\chi(n)$ in each training step entails 8 cycles of an 80-MHz clock. $\chi(n)$ converges after 12,000 training steps (1.2 ms), which is considerably faster than the adaptive decorrelation method that requires 3 to 4 ms [2]. The measured performance is given in Fig. 5. The wideband IRR and LRR are improved from (18.9 to 29.0 dB → 41.3 to 51.1 dB) and (20.4 to 31.7 dB → 37.9 to 45.4 dB), respectively. Note that the TX's phase error is highly accurate, allowing one-shot calibration for the entire lower sub-band to save cost. The algorithm is based on a field-programmable gate array, and the required power, area and calibration time estimated in Cadence Encounter™ are given in Table I. The HD_3 of the ED mainly influences the accuracy of the LOFT estimation (Fig. 6), but not that of the I/Q imbalance. The calibrated LRRs are in good agreement with the simulation over a number of test chips [6].

IV. Conclusions

A time-domain I/Q-LOFT calibration scheme has been proposed for a sub-GHz wideband TX. Only an ED is required as the analog interface, and the parameters can be adaptively updated by using a LMS algorithm and estimated by CORDIC. One-shot calibration on wideband IRR and LRR can improve them to >41.3 dB and >37.9 dB, respectively.

Acknowledgements

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References

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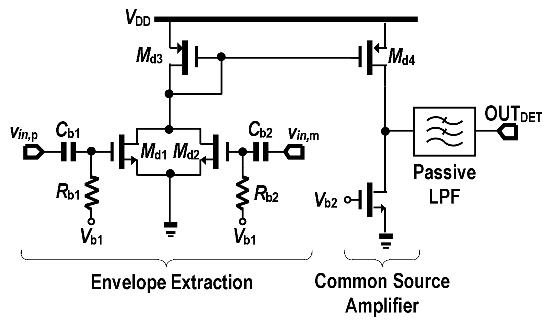


Fig. 1. The ED extracts the I/Q imbalance and LOFT. M_{d1} and M_{d2} generate the envelope of the input signal and are followed by a common-source amplifier and passive-RC lowpass filter. The 3-dB bandwidth of the latter is set at ~1 MHz to provide >65 dB rejection at the LO’s 2nd harmonic. A proper bias level (V_{b2}) ensures the detector is working in the linear region.

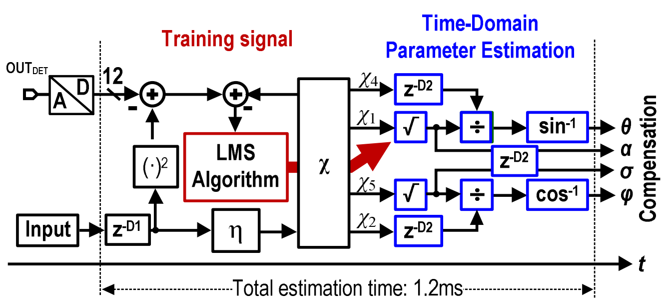
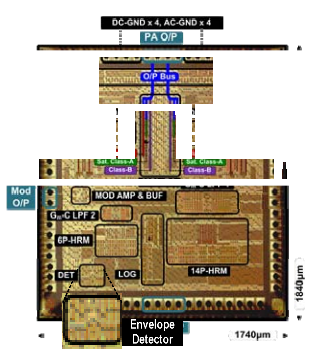


Fig. 2. Timing diagram of the proposed I/Q-LOFT calibration using time-domain parameter estimation.



	This Work
RF Range (MHz)	54 to 864
IRR/LRR (dB)	>18.9 (Before cal.) >37.9 (After cal.)
TX Power Consumption (mW)	230.4 to 240.3
OP_{1dB} (dBm)	12.5 to 16.3
Power Efficiency at OP_{1dB} (%)	7.4 to 18.5
OIP_3 (dBm)	16.1 to 27.0
Active Area (mm²)	1.03
Supply Voltage (V)	1.2, 2
Technology	65 nm CMOS

Fig. 3. Chip micrograph of the wideband TX and its performance summary.

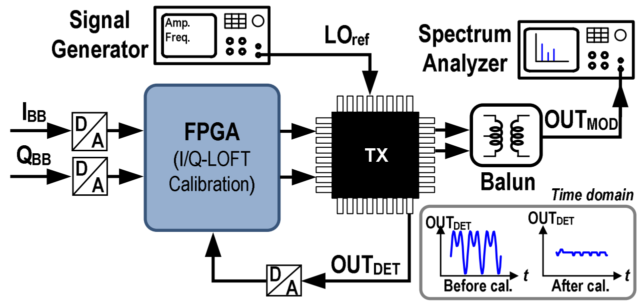


Fig. 4. Measurement setup for the I/Q-LOFT calibration scheme.

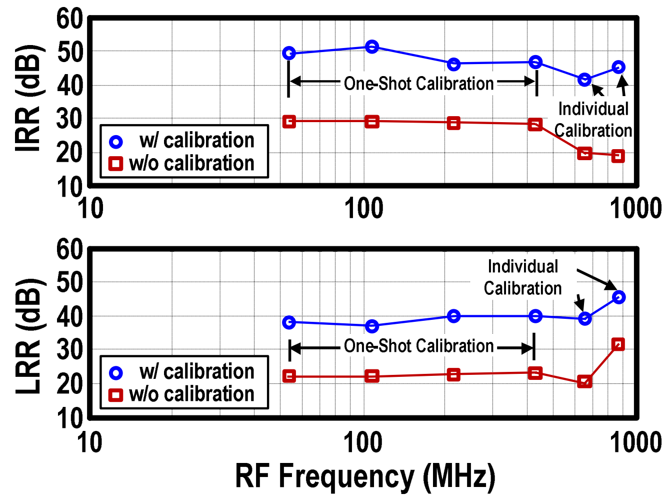


Fig. 5. Measured IRR (upper) and LRR (lower) with and without calibration.

TABLE I.
PERFORMANCE ESTIMATION OF THE I/Q-LOFT CALIBRATION ALGORITHM IN 65-NM CMOS AT 1.2 V AND 25°C.

FPGA Operation	Algorithm	Used No. of Operator	Power (μW)	No. of Gate	Area (μm²)	No. of Clock cycle
Updating Block	LMS	1	234.879	1099	4954.5	8 × 12000
Parameter Estimator and Compensator	CORDIC	2	264.631	2104	8107.3	25 × 6
	Division	2	128.233	421	1597.4	9
	Multiplication	4	90.595	371	1714.4	1
	Add	4	10.360	36	149.7	1

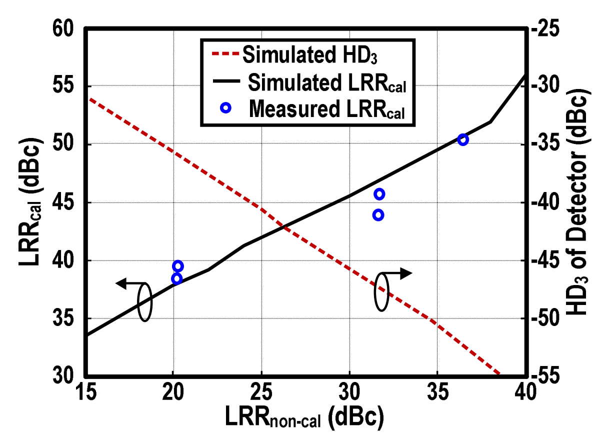


Fig. 6. The HD_3 of the ED in relationship with the non-calibrated LRR ($LRR_{non-cal}$) and calibrated (LRR_{cal})