Intermittent Polyphase SC Structures For FIR Rational Interpolation

U Seng Pan, R.P.Martins, J.E.Franca

Abstract - Rational sampling rate conversion factors *L/M* are usually obtained by cascading an L-fold upconverter followed by an M-fold downconverter. Because the traditional SC circuits employed in such cases give rise to undesired distortion effects due to the intermediary sampled-and-held signals, this paper proposes alternative solutions based on impulse sampled Intermittent Polyphase SC Structures that operate with either sampled-and-held or arbitrary input signal formats. Two alternative architectures are studied and their comparative advantages will be discussed from the viewpoints of component count and speed of the amplifiers. Behavioural level simulations illustrate well their discrete-time operation and the resulting input-output frequency responses.

I. INTRODUCTION

SAMPLED-DATA ANALOGUE sampling rate converters, namely Decimators and Interpolators, are widely used in mixed analogue and digital multirate signal processing systems [1]. Although most research efforts have been devoted until now to the design of decimators and interpolators with integer sampling rate conversion factor, respectively *M* and *L*, sampling rate converters with a rational sampling rate ratio of *L/M* are also necessary in some interface applications. In general, they can be obtained by a cascade of two integer conversions: first an increase of the sampling rate by *L* (integer interpolator) and then a decrease by *M* (integer decimator). Since both the interpolation and decimation filters are operating at the same high rate Lf_s, they can be combined into a single filter preceded by an upsampler and followed by a downsampler as shown in Fig.1.

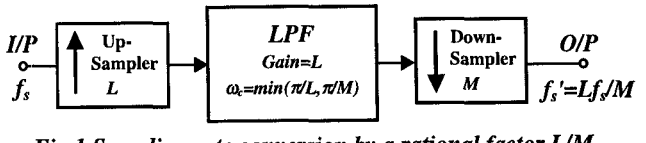

Fig.1 Sampling rate conversion by a rational factor L/M

Conventional SC circuits for integer interpolation followed by a simple downsampler can be used for realization of rational interpolators. However, additional distortion will exist in the overall frequency response caused by the Sample-and-Hold (S/H) filtering effect at lower input sampling rate [2-4]. Therefore, only the recently proposed Impulse Sampled SC Interpolators without input S/H filtering effect can be employed for such technique of rational interpolation [5-8]. Since such scheme is not efficient enough in terms of power and silicon consumption for high speed of operation, we propose in this paper improved solutions based on new Intermittent Polyphase Structures. Two alternative architectures and their comparative advantages in terms of component count and speed of the amplifiers are investigated. Behavioural level simulations verify well their discrete-time operation and the resulting input-output frequency responses.

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II. INTERMITTENT POLYPHASE STRUCTURES

For clarity of explanation, we consider an FIR interpolator with rational conversion ratio of *4/3* and output sampling rate of *2MHz*. The proposed architecture combines an impulse sampled 4-fold SC interpolator followed by a simple 3-fold downsampler (switch S) as illustrated in the diagram given in Fig.2. The coefficients of the impulse response of the 4-fold interpolator are depicted in Fig.3.

Referring to the clock waveforms also depicted in Fig.2, the impulse sampled 4-fold SC interpolator implemented with Active-Delayed Block (ADB) Polyphase Structures produces 4 output samples at $1/f_s$

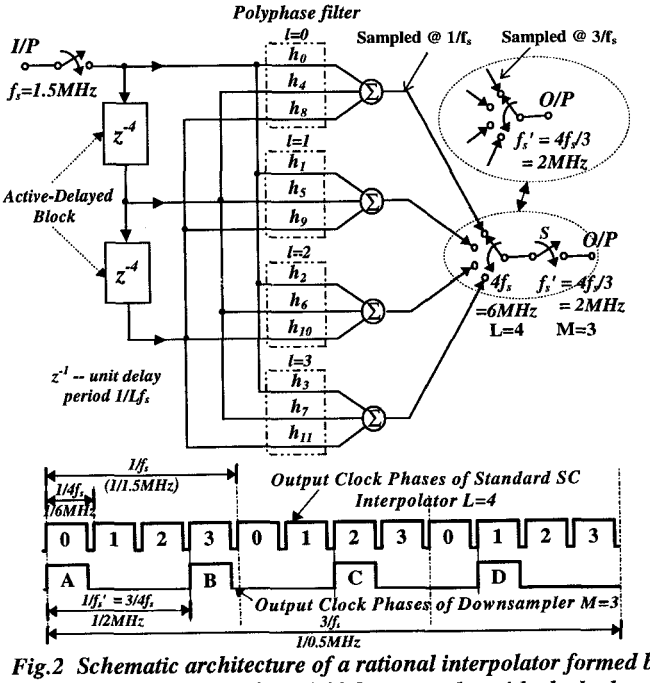

Fig.2 Schematic architecture of a rational interpolator formed by a 4-fold interpolator and a 3-fold downsampler with clock phases

(*1/1.5MHz*), respectively during clock phases 0, 1, 2 and 3 for each polyphase filter [6-8]. However, the downsampler only keeps every 3rd output sample from the interpolator at clock phase A, B, C or D. Therefore, the output-fast commutator operating at $4f_s$ and the slower downsampler operating at $4f_s/3$ can be simplified to a single slow commutator at $4f_s/3$ as indicated in Fig.2. Here, only those interpolated values that correspond to the output time grid need to be computed. For instance, the slow commutator samples the polyphase filter l=0 at clock phase A for every $3/f_s$ even though the filter normally generates 3 samples during $3/f_s$. By analogy, the polyphase filters l=1, 2 and 3 all need to produce only 1 sample at clock phase D, C and B respectively, in the period of $3/f_s$. For the rest of the time, such polyphase filters are in an "idle" status similar to an operation in an intermittent mode. Such an efficient switching scheme suggests the designation of Intermittent Polyphase Structures for those structures. The possible forms of SC implementation are discussed next, one using L-Slow-Output-Accumulator and the other using only One-Fast-Output-Accumulator.

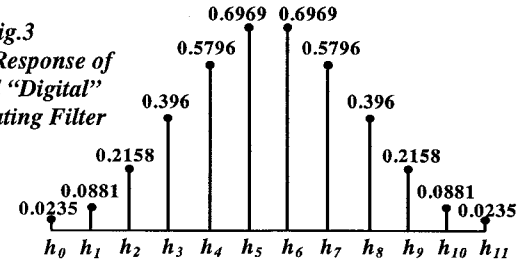

Fig.3 Impulse Response of Original "Digital" Interpolating Filter

III. USING L-SLOW-OUTPUT-ACCUMULATOR

In the Intermittent Polyphase filters, the passive SC branches with normalised capacitance values only sample, weigh, delay and transfer the input signals once per $3/f_s$. This allows the increase of time interval for charge transfer to the Operational Amplifiers (OA)'s, thus relaxing their speed requirements. The overall SC circuit architecture and the corresponding clock phases are derived in Fig.4(a) and (b) respectively. The upper two Active-Delayed-Blocks (ADB), formed by the OA with input and feedback/reset PCTSC branches, are a serial processing delay line for generating the delay of z^{-4} with the unit delay period $1/4f_s$. Since each polyphase filter has its own output accumulator, the settling time of the OA in the accumulator is close to $11/4f_s$ which is at least M or

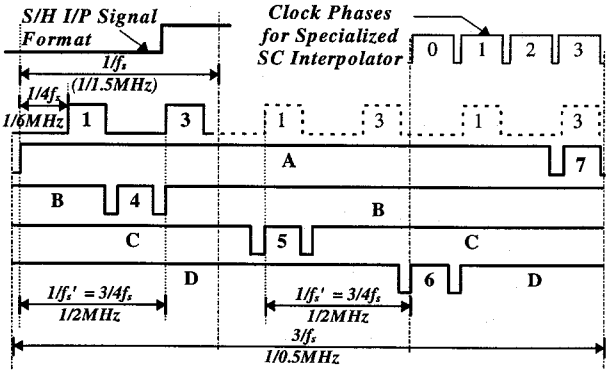

Fig. 4(b)

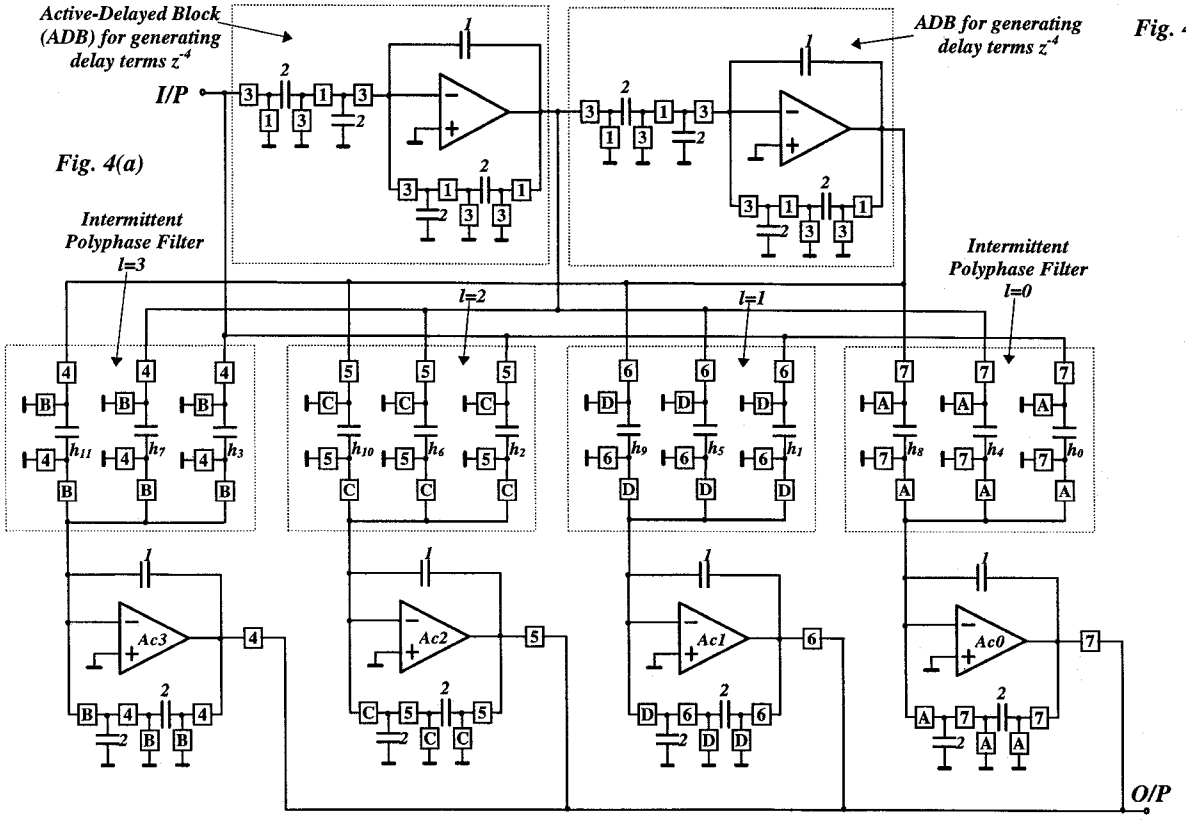

Fig. 4(a)

Fig.4 SC Interpolator with Rational Factor 4/3 with L-Slow-Output-Accumulators (a) SC Implementation (b) Clock Phases

ML-1 times longer than that in specialised SC interpolators [8]. The output switches with clock phases 4, 5, 6 and 7 constitute a simple output commutator at $4/3f_s$. The SC branches in polyphase filters sample the input signals at clock phases 4, 5, 6 and 7 which correspond to the same time grid of 0, 1, 2 and 3 in a specialised interpolator [8]. Thus, in order to guarantee the same input sampling value, both the input and output signals of ADB's must be strictly sampled-and-held at clock phase 3 with input lower sampling rate f_s. Consequently, the settling time of OA's in ADB's must be $1/4f_s$ which is considerably shorter than that in the accumulators.

IV. Using One-Fast-Output-Accumulator

In order to overcome the limitations of the previous circuit in terms of relaxing settling time requirements of the OA's in ADB's and allowing arbitrary input signal formats, a second circuit architecture with fewer clock phases is presented in Fig.5. Here, instead of the L slow output accumulators, only one faster output accumulator is employed. In this approach, each polyphase filter waits for its turn to transfer charge to the same output accumulator. The previous charges stored in the accumulator have to be reset when the next polyphase filter is activated. Thus the longest charge transfer time or the settling time of OA in accumulator, that also functions as a commutator, is close to $1/f_s'=3/4f_s$ which is still longer than that in the typical impulse sampled SC interpolator [8]. Due to the reduction of charge transfer time of SC branches in the Intermittent Polyphase filters which generate one sample for every $3/f_s$, as discussed before, the sampling time restriction of the SC branches can be relaxed. Therefore, the settling time of OA's in ADB's can be extended to $1/2f_s$ due to the increase of phases 3 and 1 to half of the lower input sampling period. Besides, since the sampling time of SC branches is at phase 4, 5 and 6 which correspond to the same time grid of phase 3, the input signals no longer need to be sampled-and-held. However, the total capacitance area will be slightly increased, since the capacitors associated with each OA of each accumulator in the previous Architecture 1 can be scaled separately, which is not possible in this architecture where all the capacitors are connected to the same input node of the OA in the output accumulator. In Table I, we show the comparison among different types of rational interpolators in terms of the most important parameters.

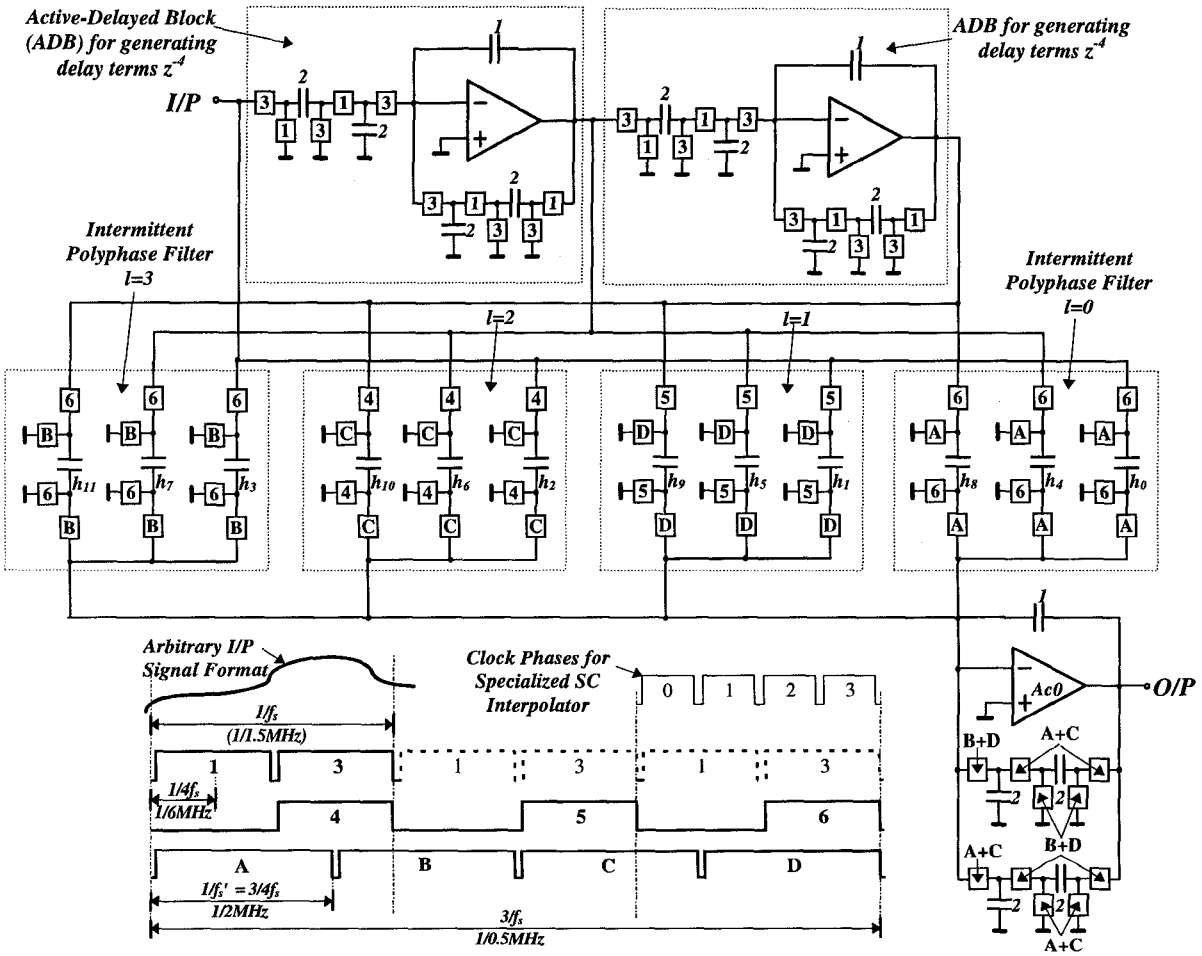

Fig.5 SC Interpolator with Rational Factor 4/3 with One-Fast-Output Accumulator

TABLE I	Passband Distortion by Input S/H Effect	Speed in terms of Settling Time of OA	Capacitance Area	I/P Signal Formats
Conventional SC Interpolator + Downsampler	Yes	$\frac{1}{2}\cdot\frac{1}{Lf_s}$	$> C_{total}$	S/H at f_s
Impulse sampled ADB Polyphase SC Interpolator (One-Output-Accumulator) with Downsampler	No	$\frac{1}{Lf_s}$ (OA's in ADB's and one Accu.)	C_{total}	Arbitrary
ADB Intermittent Polyphase SC Rational Interpolator (L-Slow-Output-Accumulator)	No	$\frac{1}{Lf_s}$ (OA's, in ADB's) $\frac{LM-1}{Lf_s}$ (L OA's. in L Accu.)	$< C_{total}$	S/H at f_s
ADB Intermittent Polyphase SC Rational Interpolator (One-Fast-Output-Accumulator)	No	$\frac{2}{Lf_s}$ (OA's, in ADB's) $\frac{1}{f_s'}=\frac{M}{Lf_s}$ (OA in 1 Accu.)	C_{total}	Arbitrary

V. COMPUTER SIMULATED RESULTS

To verify the behaviour of the above SC rational interpolators, we analysed the resulting computer simulated overall amplitude responses of both architectures, that are exactly identical: one obtained with input sampled-and-held signal (L-Slow-Output-Accumulator) and the other with arbitrary signal formats (One-Fast-Output-Accumulator) as illustrated in curve I of Fig.6. When the output sample-and-hold effect at higher sampling rate $4f_s/3=2MHz$ is considered, the amplitude response is also plotted in curve II with the additional zeros at *2MHz*, *4MHz* and *6MHz*. The spectrum analysis is also presented in Fig.7(a) and (b). Fig.7(a) illustrates the spectra of output interpolated signals with the corresponding input signal frequency ranging from *0* to *1MHz*. Obviously, the output spectra replicate at the multiples of $f_s'=2MHz$. The detailed output spectra including the aliasing components are also illustrated in Fig.7(b), i.e. the spectra at *375kHz* and *3.625MHz* are the aliasing components caused by the downsampling

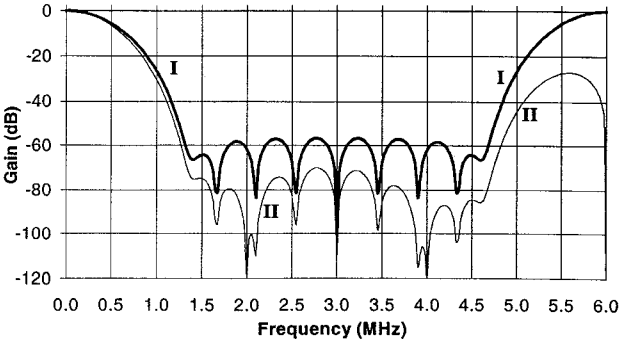

Fig. 6 Overall Computer Simulated Amplitude Response

operations. Indeed, they are derived from the frequency-translated imaging component at *1.65MHz* of the original *125kHz* input signal sampled at *1.5MHz* that has already been attenuated by the interpolating filter to *-71.7dB*.

VI. CONCLUSIONS

Two new Intermittent Polyphase SC structures for rational sampling rate conversion have been proposed. The structure using L-Slow-Output-Accumulator needs slower output accumulators but faster ADB's and requires an input S/H signal format. By contrast, the structure using One-Fast-Output-Accumulator needs fewer OA's and slower ADB's and allows arbitrary input signal formats at the expense of one faster accumulator and a slightly larger capacitance area. Computer simulated amplitude responses and output spectra have been shown to illustrate the operation and response of such new SC circuits and techniques which can also be applied in other rational sampling rate converters.

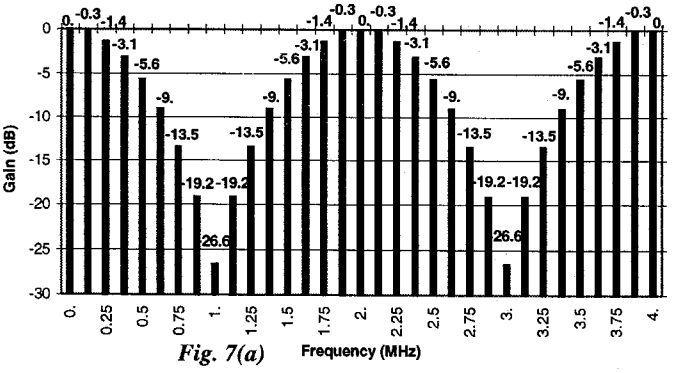

Fig. 7(a)

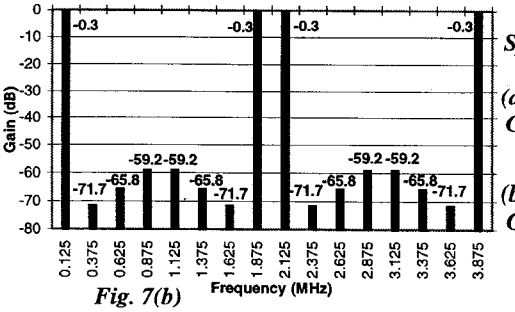

Fig. 7(b)

Fig.7 Spectrum Analysis

(a) Output Spectra Given by 0-1MHz Input Signals

(b) Output Spectra Given by 125KHz Input Signal

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