An All-Factor Modulation Bandwidth Extension Technique for Delta-Sigma PLL Transmitter

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Abstract— **In this work, an all-factor modulation bandwidth extension technique for one-point delta-sigma (ΔΣ) phase locked loop (PLL) transmitter is presented. The factors that need to be calibrated have been discussed. Firstly, *RC* variation of the loop filter is compensated by using an *RC* tracking circuit. Secondly, variation of the loop gain of the modulator is calibrated by sensing the magnitude differences between its values at DC and high frequency. Since two critical factors of PLL are calibrated, the proposed technique can achieve higher calibration accuracy. Moreover, this technique has been proven to be valid for all PLL types and orders by theoretical analyses given in this paper. And one particular case has been verified by measurement results.**

Keywords—Delta-sigma; transmitters; phase locked loop (PLL); modulation bandwidth extension.

I. INTRODUCTION

One-point delta-sigma (ΔΣ) modulation phase-locked loop (PLL) transmitter (as shown in Fig. 1(a)) has been widely used due to its low noise, low power consumption and reduced complexity [1], comparing to direct up-conversion [2] and offset PLL ones. However, with the low-pass characteristic of the PLL, the maximum achievable data rate of this transmitter is limited [1]. When the loop bandwidth is smaller than the modulation bandwidth, the modulation accuracy is deteriorated due to the shrinkage of signal spectrum. On the other hand, with larger loop bandwidth, the phase noise and spurious emission are less attenuated. Hence, the modulation bandwidth extension without noise degradation is highly favored.

In previous works, the low-pass feature of the PLL was compensated by cascading a digital pre-emphasis filter having the transfer function inverse of the PLL. However, under process, voltage and temperature (PVT) variations, the mismatch between the digital filter and the analog PLL will degrade the modulation accuracy. To tackle this issue, several techniques [3]-[6] have been proposed.

In [3], a scalable charge pump current (I_{cp}) was employed to compensate the loop gain error. With an over-damped, 2nd order loop filter, the loop gain error can be compensated by sensing the voltage-controlled oscillator (VCO) sensitivity (K_v)
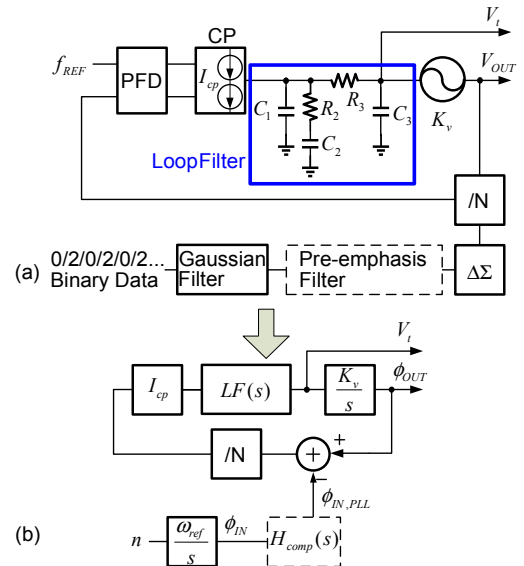
Fig. 1 (a) Block diagram of one-point ΔΣ PLL transmitter with a 3rd order loop filter. (b) Linear model of the ΔΣ PLL transmitter.

error and setting I_{cp} accordingly. However, this technique is only applicable to limited PLL types and orders. Another loop compensation technique is reported in [4], where the loop filter *RC* variation was approximated as a pseudo loop gain error and calibrated simultaneously with the original loop gain error. However, under certain *RC* variations, this pseudo approximation might not achieve an even magnitude-frequency response within the modulation bandwidth. Moreover, a less than ±2% scalable I_{cp} resolution was required in this design, which increases the design difficulty in nanometer CMOS technologies.

In view of supporting multiple PLL types/orders with all factors calibrated, a new calibration technique with less complexity is proposed in this work. Following by the introduction, Section II illustrates the factors that need to be calibrated. Section III describes the proposed calibration scheme and its implementation. Then section IV discusses the application of the proposed technique to other PLL type/order, and conclusion is drawn in Section V.

II. FACTORS TO BE CALIBRATED

A conventional one-point $\Delta\Sigma$ PLL transmitter is shown in Fig. 1(a), consisting of phase-frequency detector (PFD), charge pump (CP), loop filter (type-II, third-order here), VCO and divide-by-N divider. The division ratio of the divider is controlled by the output of the $\Delta\Sigma$ modulator, which modulates the Gaussian-filtered binary data. The linear model of this $\Delta\Sigma$ PLL transmitter is presented in Fig. 1(b), and its closed-loop transfer function equals to

$$H_o(s) = \frac{K(1+T_2 s)}{A_2 s^4 + A_1 s^3 + A_0 s^2 + K(1+T_2 s)}, \quad (1)$$

where
$$\begin{aligned}
A_2 &= C_1 C_2 C_3 R_2 R_3 \\
A_1 &= C_2 C_3 R_2 + C_1 C_2 R_2 + C_1 C_3 R_3 + C_2 C_3 R_3 \\
A_0 &= C_1 + C_2 + C_3 \\
T_2 &= C_2 R_2 \\
K &= I_{cp} K_v / N
\end{aligned} \quad (2)$$

A_2–A_0 and T_2 are the loop-filter-related coefficients, I_{cp} is the CP current, and K_v represents the VCO sensitivity.

As discussed in section I, the transmitted data is pre-emphasized by a digital filter (shown as the dashed box in Fig. 1(a)) with an inverse transfer function of $H_o(s)$. For more convenient analysis, this discrete digital pre-emphasis filter can be replaced by its equivalent continuous-time model [7]. Hence, the transfer function of the pre-emphasis filter should be given by:

$$H_{comp}(s) = \frac{A_{2d} s^4 + A_{1d} s^3 + A_{0d} s^2 + K_d(1+T_{2d} s)}{K_d(1+T_{2d} s)}, \quad (3)$$

where A_{2d}, A_{1d}, A_{0d}, T_{2d} and K_d are the digital loop coefficients denoted by the subscript d. Combining (1) and (3), the modulation transfer function can be expressed as

$$\begin{aligned}
H(s) &= H_o(s) H_{comp}(s) \\
&= \frac{\left[A_{2d} s^4 + A_{1d} s^3 + A_{0d} s^2 + K_d(1+T_{2d} s)\right]\left[K(1+T_2 s)\right]}{\left[A_2 s^4 + A_1 s^3 + A_0 s^2 + K(1+T_2 s)\right]\left[K_d(1+T_{2d} s)\right]}
\end{aligned} \quad (4)$$

Assume the resistors, capacitors, and K are α, β, γ times of their nominal values respectively, as in (5):

$$A_2 = \alpha^2 \beta^3 A_{2n}, A_1 = \alpha\beta^2 A_{1n}, A_2 = \beta A_{0n}, T_2 = \alpha\beta T_{2n}, K = \gamma K_n, (5)$$

where subscript n denotes the nominal value. Then the total RMS phase error ϕ_{RMS} of the modulator is calculated as:

$$\phi_{RMS} = \frac{180^o}{\pi}\sqrt{2\int_0^\infty \left[\left(\frac{\pi}{2}\right)^2 \left|\frac{1-H(s)}{s}\right|^2 f_{SYM}\right]df + S_{un-mod}}, \quad (6)$$

where f_{SYM} represents the transmission symbol rate, and S_{un-mod} denotes the un-modulated phase error variance. The simulated ϕ_{RMS} versus α, β and γ variations is shown in Fig. 2. It can be found that the γ variation causes the largest RMS phase error degradation. Besides, the variations of α and β also contribute
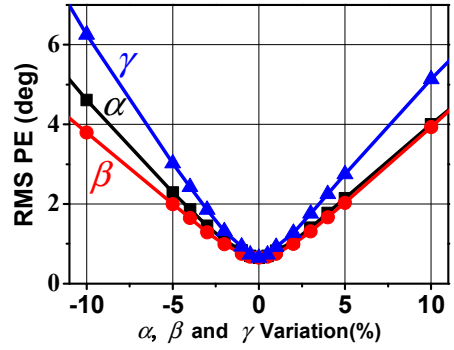

Fig. 2 Simulated RMS phase error (PE) ϕ_{RMS} under α, β and γ variation. under different β variations of 0, 5% and 10%, respectively.

with a significant part. As a result, all the α, β and γ variations should be calibrated for a low ϕ_{RMS}. Another significance of (6) is that ϕ_{RMS} caused by the digital-analog mismatch is theoretically eliminated if $H(j\omega)=1$ $(\omega<<2\pi\cdot f_{SYM})$.

III. PROPOSED TECHNIQUE AND IMPLEMENTATION

A. Proposed Techinque

When combining (5) to (4), H(s) can be rewritten as:

$$\begin{aligned}
H(s) &= \frac{\gamma K_n(1+\alpha\beta T_{2n} s)}{K_d(1+T_{2d} s)} \\
&\cdot \frac{A_{2d} s^4 + A_{1d} s^3 + A_{0d} s^2 + K_d(1+T_{2d} s)}{\alpha^2\beta^3 A_{2n} s^4 + \alpha\beta^2 A_{1n} s^3 + \beta A_{0n} s^2 + \gamma K_n(1+\alpha\beta T_{2n} s)}
\end{aligned} \quad (7)$$

To make $H(j\omega)=1$ $(\omega<<2\pi\cdot f_{SYM})$, the following terms should be met.

$$A_{2d} = (\alpha\beta)^2 A_{2n}, A_{1d} = (\alpha\beta) A_{1n}, A_{0d} = A_{0n}, T_{2d} = (\alpha\beta) T_{2n}, \quad (8)$$

and
$$K_d = \gamma / \beta K_n \quad (9)$$

As a result, to design the loop-filter-related coefficients A_{2d}–A_{0d}, and T_{2d} based on (8), the product of α and β should be found. This is achieved by tracking the RC constant variation from its nominal value. For finding γ/β and meeting (9), it is realized by measuring the differences of the magnitude-frequency response between DC and high frequency as follows.

If (8) is firstly achieved and K_d is initially set to its nominal value K_n, (7) is rewritten as:

$$\begin{aligned}
H(s) &= \frac{\gamma K_n(1+\alpha\beta T_{2n} s)}{K_n(1+\alpha\beta T_{2n} s)} \\
&\cdot \frac{\alpha^2\beta^2 A_{2n} s^4 + \alpha\beta A_{1n} s^3 + A_{0n} s^2 + K_n(1+\alpha\beta T_{2n} s)}{\beta\left(\alpha^2\beta^2 A_{2n} s^4 + \alpha\beta A_{1n} s^3 + A_{0n} s^2\right) + \gamma K_n(1+\alpha\beta T_{2n} s)}
\end{aligned} \quad (10)$$

For a calibration frequency ω_c much higher than PLL's loop bandwidth ω_0, the s^4 terms will dominate in both nominator and denominator of (10). On the other hand, for a DC signal,

the s^0 terms dominate. As such, the value of γ/β can be approximated as:

$$\frac{\gamma}{\beta} \approx \frac{\left|H\left(j\omega_c\right)\right|}{\left|H\left(j\omega_{dc}\right)\right|}, \text{if } \omega_c \gg \omega_0 . \qquad (11)$$

In this work, to simplify the detection procedure, the modulation index is detected based on the loop filter output (V_t as shown in Fig. 1(b)). A calibration pattern $A[sin(\omega_c t)+1]$, with both amplitude and DC equal to A, is fed to the modulator input (n in Fig. 1(b)) during the calibration, and the input phase is thus given by:

$$\phi_{IN} = A\omega_{ref} \int \left(\sin\omega_c t + 1\right) dt . \qquad (12)$$

The output phase, which is equal to $\phi_{IN}|H(s)|$, is depicted as

$$\phi_{OUT} = A\omega_{ref} \int \left(\left|H\left(j\omega_c\right)\right|\sin\omega_c t + \left|H\left(j\omega_{dc}\right)\right|\right) dt . \qquad (13)$$

Hence, the voltage shift ΔV_t observed on V_t is:

$$\Delta V_t = \frac{1}{K_v} \cdot \frac{d\phi_{OUT}}{dt} = \frac{A\omega_{ref}}{K_v}\left(\left|H\left(j\omega_c\right)\right|\sin\left(\omega_c t\right) + \left|H\left(j\omega_{dc}\right)\right|\right),(14)$$

where $A\omega_{ref}/K_v|H(j\omega_c)|$ represents the amplitude of V_t, while its DC deviation is given by $A\omega_{ref}/K_v|H(j\omega_{dc})|$ term. Therefore, γ/β can be further derived as:

$$\frac{\gamma}{\beta} \approx \frac{\left|H\left(j\omega_c\right)\right|}{\left|H\left(j\omega_{dc}\right)\right|} = \frac{V_t \text{ amplitude}}{V_t \text{ DC deviation}}, \text{if } \omega_c \gg \omega_0 \qquad (15)$$

B. Implementation

This calibration procedure, divided into three stages, was simulated with Simulink. And its result is shown in Fig. 3.

Stage 1: When calibration starts, a calibration data pattern of 0/2/0/2/0/2/… at a frequency of ω_c is applied to the modulator input. This pattern ensures both the amplitude and DC value of the signal to be 1 unit. As such, a sine wave, together with a DC deviation, will be expected on V_t. The RC tracking is also performed in this stage to find out $\alpha\beta$ and to adjust respective coefficients. In the meanwhile, K_d is set to its nominal value K_n.

Stage 2: After PLL tracks the calibration data pattern stably, the waveform of V_t is measured. In the ideal case, if $H_{comp}(s)$ matches PLL transfer function $H_o(s)$, the measured amplitude of V_t should be equal to its DC deviation. Here, the DC value of the calibration data (V_{DC1}) is obtained by averaging out the V_t voltage over a number of periods. As for V_t amplitude, it is done by subtracting V_{DC1} from its peak value V_{peak}.

Stage 3: The calibration data pattern is terminated in this stage. As a result, PLL will lock to a carrier frequency for the coming transmission, and V_t will stabilize to the respective DC value (V_{DC2}). This DC value is also measured, and the DC
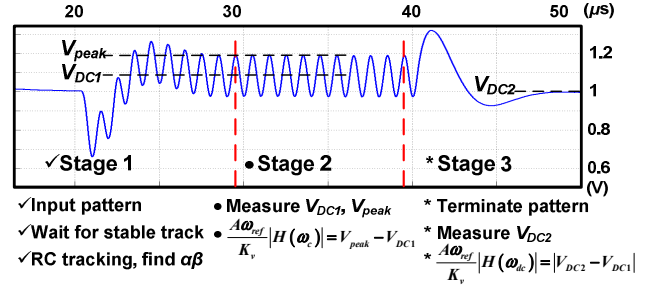

Fig. 3 The simulated calibration output V_t.

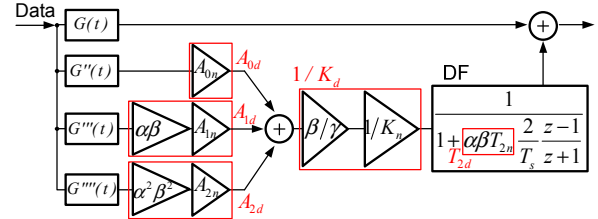Fig. 4 Simplified block diagram of the proposed digital pre-emphasis filter

deviation during calibration can be calculated as $|V_{DC2}-V_{DC1}|$. Thereby, the value of γ/β is obtained based on (15) and K_d is adjusted accordingly. All the voltage measurements are done by a $\Delta\Sigma$ analog-to-digital converter (ADC) [8]. After that, the calibration mode ends, and the transmitter is ready for transmission.

With these stages, (8) and (9) are met and the limited modulation bandwidth can be extended. The simplified block diagram of the proposed GMSK & pre-emphasis digital filter is shown in Fig. 4. $G(t)$ represents the Gaussian filter, while $G''(t)$, $G'''(t)$ and $G''''(t)$ represent the second, third and fourth order derivative of $G(t)$, respectively. The outputs of $G''(t)$, $G'''(t)$ and $G''''(t)$ are multiplied with digital coefficients A_{0d}, A_{1d}, and A_{2d}, and then summed up and amplified by $1/K_d$. The result is then applied to a digital filter DF (corresponding to the $1+T_2s$ term in (1)) and added to the output of Gaussian filter $G(t)$. A_{0d}, A_{1d}, A_{2d}, T_{2d} and K_d are designed in the same configurations as in (8) and (9).

IV. APPLICATIONS TO OTHER PLL

A. Type-I, second-order PLL

The closed-loop transfer function of a type-I, second-order PLL and digital pre-emphasis filter are depicted as:

$$H_0\left(s\right) = \frac{K}{As^2+s+K} \text{ and } H_{comp}\left(s\right) = \frac{A_d s^2 + s + K_d}{K_d}, \qquad (16)$$

where $A = \alpha\beta A_n$ and $K = \gamma K_n$. Then the modulation transfer function is given by:

$$H\left(s\right) = H_0\left(s\right)H_{comp}\left(s\right) = \frac{\gamma K_n\left(A_d s^2 + s + K_d\right)}{K_d\left(\alpha\beta A_n s^2 + s + \gamma K_n\right)}, \qquad (17)$$

which will exhibit an even transfer function if:

$$A_d = \alpha\beta A_n, K_d = \gamma K_n . \qquad (18)$$

Once the *RC* tracking is performed and $\alpha\beta$ value is found out, A_d is pre-distorted to $\alpha\beta A_n$. After that, setting K_d to its nominal value K_n, γ can be obtained by the method in Section III. Therefore, the proposed calibration can be applied to a Type-I, second-order PLL.

B. Type-II PLL

Fig. 5 shows a typical N^{th}-order PLL loop filter. The close loop transfer function $H_0(s)$ with this loop filter is given by:

$$H_o(s) = \frac{K(1+T_2 s)}{s \cdot \sum_{i=1}^{N} C_i \cdot (1+T_1 s) \cdot \prod_{k=2}^{N-1}(1+T_k s) + K(1+T_2 s)}, \quad (19)$$

where

$$T_1 = \frac{C_1 C_2 R_2}{C_1 + C_2}, \quad (20)$$

and T_k represents the pole in the loop filter. With the transfer function $H_{comp}(s)$ inverse of (19), and replacing the analog variables with their nominal values and the variations α, β, γ, $H(s)$ is given as:

$$H(s) = \frac{\gamma K_n(1+\alpha\beta T_{2n}s)}{K_d(1+T_{2d}s)}$$
$$\cdot \frac{s \cdot \sum_{i=1}^{N} C_{id} \cdot (1+T_{1d}s) \cdot \prod_{k=2}^{N-1}(1+T_{kd}s) + K_d(1+T_{2d}s)}{s \cdot \beta \sum_{i=1}^{N} C_{in} \cdot (1+\alpha\beta T_{1n}s) \cdot \prod_{k=2}^{N-1}(1+\alpha\beta T_{kn}s) + \gamma K_n(1+\alpha\beta T_{2n}s)} \quad (21)$$

When the value of $\alpha\beta$ is tracked by the *RC* constant tracking, T_{id} is set to $\alpha\beta T_n$. Hence, setting C_{id} and K_d to their nominal values, $H(s)$ turns out to be:

$$H(s) = \frac{\gamma K_n(1+\alpha\beta T_{2n}s)}{K_n(1+\alpha\beta T_{2n}s)}$$
$$\cdot \frac{s \cdot \sum_{i=1}^{N} C_{in} \cdot (1+\alpha\beta T_{1n}s) \cdot \prod_{k=2}^{N-1}(1+\alpha\beta T_{kn}s) + K_d(1+\alpha\beta T_{2n}s)}{s \cdot \beta \sum_{i=1}^{N} C_{in} \cdot (1+\alpha\beta T_{1n}s) \cdot \prod_{k=2}^{N-1}(1+\alpha\beta T_{kn}s) + \gamma K_n(1+\alpha\beta T_{2n}s)} \quad (22)$$

Due to (22) is with the same format as (10), the value of γ/β is obtained by running the γ/β tracking as well, and the digital-analog mismatch is calibrated thereby. Hence, the proposed method is valid for type-II PLLs.

A comparison, among the proposed work and the state-of-art modulation bandwidth extension techniques, is presented in Table I. As can be seen, this work calibrates all the factors of the PLL loop, and thus can achieve comparable or better calibration accuracy. In addition, this work is the only technique that can cover all the PLL types and orders.

The proposed modulation bandwidth calibration technique, together with a one-point $\Delta\Sigma$ modulation PLL transmitter, was fabricated in a 0.18-μm CMOS process. The measurement results [9] show that this technique achieves a maximum RMS phase error of 0.8°, because of the proposed all-factor
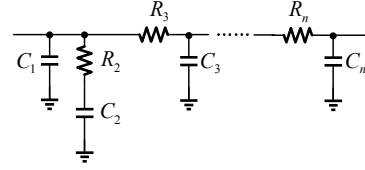

Fig. 5 N^{th}-order PLL Loop Filter.

TABLE I. Performances Comparison with State-of-art Works

	[3]	[4]	[5]	[6]	This work
Calibrated Factors	Loop gain	Loop gain	*RC*, Loop gain	*RC*, Loop gain	***RC*, Loop gain**
PLL type	I	II	I	I	**All**
PLL order	2nd	3rd	2nd	2nd	**All**

calibration. The measured respective calibration accuracy is 0.5% and 0.8%, for *RC* and γ/β tracking, respectively.

V. Conclusion

An all-factor modulation bandwidth extension technique for one-point $\Delta\Sigma$ PLL transmitter is proposed in this work. The factors needed to be calibrated have been discussed. And then the proposed technique and implementation are presented. This technique can achieve higher accuracy because of its calibration on all PLL factors. Moreover, the effectiveness of applying this technique to all PLL types/orders has been proven by the theoretical analyses. The proposed technique has been verified by the measurement results on a type II, 3rd order case.

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