Multi-range, Ultra-lower Power, -20 to 60°C CMOS Smart Temperature Sensor with ±0.1°C Accuracy

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***Abstract*—This paper presents a multi-range ultra-lower power high accuracy CMOS smart temperature sensor based on substrate BJTs and a first-order incremental delta-sigma analog-to-digital converter (ΔΣ-ADC) targeting on applications where accuracy and power have higher priority over the sensing range and speed requirement. By using a reconfigurable pre-gain stage, the input range of the ΔΣ-ADC can be optimized for different application specific temperature sub-ranges, relaxing the resolution as well as power requirements for subsequent analog-to-digital conversion. High accuracy with reduced control circuit complexity is achieved through the use of dynamic element match (DEM) and multi-cycle integration. The proposed CMOS temperature sensor is designed for three temperature sub-ranges (-20°C to 7°C, 5°C to 35°C, and 33°C to 60°C) using a standard 0.18μm CMOS technology. An inaccuracy of ±0.1°C is achieved in all the three sub-ranges using only one-point calibration while consuming 1μW.**

I. INTRODUCTION

Compared to the traditional temperature sensors using discrete devices like thermistors or platinum resistors, smart temperature sensors based on low-cost standard CMOS technology are becoming more and more popular as the sensor interface electronic can be fabricated in a single chip, producing a readily interpretable temperature reading in a digital format. Various CMOS temperature sensor designs with high accuracy, ultra-low power, wide sensing range and fast conversion for various applications have already been demonstrated [1-4].

Recently, smart temperature sensors are widely applied to many emerging areas, such as chip temperature monitoring for protecting integrated electronic systems from overheating to ensure long-term reliability [1], cold-chain temperature tracking for goods preservation [2-3], human body temperature monitoring for improved healthcare [4], as well as ambient temperature sensing for smart home systems. These new applications necessitate various design specifications, and generally require ultra-low power consumption for extended operation lifetime and high accuracy for precise temperature measurement. The sensing range requirement, however, is more relaxed as it is becoming to a great extent application defined (e.g. cold chain monitoring and biomedical applications). By optimizing the temperature sensing range with the full-range of the ADC, the ADC resolution and bandwidth requirements to achieve high temperature accuracy can be much relaxed, resulting in an ultra-low power high accuracy CMOS temperature sensor design. Yet, a limited sensing range can restrain the possible application areas.

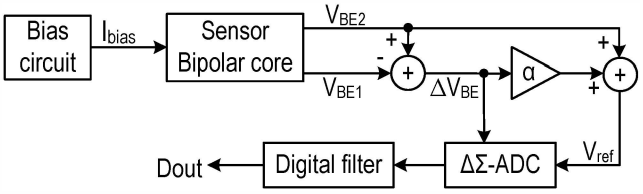

Fig. 1 Working principle of a conventional smart temperature sensor.

This paper presents a multi-range ultra-low power high accuracy CMOS smart temperature sensor covering three different temperature sub-ranges, i.e. low temperature sub-range (L) from -20°C to 7°C, medium temperature sub-range (M) from 5°C to 35°C, and high temperature sub-range (H) from 33°C to 60°C, while preserving an accuracy of ±0.1°C in every sub-range. This is achieved by integrating a pre-gain stage [5] into a first-order incremental ΔΣ-ADC. Temperature data feedback is utilized to automatically reconfigure the pre-gain stage to switch between different sub-ranges while preserving high sensing accuracy with ultra-low power consumption. Different sampling frequency to compensate for the temperature effect has also been exploited to optimize the power efficiency and accuracy of the integrator. A multi-cycle integration scheme is introduced to reduce the excessive control overhead of the pre-gain stage.

This paper is organized as follows. Section II illustrates the sensor operation principle. Section III describes the circuit techniques while simulation results are showed in Section IV. Section V draws the conclusions.

II. OPERATION PRINCIPLE

A ratiometric readout scheme, which is a ratio of the temperature dependent signal to the reference signal, is employed to produce a readily interpretable temperature reading in a digital format. For a smart temperature sensor, the bipolar junction transistor (BJT) temperature-characteristic [6] is utilized to generate this ratio. The temperature reading can be obtained by a "one-shot" operation offered by an incremental ΔΣ-ADC. Fig. 1 illustrates the operation principle of BJT-based temperature sensor.

A. Conventional Structure

Fig. 2 shows two identical diode-connect BJTs $Q_{1,2}$ biased

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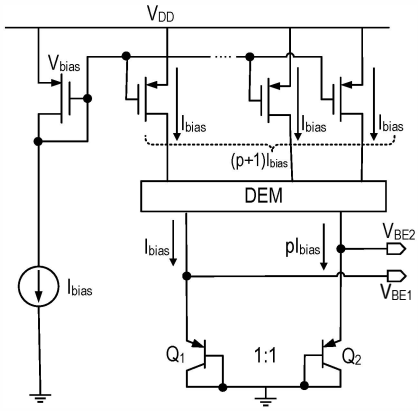

Fig. 2 Simplified analog front end of the proposed temperature sensor.

by a $1:p$ current ratio to generate two complementary-to-absolute-temperature (CTAT) voltages as follows:

$$V_{BE1} = \frac{kT}{q} ln \frac{I_{C1}}{I_{S1}} \quad (1)$$

$$V_{BE2} = \frac{kT}{q} ln \frac{I_{C2}}{I_{S2}} \quad (2)$$

where I_{C1}, I_{C2}, I_{S1} and I_{S2} are the corresponding collector currents and saturation currents of the two BJTs, k is the Boltzmann constant, q is the electron charge and T is the temperature in $°K$. The difference between the two CTAT voltages is proportional-to-absolute-temperature (PTAT):

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} ln\, p \quad (3)$$

As shown in Fig. 1, the V_{BE2} and ΔV_{be} voltages can be linearly combined to generate a temperature independent reference signal V_{ref}, where α is a fixed gain factor to balance the positive and negative temperature coefficients. The digital ratio μ is scaled to temperature T and can be obtained by ΔΣ-ADC, which can be expressed as:

$$\mu = \frac{\alpha \Delta V_{BE}}{V_{BE2} + \Delta V_{BE}} \quad (4)$$

Finally, μ can be scaled back to represent the instantaneous temperature data (D_{out}) in $°C$ through a digital filter:

$$D_{out} = A\mu + B \quad (5)$$

where A and B are constants with $A \approx 600$ and $B \approx 273$ as stated in [7].

A more accurate μ is required for a better approximation to the real temperature. This necessitates a small quantization error in the ΔΣ-ADC. To achieve an accuracy in the order of $0.01°C$, the resolution of the ΔΣ-ADC should be as high as 16 bits. This results in an excessive conversion time (2^{16} cycles for a first-order implementation), jeopardizing the temperature sensor energy efficiency. Conventionally, this can be solved by a high-order modulator with a large integrator bandwidth, with the disadvantages of increased circuit complexity and overall power consumption.

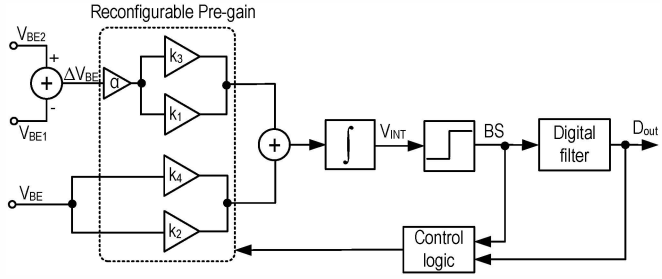

Fig. 3 Simplified block diagram of ΔΣ-ADC with a reconfigurable pre-gain stage and temperature data feedback.

B. Proposed Structure

It can be observed that for a traditional smart CMOS temperature sensor, the input signal full scale is equivalent to approximately $600\,°K$. Notice that the military full range spanning from -55 to $125°C$ only occupies one third of this input range. For many recent emerging applications, e.g. cold chain temperature monitoring, human-body temperature monitoring etc., the targeted temperature range is much narrower than the military range, rendering an inefficient ΔΣ-ADC implementation. This work is aimed to increase the ΔΣ-ADC input range coverage for relaxed resolution requirement by employing a reconfigurable pre-gain stage to optimize the sensing range according to different practical application requirements, as shown in Fig. 3. The proposed structure samples ΔV_{be} and V_{be} with two sets of gain stages to modify their differences based on the ΔΣ-ADC bit-stream output (BS) for better utilization of the sensing range with the full input range of ΔΣ-ADC. The gain ratios including α *and* k_{1-4} are implemented by a capacitor array with DEM technique to minimize the gain error as a result of capacitor mismatch. To solve the problem of the limited application areas as a result of the reduced temperature sensing range, temperature data feedback is utilized to reconfigure the pre-gain stage to achieve multi-range sensing.

The principle of the incremental ΔΣ-ADC is based on charge balancing and is illustrated as:

$$Q_{charging} = C_{int} \cdot (k_1 \cdot \alpha \cdot \Delta V_{BE} - k_2 \cdot V_{BE}) \quad (7)$$

$$Q_{discharging} = C_{int} \cdot (k_3 \cdot \alpha \cdot \Delta V_{BE} - k_4 \cdot V_{BE}) \quad (8)$$

where $Q_{charging}$ and $Q_{discharging}$ are the charges integrated when BS=0 and BS=1, respectively. After totally M cycles and N cycles for BS=1, the following charge balancing equation results:

$$(M - N) \cdot Q_{charging} + N \cdot Q_{discharging} = 0 \quad (9)$$

The ratiometric readout μ' obtained can be expressed as:

$$\mu' = \frac{N}{M} = \frac{k_1 + k_2}{k_1 - k_3} \cdot \frac{\alpha \Delta V_{BE}}{V_{BE2} + \Delta V_{BE}} - \frac{k_2}{k_1 - k_3}$$

$$= G \cdot \frac{\alpha \Delta V_{BE}}{V_{BE2} + \Delta V_{BE}} + C \quad (10)$$

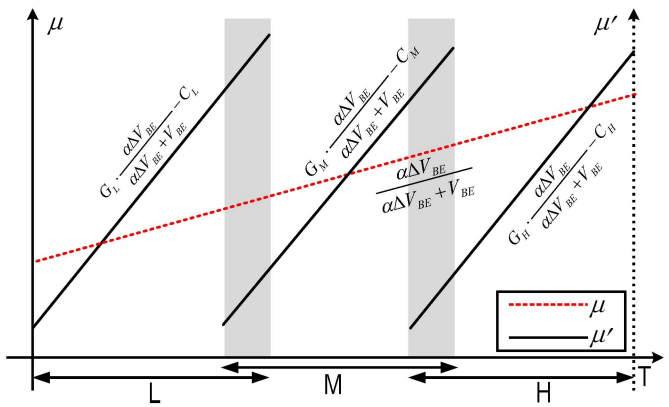

Fig. 4 Comparison of ratiometric output between the conventional (μ) and proposed structure with pre-gain (μ').

where G and C denotes the gain and offset, respectively. When compared with the traditional implementation (4), (10) indicates a more efficient sensing range coverage which can be achieved by adjusting G and C. Furthermore, these two terms are dependent only on k_{1-4}, which can be accurately achieved by DEM. For the same quantization error (e.g. 0.01℃), the resolution requirement can be relaxed by ΔB bits:

$$\Delta B = \log_2\left(\frac{k_1+k_2}{k_1-k_3}\right) \quad (11)$$

This results in a much relaxed ΔΣ-ADC design requirement to achieve high temperature sensing accuracy. A reconfigurable pre-gain stage is designed to achieve wide temperature range overage while preserving low ΔΣ-ADC design complexity and high accuracy. According to (10), this can be readily achieved by using different G and C with several k_{1-4} ratios, as illustrated in Fig. 4. Here, we have implemented a smart temperature sensor for three temperature sub-ranges (L, M and H) to cover an extended -20 to 60°C range, using the k_{1-4} parameters as shown in Table I. A 2 ℃ guard band is implemented between neighboring sub-ranges to ensure the system robustness in case of temperature hysteresis.

III. ΔΣ-ADC WITH PRE-GAIN STAGE

For temperature signal conversions, the pre-gain stage first samples V_{BE} and ΔV_{BE} extracted from the front-end bias circuit. A ΔΣ-ADC is then employed to digitize the combination of V_{BE} and ΔV_{BE} into a bit-stream.

A. Reconfigurable pre-gain stage

As shown in Fig. 3, reconfigurable pre-gains are realized by using different ratios implemented with a number of sampling unit capacitors. Due to the large ratios required for α and k_{1-4}, a significant number of unit capacitors are required which will inevitably increase the chip area as well as the DEM control complexity. To solve this problem, a multi-cycle integration scheme that trades off chip area and design complexity with conversion time is introduced. As a consequence, the required number of sampling unit capacitors can be reduced to 1/N when compared with the conventional integration scheme, where N is equal to the number of integration cycles. In our implementation we set $N = 8$ and the estimated area reduction can be up to almost 50%.

TABLE I GAIN PARAMETER SELECTIONS

Range	L (-20~7 ℃)	M (5~35 ℃)	H (33~60 ℃)
k_1	9	7.5	7
k_2	7	7	8
k_3	8	6.5	6
k_4	8	8	9

B. Capacitor optimization

Since the number of sampling capacitors is largely reduced, the corresponding settling time in the sampling front-end is also relaxed which can help to improve the overall energy efficiency. Assuming an error tolerance of $\varepsilon = 0.1\%$, a settling time of $\tau\, ln(1/\varepsilon)$ is required, where τ is the corresponding time constant. This sets the upper limit of C_s for a half clock period sampling time. Due to the use of multi-cycle integration, a smaller C_s is obtained which can lead to increased thermal noise. This, however, can be compensated by the relaxed ΔΣ-ADC resolution requirement. In our design, we set the value of C_s in order the thermal noise is smaller than the quantization noise to achieve the required resolution.

C. Variable sampling frequency in different sub-ranges

Since I_{bias} is temperature dependent, the front-end circuit settling time also varies with temperature. This can be compensated by providing a larger I_{bias} in the sub-range L and a smaller one in the sub-range H, with the disadvantage of increased control complexity. In our implementation, we ensure accurate settling in all the three temperature sub-ranges by using a temperature dependent clock to sample the PTAT and CTAT voltages [8]. The selected f_{clk} for sub-ranges L, M and H are 20kHz, 25kHz and 28kHz, respectively.

IV. SIMULATION RESULTS

This work is implemented in a standard 0.18μm CMOS process. The input range of the ΔΣ-ADC has been optimized in all the sub-ranges with temperature data feedback to switch between the sub-ranges in case of temperature hysteresis. The corresponding simulation results are shown in Fig. 5. It can be observed that an accuracy of ±0.1°C for the entire temperature range can be achieved using only one-point calibration. Fig. 6 shows the simulated results using individual calibration in each sub-range, and the corresponding residue error can be further reduced to ±0.05°C. Simulation results show that a maximum energy saving of ~20% per conversion can be achieved in sub-range H by using the variable sampling frequency scheme. Fig. 7 shows the power breakdown at nominal operating condition in sub-range M (i.e. 27°C). It can be seen that almost half of the total power is consumed by the ΔΣ-ADC. Table II shows the

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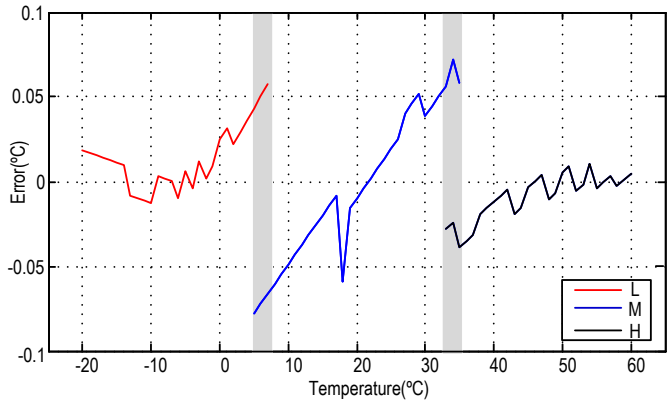

Fig. 5 Simulated sensing accuracy for the three sub-ranges with one point calibration.

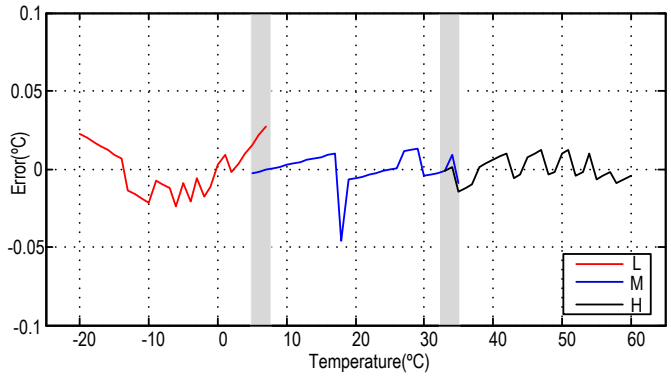

Fig. 6 Simulated sensing accuracy for the three sub-ranges with individual calibration.

performance comparisons with the previous works. The proposed temperature sensor has a more flexible temperature sensing range while keeping a high accuracy with low power consumption and one point calibration.

V. CONCLUSIONS

This paper presents a multi-range ultra-lower power, high accuracy CMOS smart temperature sensor based on substrate BJT and a first-order incremental ΔΣ-ADC with pre-gains. This sensor can be used in modern expanded areas with the sensing range defined by multiple sub-ranges, high accuracy and low power consumption.

An inaccuracy of below $\pm 0.1°C$ has been achieved after one-point calibration for wide sensing range applications and $\pm 0.05°C$ with individual calibration for targeted short sensing range applications while the power-consumption is only $1\mu W$.

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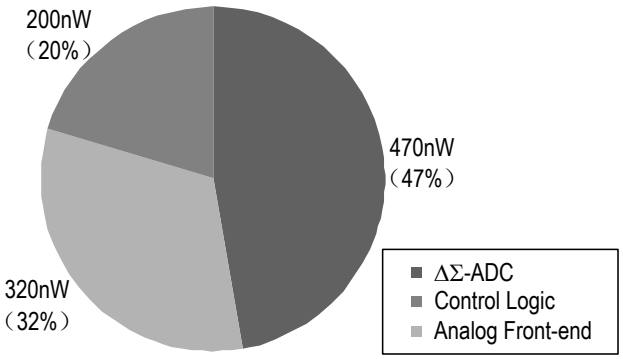

Fig. 7 Power breakdown of this proposed sensor at $27°C$.

TABLE II PERFORMANCE COMPARISONS

	This work#			[1]^	[4]^	[5]#
Process	0.18μm			0.16μm	0.35μm	0.18μm
Temperature Range (°C)	-20~60			-55~125	35~45	35~45 (27~47)
	-20~7	5~35	33~60			
Power(μW)	~1			5.1	0.11	1.1
Inaccuracy (°C)	±0.1			±0.15	±0.1	±0.04 (±0.1)
	±0.03	±0.05	±0.02			
Sampling Rate (Sa/s)	~0.7			188	10	2
Calibration point	1			1	2	1

Simulation Results
^ Measurement Results

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