A Review and Design of the On-Chip Rectifiers for RF Energy Harvesting

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***Abstract*—This paper presents an overview of the CMOS on-chip rectifiers for RF energy harvesting in the RFID, internet of things, or wearable device applications. The pros and cons of different RF to DC rectifier topologies are investigated, compared, and summarized. All the topologies are designed and optimized in a 65nm CMOS process, with the input power range from –10dBm to 4dBm and the load resistor range from 10kΩ to 1MΩ. The simulated results show that the cross-connected (CC) topology exhibits the highest achievable power conversion efficiency up to 65% (rectifier only), while the CC topology with the threshold voltage cancellation technique and the MOS diode topology achieve 46.7% and 51%, respectively.**

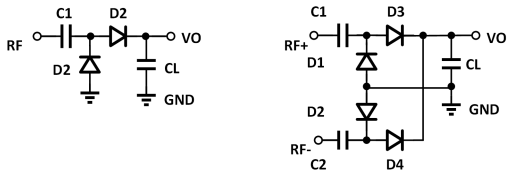
Keywords—RF energy harvesting, CMOS rectifier, wireless power, power converter, RF-DC, ultra-high frequency (UHF)

I. INTRODUCTION

There is a growing demand in harvesting the energy from the ambient to supply the wearable electronic devices, internet of things (IoT), wireless sensor networks (WSN), RF identification (RFID), and the biomedical implantable devices. RF energy harvesting is one of the most popular power extraction methods, as the density of wireless communication devices increases rapidly, especially in the metropolises. Most of the communication systems are designed to operate in the ultra-high-frequency (UHF) ISM bands (300MHz to 3GHz). Thus, there is much RF energy readily available in the environment at the UHF. Moreover, using the UHF for wireless power transfer could lead to a low cost and/or small size solution.

In the past decade, many works on the rectifiers for UHF-band RF energy harvesting have been published. Defined by their symmetry property, the rectifiers could be categorized into two groups: single-ended topology [1]-[14], and differential topology [15]-[20]. And, for their conduction characteristic, the rectifiers can work as either half-wave or full-wave rectifier, even for the single-ended rectifiers like the voltage doubler and voltage multiplier [1], [21]. Fig. 1 shows the structure of a typical single-ended rectifier and a differential rectifier. This paper reviews different multi-stage rectifier topologies, and how were the diodes in these rectifiers realized in CMOS process.

This paper is organized as follows. Section II gives an overview of the prior arts. Section III shows the rectifier simulation results with different topologies in a 65nm CMOS process. Finally, a brief conclusion is drawn in Section IV.



(a) Single-ended (b) Differential

Fig. 1. Schematics of the (a) single-ended and (b) differential rectifiers.

II. PRIOR ART OVERVIEW

For the RF energy harvesting application, the voltage multiplier, which is similar to the Dickson charge pump [2], was used in [3] as a rectifier for the RF to DC conversion at UHF in 2003. In that rectifier circuit, Schottky diodes with low turn-on voltage (around 200mV) and high saturation current were employed. Hence, the rectifier efficiency was increased significantly. However, the high fabrication cost (due to extra masks) associated with Schottky diodes, makes it not suitable for the low-cost solutions [4]. And the off-chip Schottky diodes would increase the PCB area and are not suitable for the miniature sized devices [15]. Instead of using the expensive or discrete Schottky diodes, CMOS compatible MOSFET diodes with zero threshold voltage V_{TH}, were employed in [5], [6]. However, using the low V_{TH} transistors resulted in a worse performance, because the transconductance of the MOS transistors in subthreshold region is less than that of a diode.

In depth analysis and design strategy for rectifier with zero V_{TH} MOS diodes were presented in [7]. Note that, intuitively, for the same amount of converted power, people would think that higher efficiency could be achieved with less conversion stages, but it was shown that for a multi-stage rectifier with specified output power, the maximum achievable efficiency can be maintained even though the number of stage increases. In other words, the efficiency would not obviously decrease with the increase of the stage number, which is an interesting feature. Fig. 2 shows a three-stage rectifier with MOS diode.

To increase the received power and to extend the communication distance of the RFID tag, several V_{TH} compensation techniques have been proposed [1], [8]. A V_{TH}

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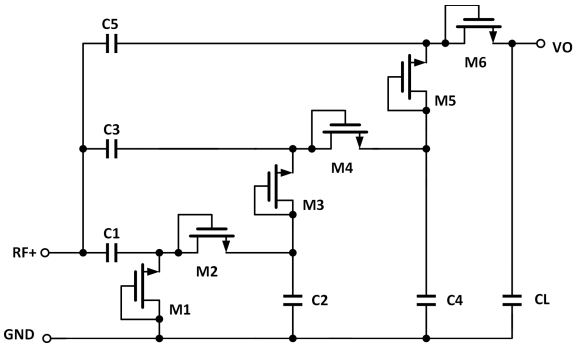

Fig. 2. A three-stage rectifier with MOS diode.

compensation for MOS diodes, which is to further reduce the forward diode voltage drop with an external voltage compensators was employed in [8] with a secondary battery. In order to get rid of the extra battery, an internal V_{TH} cancellation circuit (IVC) was proposed in [1], as shown in Fig. 3, where a capacitor stored the threshold voltage that was applied between the gate-source terminals of the MOS transistor. However, this technique needs to use large capacitors and resistors which would occupy large silicon area, especially in the multi-stage implementation.

Similar to the IVC technique, floating-gate techniques were adopted to reduce the threshold voltage of MOS transistor, which required an additional pre-charge phase to store a pre-charged compensation voltage, making the system unattractive for fully battery-less applications [9]. Moreover, a dynamic threshold MOSFET was accomplished by just tying the transistor gate and the substrate together in deep n-well process, which had a lower leakage current when reverse biased and a higher forward current when the transistor was turned on [10].

As shown in Fig. 4, an inter-stage V_{TH} compensation scheme was introduced in [11], [12]. The compensation was achieved by connecting the gate terminal to the post-stages which eliminated the large additional capacitors and resistors in the IVC topology, and gives similar performances with the IVC topology. In [13], NMOS transistors within deep n-well were used to provide individual bulk biasing and to reduce the variation of threshold voltage between different rectifier stages.

In order to further increase the sensitivity of the rectifier, it was found that, the output voltage with the transistors operating in subthreshold region was different from that of operating in saturation region [14]. It was shown that transistor size and V_{TH} have no effect on V_{OUT} and −32dBm which is the highest sensitivity was achieved with 50 stages in [14].

Different from the above mentioned topologies, a self-driven synchronous rectifier or so-called cross-connected differential rectifier was proposed in [16]. Fig. 5 shows a 3-stage cross-connected differential rectifier. In this topology, the MOS transistors are acting now as switches for rectification, and would exhibit lower on-resistance. Through such an active operation scheme, the forward voltage drop can be minimized, however, the reverse leakage current would increase at high input amplitudes [17]. Due to this self-driven scheme, the rectifier could operate at a lower input power level than other

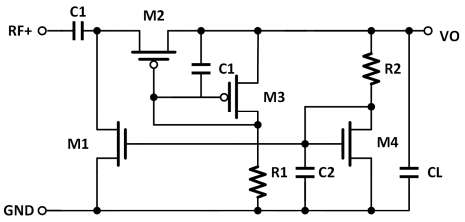

Fig. 3. A one-stage rectifier with the IVC technique.

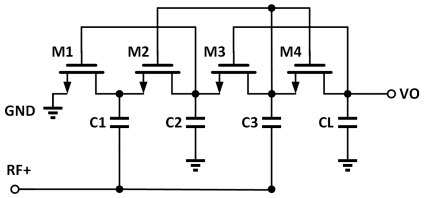

Fig. 4. A Two-stage inter-stage V_{TH} compensation rectifier.

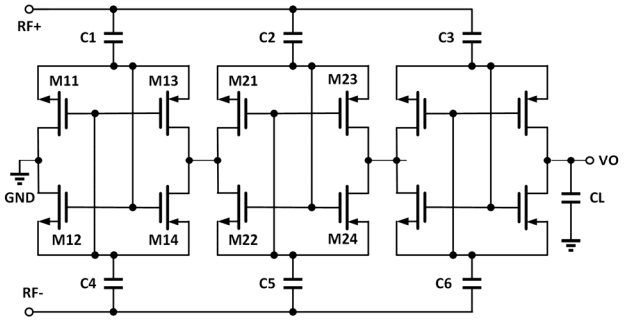

Fig. 5. A three-stage cross-connected differential rectifier.

topologies [18]. It was shown that the voltage conversion ratio (VCR) could be larger than 80% when the rectifier input amplitude was higher than 150mV in [19]. In [20], the cross-connected structure was combined with the IVC technique as shown in Fig. 6, and high efficiencies was achieved at 13 MHz by simulation with relatively high input amplitudes.

III. SIMUATION OF DIFFERENT TOPOLOGIES

To demonstrate more useful details on the CMOS process based rectifiers for the RF-DC conversion, the above mentioned topologies have been simulated with a 65nm CMOS process, and then the data was analyzed, compared, and summarized for the conclusion. For simplicity and fair comparison, perfect impedance matching is assumed here.

The PCE of an RF to DC converter is defined as

$$\mathrm{PCE} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \frac{V_{\mathrm{DD}}^2 / R_{\mathrm{L}}}{\frac{1}{N \cdot T}\int_{t_0}^{t_0+N\cdot T} V_{\mathrm{RF}}(t)\cdot I_{\mathrm{RF}}(t)\,\mathrm{d}t} \tag{1}$$

where T is the period of the input sinusoidal wave, and N is the number of cycles that are integrated for P_{IN} calculation. The VCR of an RF to DC converter is defined as

$$\mathrm{VCR} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN,\,Peak}}} \tag{2}$$

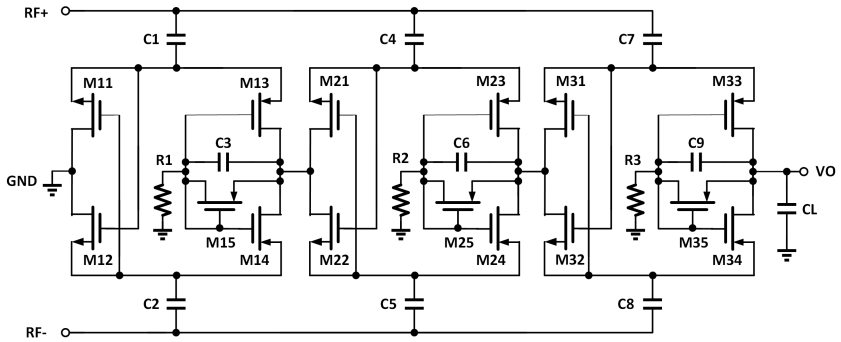

Fig. 6. A three-stage Rectifier using cross-connected NMOS switches in combination with two PMOS diodes with IVC.

where $V_{IN,\,Peak}$ is the input amplitude of the rectifier sinusoidal wave, and V_{OUT} is the output voltage of the rectifier.

In this part, the three rectifier configurations shown in Fig. 2, Fig. 5, and Fig. 6 are designed, simulated and compared. The simulation setup is shown in Fig. 7. The circuit consists of resistive and capacitive loading and an antenna. Instead of using the voltage source, a power source with 50Ω output impedance is used to perform the simulation at 900MHz. The rectifier configurations are implemented in a CMOS 65nm technology. For a fair comparison, each structure is built with three stages. The designed parameters for the rectifiers are listed in Table I.

Fig. 8(a) shows the PCE of the rectifiers under different input power levels with the same load resistor R_L of 100kΩ. It is shown that the highest PCE could be achieved with the CC structure, of which the PCE can only be maintained for a quite short range of input power and then decreases rapidly. For the other topologies, the PCE curves are flatter. Fig. 8(b) shows the VCR of the rectifiers under different input power with an R_L of 100kΩ. It is shown that the highest VCR could be achieved by the MOS diode structure. Comparing Fig. 8(a) and Fig. 8(b), the peak PCE and the peak VCR are not achieved by the same topology. It is a trade-off between PCE and VCR with a specified application under consideration. Fig. 8(c) and 8(d) shows the PCE and VCR of the rectifiers, respectively, under different loading at the input power of −6dBm. High overall PCEs are still obtained by the CC structure. On the other hand, the highest VCR is obtained with MOS diode structure. And, the CC with IVC technique does not give comparable performances at 900MHz. In addition, it is found that the peak PCE of a CC rectifier can be maintained for different specific input power levels with the optimized parameters, as demonstrated in Fig. 9. The widths of the PMOS transistors are 2.5 times larger than that of the NMOS transistors which are 3µm, 1.15µm, 0.66µm, 0.26µm for those four simulations. Larger sizes are used for lower input power level.

IV. Conclusion

A comparison for different RF-DC rectifiers operating in the UHF-band for RF energy harvesting has been performed. Three different RF-DC rectifiers have been simulated in 65 nm CMOS process. PCEs and VCRs have been listed for performances comparison. The simulation results show that the cross-connected topology exhibit the highest achievable power

TABLE I. Designed Parameters for the Rectifiers

	CC	CC + IVC	MOS Diode
NMOS W/L	3µm/0.06µm	5µm/0.06µm	40µm/0.06µm
PMOS W/L	7.5µm/0.06µm	15µm/0.06µm	N/A

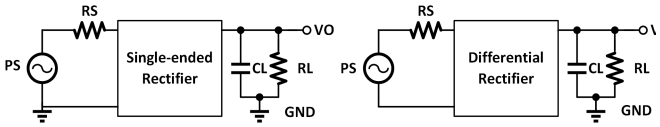

Fig. 7. Simulation circuit of the RF energy harvesting.

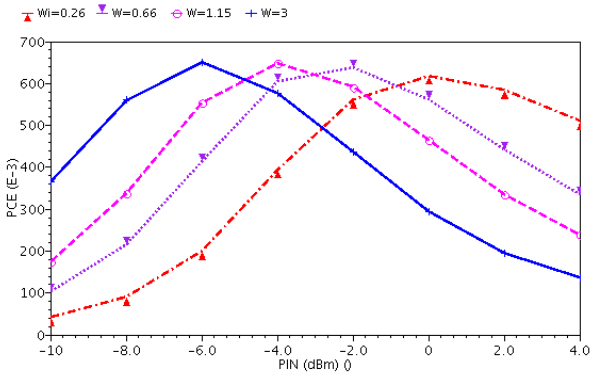

Fig. 9. Simulated PCE versus P_{IN} of the CC rectifier with different sizes

conversion efficiency up to 65% (rectifier only) which can be maintained over a wide input range by adjusting the transistor size, while the other topologies only achieve 46.7% and 51%, respectively.

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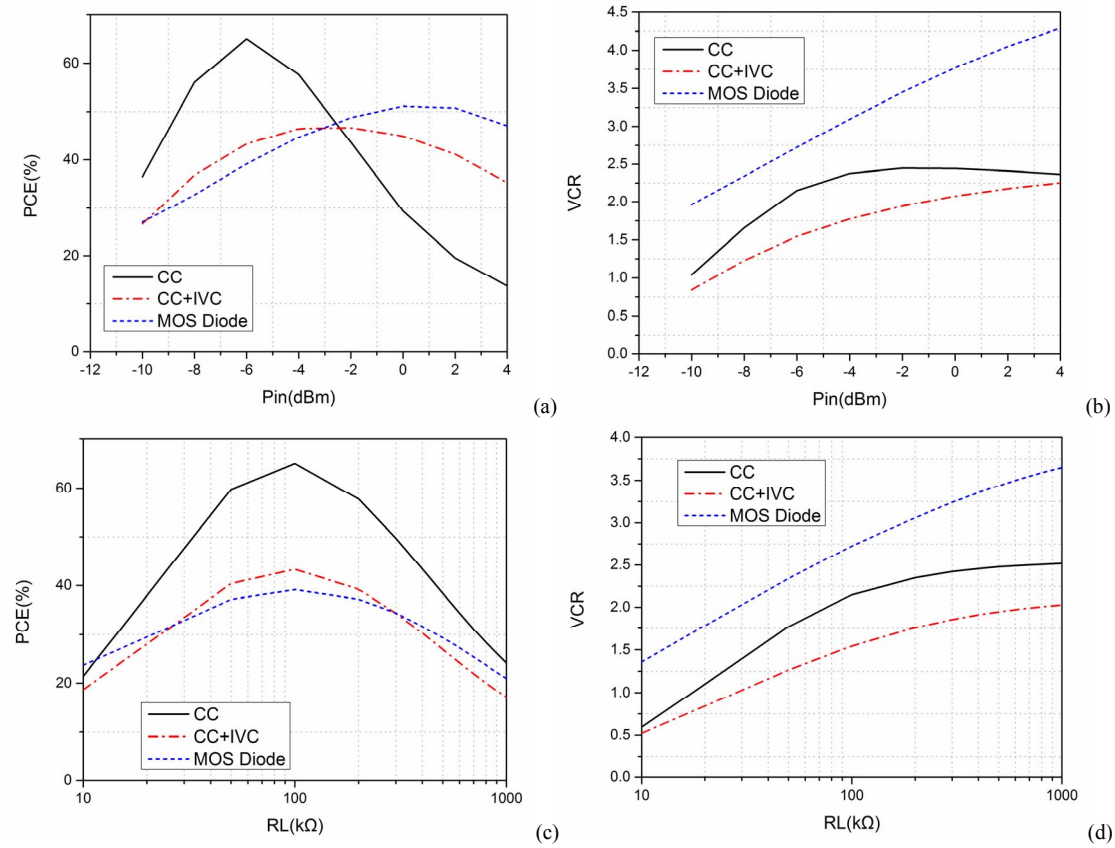

Fig. 8. Simulated (a) PCE and (b) VCR versus P_{IN} of the rectifiers; and (c) PCE and (d) VCR versus R_{LOAD} of the rectifiers

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