2.4 A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF

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RF-tunable blocker-tolerant receivers (RXs) enhance the flexibility of multiband multistandard radios at low cost (Fig. 2.4.1). The mixer-first RX [1] delays the signal amplification to baseband (BB) by frequency-translating the BB lowpass response to RF as bandpass. This raises the out-of-band (OB) IIP3 (27dBm) at the expense of NF (5.5dB) and power (60mW) due to no RF gain. The noise-cancellation RX [2] breaks such a tradeoff by paralleling a voltage-sensing RX with the mixer-first RX. This achieves a better pair of NF (1.9dB) and OB-IIP3 (13.5dBm), but sacrifices more die size (1.2mm²) and power (<78mW) to accommodate the doubled RF and BB circuits. In [3], N-path RF filtering and noise cancellation are concurrently attained in one current-reuse RX. That approach saves die area (0.55mm²) and power (16.2mW) at a high OB-IIP3 (17.4dBm), but requires a high V_{DD} (2.5V) to widen the voltage headroom. Also, seeing that its NF (4.6dB) is handicapped by the input-impedance matching requirement (S_{11}<−10dB), there is no flexibility to get better NF. Finally, as both [2] and [3] involve two mixing steps, the LO power is penalized.

This work aims at a single-mixing blocker-tolerant RX by proposing a *gain-boosted-mixer-first* topology. Two unexplored features: *indirect BB amplification* and *double-RF N-path filtering* improve the NF (1.5 to 2.9dB) and OB-IIP3 (13dBm) over a wide range of RF (0.1 to 1.5GHz), while squeezing the power (11mW) and area (0.028mm²) with zero external components. The RX also originates *partial-inductive input impedance* to self-cancel the frequency shift of S_{11} BW, which is a typical inadequacy of mixer-first RX circuits demanding input-impedance tuning [1].

For blocker rejection a wideband RX can benefit from on-chip LO-defined N-path filters to narrow down the RF BW. The function-reuse RX in [4] embedded a *gain-boosted N-path switched-capacitor filter* to improve the NF and OB-IIP3 with small capacitors. However, the RF BW is coupled with the input-impedance matching (S_{11}<−10dB), bottlenecking the close-in-blocker tolerability. The proposed RX (Fig. 2.4.2a) benefits from two frequency-translational paths to circumvent that constraint. Specifically, when the RF input (V_i) is downconverted to BB ($V_{B1,I\pm}$ and $V_{B1,Q\pm}$) by the 4-path passive mixer M_p, the BB impedance $Z_{i,BB}$ is frequency-translated to V_i as bandpass $Z_{i,RF}$ for input-impedance matching and N-path filtering (Fig. 2.4.2b). A voltage-sensing amplifier G_m is added to drive the bottom plate of 4 BB capacitors C_1. As V_i and V_o are out-of-phase, the effective capacitance of C_1 can be enlarged by a high gain-boosted factor for steeper RF filtering at V_o (i.e., $Z_{o,RF}$), while not affecting the input-impedance matching. Besides, the introduction of C_1 adds two distinct features: 1) the amplified RF signal at V_o is downconverted to BB via C_1 [4], allowing more BB voltage gain at $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ than the typical mixer-first RX, and 2) the BB impedance $Z_{i,BB}$ is also frequency-translated to V_o contributing to its high-Q filtering. For the former, it brings down the input-referred noise of R_1 and relaxes the power budget of the 4 BB amplifiers (G_{mB}). The latter benefits the blocker tolerability of G_m. Additionally, the presence of R_1 permits G_m to deliver a higher voltage gain to $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ without penalizing the linearity. Both G_m and G_{mB} are realized as inverter-based amplifiers to maximize their transconductance-to-current efficiency.

For a typical mixer-first RX, the input impedance incurs an imaginary (capacitive) part shifting the S_{11} BW away from the LO frequency (~5MHz in simulation, Fig. 2.4.3a). Solved here, the BB impedance $Z_{i,BB}$ is upconverted with a phase shift of $-\theta$ at V_i [i.e., $|Z_1|e^{-j\theta}$] and V_o [i.e., $|Z_2|e^{-j\theta}$]. As G_m offers phase-inverting, the phase shift $-\theta$ at V_o becomes θ when referring back to V_i, resulting in an inductive part (Fig. 2.4.3b) that can partially cancel the capacitive part from $|Z_1|e^{-j\theta}$. Thus, the simulated S_{11} is re-centered back to f_{LO} with only 1MHz frequency shift.

The −3dB BW at V_i is mainly defined by $Z_{i,BB}$. Since $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ are differential, V_o is a virtual ground for the BB signals, and the voltages at $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ are upconverted and in-phase summed at V_o. Thus, the −3dB BW at V_o is also approximately defined by $Z_{i,BB}$. Overall, single-mixing and one set of BB capacitors C_2 are adequate to acquire double-RF N-path filtering with a narrow RF BW (2.6MHz). In this design, R_1=128Ω, and a large R_2 (21kΩ) reduces C_2 (7pF). Thanks to the capacitor multiplication effect of C_1 by G_m, C_1 is small (4.6pF) while keeping a narrow RF BW at both V_i and V_o (Fig. 2.4.3c). This also avoids any large parasitic capacitance at V_o. Since the input-impedance matching no longer relies on R_F and G_m, they are free to be enlarged to enhance the RF gain and NF. From simulations, when the transconductance ($g_{m,Gm}$) of G_m is upscaled from 50 to 200mS, the input-impedance matching is preserved, while the NF improves from 2.4 to 1.7dB, and OB-IIP3 improves from 7.3 to 9.5dBm.

The NF of this single-mixing RX can be compared with the theoretical minimum NF of [2,3] that involves double-mixing and/or two RX paths [2]. As plotted in Fig. 2.4.3d, under perfect noise cancellation, their NFs [2,3] are dominated by the thermal noise of G_m (equation in Fig. 2.4.3d). Comparing with [2,3], here the simulated BB NF at $V_{B1,I\pm}$ (the same for Q-channel $V_{B1,Q\pm}$) can even be smaller when $g_{m,Gm}$<70mS, while the NF at $V_{B2,I\pm}$ is only 0.2dB higher than such a theoretical value. This is intuitively plausible as the BB gain and noise responses at $V_{B2,I\pm}$ are built up *concurrently* with those at V_o. For $g_{m,Gm}$=200mS, the NF at $V_{B1,I\pm}$ and $V_{B2,I\pm}$ are roughly 0.3 and 0.5dB higher than the theoretical value, respectively. This extra noise comes from M_p, R_1 and G_{mB}, as their noise contributions have been neglected in the NF equation.

The RX fabricated in 65nm CMOS occupies a die size of 0.028mm², in which C_1 is a MIM capacitor (5fF/μm²) to minimize the parasitic effect. Both G_m and G_{mB} aim at 0.7V operation to save the static power, whereas the LO generator operates better at 1.2V (results at 0.7V were also tested, as summarized in Fig. 2.4.7). The measured S_{11} is <−16dB over a 0.1-to-1.5GHz RF range (Fig. 2.4.4). By selecting $g_{m,Gm}$=200mS and R_F=7kΩ, the NF measures down to 1.5dB at 0.2GHz, and up to 2.9dB at 1.5GHz, limited by the RF BW. The 1/f noise corner is ~150kHz. Thanks to the double-RF N-path filtering with narrow −3dB BW, the OB-IIP3 rapidly reaches 10dBm at 30MHz offset. The RF-to-IF gain is 38dB, and drops by 1dB with a −6dBm blocker power (Fig. 2.4.5) at 80MHz offset, consistent with the 5.8dB BB gain measured at that frequency offset. With a 0dBm blocker, the 10dB gain compression is due to the saturation of the BB amplifiers. The −3dB BW measured at BB is ~2MHz. The OB P_{1dB} is up to -6dBm limited by the filtering (~6dB) at $V_{B1,I\pm}$ and $V_{B1,Q\pm}$. In fact, if more die area is allowed, C_3=10pF can be added at $V_{B1,I\pm}$ and $V_{B1,Q\pm}$ (Fig. 2.4.2) to limit their voltage gain <0dB at 80MHz offset for a better P_{1dB} (−2dBm, simulated). With a single-tone blocker injected at 80MHz offset, the 0dBm-blocker NF is 13.5dB.

Benchmarking with the recent art (Fig. 2.4.6), this work succeeds in squeezing the power and area without penalizing the NF and OB-IIP3. Comparing with [3], this work saves 47% of power and shows 2dB better NF and 20x less area. The NF is also ~5dB better than [5], which reported the smallest area before this work. The proposed RX is also measured at single-0.7V supply and can compete further with the high-performance version of [4], which was also fabricated (Fig. 2.4.7) and tested for merit comparison.

References:
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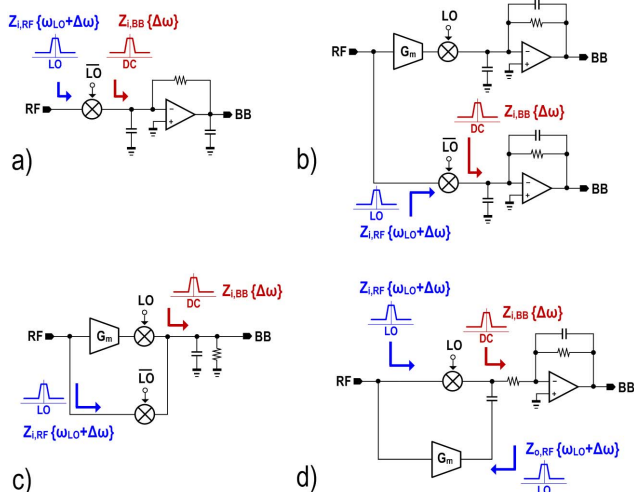
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Figure 2.4.1: a) Mixer-first RX [1]; b) Dual-mixer dual-BB noise-canceling RX [2]; c) Dual-mixer single-BB noise-canceling RX [3]; d) Proposed gain-boosted mixer-first RX.
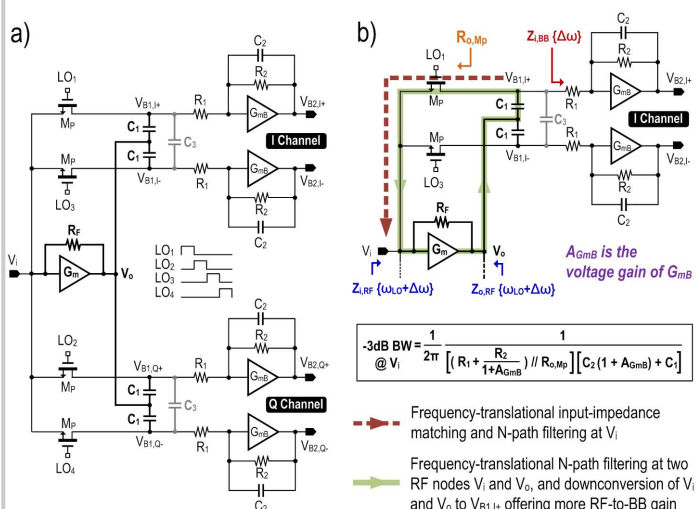

Figure 2.4.2: a) Schematic of the proposed RX and b) there are two frequency-translational paths marked at I channel.
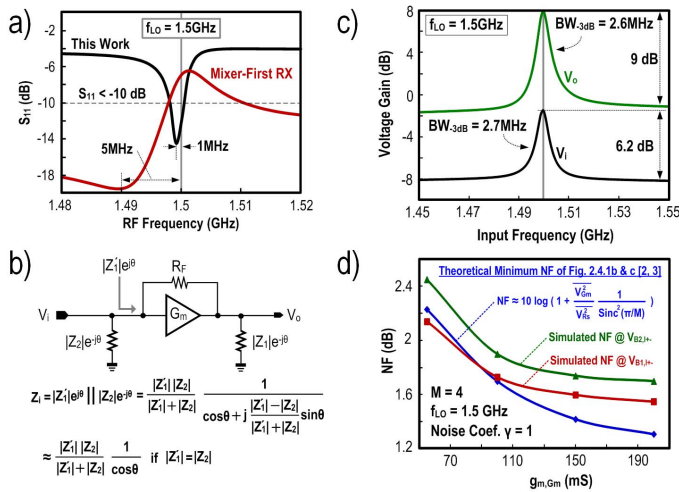

Figure 2.4.3: Simulated a) S_{11} of a typical mixer-first RX and this work; b) the inductive effect created by Gm improves S_{11}; c) gain responses at Vi and Vo; d) NF versus $g_{m,Gm}$ at $V_{B1,I\pm}$ and $V_{B2,I\pm}$.
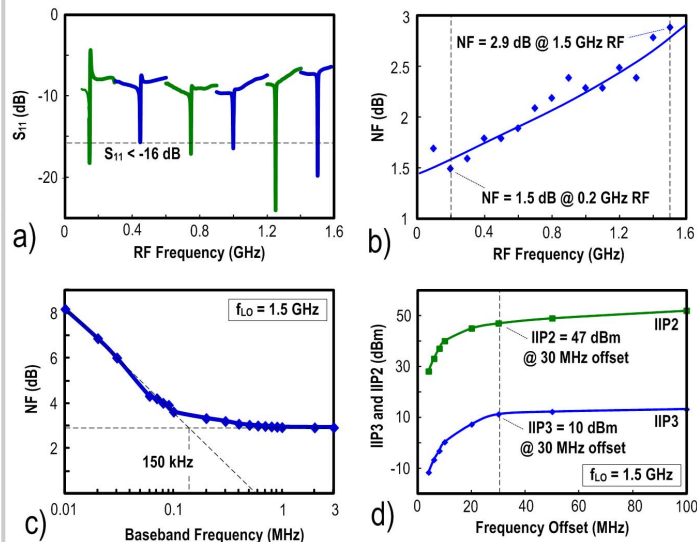

Figure 2.4.4: Measured a) S_{11}; b) NF; c) 1/f noise corner; d) IIP2 and IIP3.
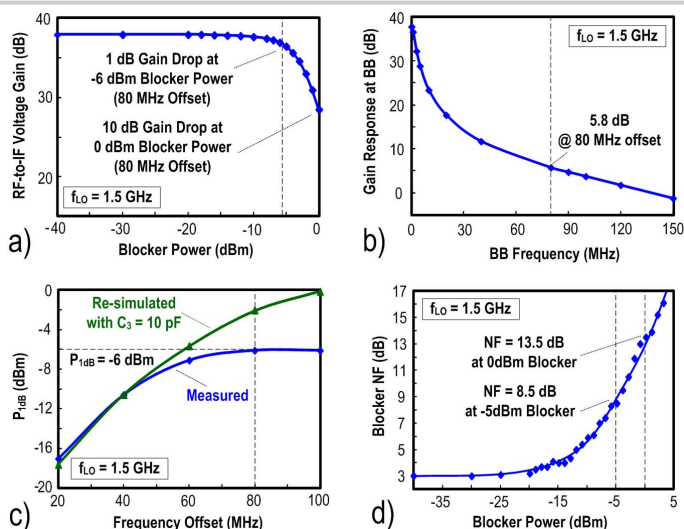

Figure 2.4.5: Measured a) voltage gain versus blocker power; b) BB gain; c) P_{1dB}; d) blocker NF.

	This Work	F. Lin [3] [ISSCC'14]	S. Youssef [5] [ISSCC'12]	B. van Liempd [JSSC'Aug 14]	A. Mirzaei [JSSC'Apr 14]	I. Fabiano [ISSCC'13]
RX Architecture	Gain-Boosted-Mixer-First + Double-RF N-Path Filtering	Current-Reuse + Active/ Passive N-Path Mixers	Active Feedback + 50Ω Matching	RF LNA + Passive Mixer + G_m-C + OpAmp	LC Matching + Passive Mixer + Op-Amp RC	Transformer + Passive-Mixer + OpApmp RC
RF Input Style	Single-Ended	Single-Ended	Differential	Differential	Single-Ended	Single-Ended
External Parts	Zero	Zero	Transformer	Transformer	LC	Zero
RF Range (GHz)	0.1 to 1.5	0.15 to 0.85	1 to 2.5	0.4 to 3	2	1.8 to 2.4
Supply (V)	0.7, 1.2	1.2, 2.5	1.2	0.9	1.2, 1.5	1.2, 1.8
Die Size (mm²)	0.028	0.55	0.06	~0.6	0.93 (w/VCO)	0.84
Power (mW) @ RF	11 @ 1.5 GHz	16.2 @ 0.85 GHz	62 @ 2.5 GHz	20 @ 0.4 GHz 40 @ 3 GHz	38 @ 2 GHz (w/VCO)	35 @ 2 GHz
DSB NF (dB)	1.5 to 2.9	3.7 to 5.5	7.25 to 8.9	2.2 to 3.1	1.7	3.8
0-dBm Blocker NF (dB)	13.5 @ 80 MHz	N/A	N/A	14 @ 80 MHz	13.5 @100 MHz	7.9 @ 20 MHz
P_{1dB} (dBm) @ Freq. Offset	-6 @ 80 MHz	-2.5 @ 50 MHz	-3 @120 MHz	-12.5 @ 80 MHz	N/A	-2 @20MHz
OB-IIP3 (dBm)	+13	+17.4	+12	+3	-2.5	+18
OB-IIP2 (dBm)	+50	+61	N/A	+80 (calibrated)	+50	+64
BB BW (MHz)	2	9	5	0.5 to 50	N/A	N/A
BB Filtering	1 Real Pole	2 Complex Poles + 2 Zeros	1 Real Pole	1 Real Pole + 1 Biquad	1 Real Pole	1 Biquad
Volt. Gain (dB)	38	51±1	30	70	50	45.5
CMOS Tech.	65 nm	65 nm	65 nm	28 nm	40 nm	40 nm

Figure 2.4.6: Chip summary and benchmark with the state-of-the-art.

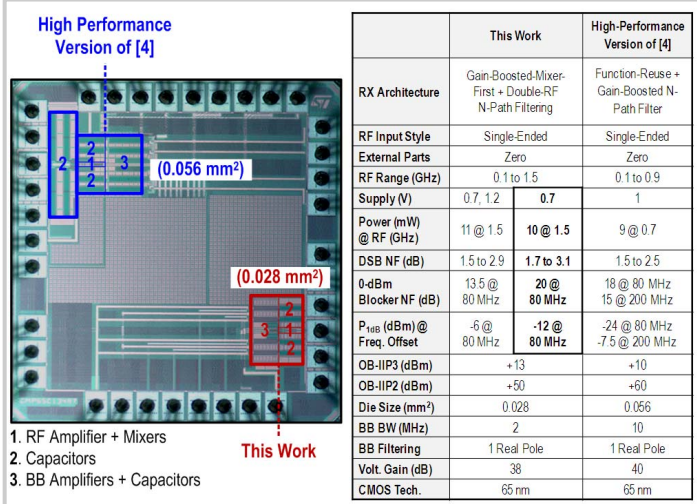|	This Work		High-Performance Version of [4]
RX Architecture	Gain-Boosted-Mixer-First + Double-RF N-Path Filtering		Function-Reuse + Gain-Boosted N-Path Filter
RF Input Style	Single-Ended		Single-Ended
External Parts	Zero		Zero
RF Range (GHz)	0.1 to 1.5		0.1 to 0.9
Supply (V)	0.7, 1.2	0.7	1
Power (mW) @ RF (GHz)	11 @ 1.5	10 @ 1.5	9 @ 0.7
DSB NF (dB)	1.5 to 2.9	1.7 to 3.1	1.5 to 2.5
0-dBm Blocker NF (dB)	13.5 @ 80 MHz	20 @ 80 MHz	18 @ 80 MHz 15 @ 200 MHz
P_{1dB} (dBm) @ Freq. Offset	-6 @ 80 MHz	-12 @ 80 MHz	-24 @ 80 MHz -7.5 @ 200 MHz
OB-IIP3 (dBm)	+13		+10
OB-IIP2 (dBm)	+50		+60
Die Size (mm^2)	0.028		0.056
BB BW (MHz)	2		10
BB Filtering	1 Real Pole		1 Real Pole
Volt. Gain (dB)	38		40
CMOS Tech.	65 nm		65 nm

Figure 2.4.7: Die micrograph of this work and the high-performance version of [4] re-designed for merit comparison. This work was also tested at a single 0.7V supply.