A 104µW EMI-Resisting Bandgap Voltage Reference Achieving –20dB PSRR, and 5% DC Shift under a 4dBm EMI Level

Shiheng Yang, Pui-In Mak and Rui P. Martins [1]

The State Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology (ECE), University of Macau, Macao, China
1 – On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal
(E-mail Correspondence: pimak@umac.mo)

Abstract

This paper describes an electromagnetic interference (EMI)-resisting Bandgap voltage reference. Its basic topology is a Kuijk Bandgap with a PMOS pass device and an active load, improved to generate a low voltage output (441.3mV) via substituting BJT by MOSFET while preserving a low temperature coefficient (TC). A double differential pair and a power-supply independent bias jointly enhance the EMI resisting ability. Simulated in 65nm CMOS, the achieved PSRR is –20dB, TC is 10.65 ppm/°C and DC shift is 5% up to a 4dBm EMI level. The total power consumption is 104µW.

I. INTRODUCTION

The omnipresence of wireless communication systems, new and various electronic appliances, and the utilization of ever increasing frequencies, contribute to a noisy electro-magnetic environment which acts detrimentally on sensitive electronic equipment [1]. When circuits and systems are densely integrated into a system-on-a-chip or a printed circuit board with shared power supply and ground lines, the unavoidable electromagnetic coupling between them becomes a critical design parameter that can no longer be safely excluded from a product design flow. Developing EMI-resisting integrated circuits becomes a critical topic for electromagnetic compatibility in recent years. Unfortunately, most voltage regulators are highly susceptible to EMI such as the Bandgap reference circuits.

Bandgap voltage references (BGRs) are aimed to generate a temperature- and supply-insensitive output voltage for other building blocks such as the voltage-controlled oscillators. Traditionally, most of the BGR studies have been focused on the small-signal performances for achieving lower temperature coefficient (TC), higher power supply rejection ratio (PSRR) and lower power consumption. Contrarily, electromagnetic interference (EMI) injection [2] may destroy the performance of the BGR itself, as its voltage disturbance can be orders of magnitude higher than that induced by temperature variation. The Kuijk BGR topology with improved immunity to EMI was introduced in [3] and illustrated in Fig. 1. It employs a PMOS pass device (M_5), and an AC-grounded compensation capacitor (C_{d1}) for the operational transconductance amplifier (OTA) to stabilize the gate-source voltage of the former, thereby cancelling the impact of low-frequency EMI on the drain current. Yet, this topology is still susceptible to high-frequency EMI because of the nonlinear output resistances of the input differential pair (M_1-M_2). The use of an active load with a positive feedback loop (M_3-M_7) can help shielding M_1-M_2 from EMI injection, while securing a constant average drain current [1].

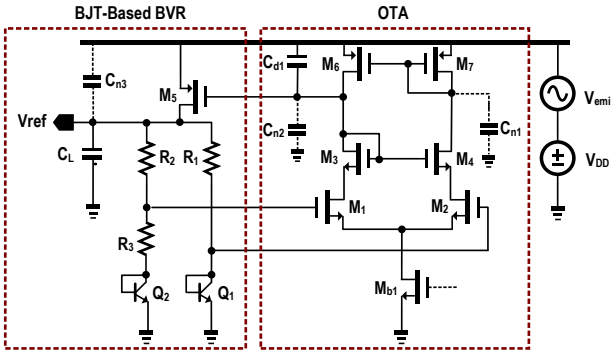


Fig. 1. Conventional EMI-resisting Kuijk BGR based on a PMOS pass device and an active load.

This paper describes the design of a 65nm CMOS EMI-resisting BGR that achieves –20dB PSRR and <5% DC shift under a 4dBm EMI level. It is improved from the classical Kuijk BGR with a PMOS pass device and an active load, while featuring: 1) a power-supply independent bias to lower the EMI susceptibility while saving power; 2) a double differential pair to suppress the DC shift, and 3) the replacement of BJT by MOSFET to reduce the output reference voltage while ensuring a low TC.

II. PROPOSED EMI-RESISTING BGR

The proposed EMI-resisting BGR is depicted in Fig. 2. Its basic topology follows the Kuijk, i.e., a PMOS pass device with a positive feedback active load made by two current mirrors (M_3-M_7) for masking the input differential pair (M_1-M_2) to EMI. The tail current of the OTA is stably biased by a power-supply independent bias circuit for further EMI robustness and to save power. An AC-coupled differential pair (M_8-M_9) cross connected with M_1-M_2 impose the reduction of the DC shift at their shared drain

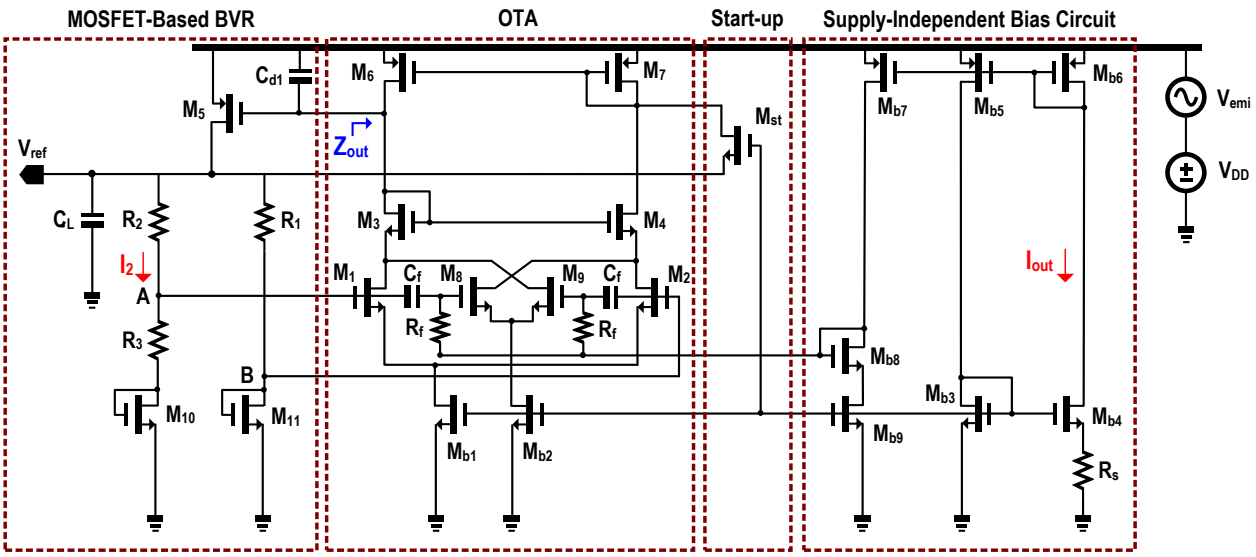


Fig. 2 Proposed EMI-resisting Bandgap voltage reference.

nodes. The substitution of BJT (Q_1-Q_2 in Fig. 1) to MOSFET (M_{10}-M_{11}) reduces the output reference voltage.

A. 1st-order Temperature-Independent BGR

In BJT, V_{BE} is complementary proportional to the absolute temperature (CPAT), which is obtained from the voltage across a forward biased p–n junction or the base-emitter voltage (V_{BE}) under diode connection. ΔV_{BE} is proportional to absolute temperature (PTAT) generated by taking the difference in the base-emitter voltages of two BJTs. In this design, V_{BE} has been changed to V_{GS} as the BJT is replaced by MOSFET. The device size of M_{10}-M_{11} should have a large aspect ratio in order to let it to have the BJT characteristics, but the TC is still not as good as that of BJT. For a sub-threshold-biased MOSFET with a drain-source voltage V_{DS} >0.1V, the sub-threshold current can be expressed as,

$$I = I_o \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{1}$$

where $I_o = (W/L)\mu C_{ox} V_T{}^2(\eta - 1)$ is the pre-exponential factor of the sub-threshold current; μ is the carrier mobility, $C_{ox}(= \varepsilon_{ox}/t_{ox})$ is the gate-oxide capacitance; ε_{ox} is the oxide permittivity; t_{ox} is the oxide thickness; η is the sub-threshold slope factor; V_{GS} is a gate-source voltage, $V_T(= K_B T/q)$ is the thermal voltage; K_B is the Boltzmann constant, T is the absolute temperature; q is the elementary charge and V_{TH} is the threshold voltage of the MOSFET [4]. Then, V_{GS} can be deduced as [5],

$$V_{GS} = V_{TH} + nV_T\left[\ln C - \ln\frac{W}{L} + (\gamma - 2)\ln T\right] \tag{2}$$

where n and γ are constants related with the CMOS process, and C is related with the current in the sub-threshold region. If $(W/L)_{11} > (W/L)_{10}$, the 1st-order derivative of ΔV_{GS} is PTAT,

$$\Delta V_{GS} = V_{GS11} - V_{GS10} = nV_T \ln\frac{(W/L)_{11}}{(W/L)_{10}} \tag{3}$$

By evaluating the current (I_2) passing through R_3,

$$I_2 = \frac{\Delta V_{GS}}{R_3} = \frac{nV_T}{R_3}\ln\frac{(W/L)_{11}}{(W/L)_{10}} \tag{4}$$

the expression of V_{ref} can be obtained,

$$\begin{aligned} V_{ref} &= V_{GS10} + I_2 \times (R_2 + R_3) \\ &= V_{GS2} + nV_T \ln\frac{(W/L)_{11}}{(W/L)_{10}}\frac{R_2 + R_3}{R_3} \end{aligned} \tag{5}$$

where V_{GS} is CPAT. By properly choosing those device sizes, V_{ref} becomes highly insensitive to temperature. If a precise V_{ref} is desired that must be out of the temperature drift, 2nd-order or exponential-compensated optimization procedures can be applied [5].

B. OTA with Double Differential Pair

In order to realize a BGR with higher EMI robustness, the double differential pair [6] combining DC-coupling and AC-coupling techniques to self-cancel the high-frequency inputs are applied here. With it, the output impedance of the OTA as well as the stability of the positive feedback will not be affected. The output resistance (Z_{out}) of the OTA is given by,

$$Z_{out} = \frac{r_{o6}}{1 + r_{o6}\frac{r_{o1}\|r_{o9} - r_{o2}\|r_{o8}}{(r_{o1}\|r_{o9}) \times (r_{o2}\|r_{o8})}} \quad (6)$$

If we assume M_1-M_2 and M_8-M_9 are equally sized, and there is no mismatch, Z_{out} can be simplified as,

$$Z_{out} \approx \frac{r_{o6}}{1 + r_{o6}\frac{r_o/2 - r_o/2}{(r_o/2)^2}} = r_{o6} \quad (7)$$

which implies that Z_{out} is masked by a positive feedback of the current mirror M_3-M_4, mostly determined by the channel length of M_6. The open-loop gain of the OTA is now changed from $2 * (r_{o6}\|r_{o1})/(1/g_{m1} + 1/g_{m2})$ to

$$2 * r_{o6}[\frac{1}{(1/g_{m1} + 1/g_{m2})} - \frac{1}{(1/g_{m8} + 1/g_{m9})}] \quad (8)$$

Thus, it is possible to achieve zero gain if the high-frequency transconductance satisfies,

$$g_{m1} + g_{m2} - g_{m8} - g_{m9} = 0 \quad (9)$$

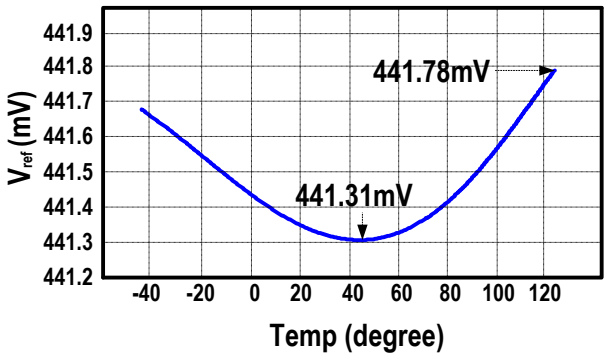
Accordingly, the high-frequency differential EMI at the OTA's input will be eliminated at the output node for the zero OTA gain. The output node will only be affected by the EMI injected from the power supply through M_6-M_7. To ensure the DC loop gain ≠ 0 and V_A=V_B (see Fig. 2), the highpass corner of the AC coupling network (R_f and C_f) is set at 150kHz since the EMI full range is normally from 150kHz to 1GHz, as specified in the direct power injection (DPI) specification [7].

Another advantage of the double differential pair is the DC shift as it helps to stabilize the drain voltage. The presence of a conducted electromagnetic disturbance on the inputs of a differential pair induces an output offset current due to distortion [8]. For a differential disturbance at the input, the unequal differential drain current effect will be cancelled since one increases/ decreases, the other will counteract it in the same amount. The differential pair M_8-M_9 can compensate the offset current generated by M_1-M_2 due to the EMI distortion. For a common-mode disturbance at the input, the current changes at the two drain nodes will be the same, and it will be restricted by the tail current.

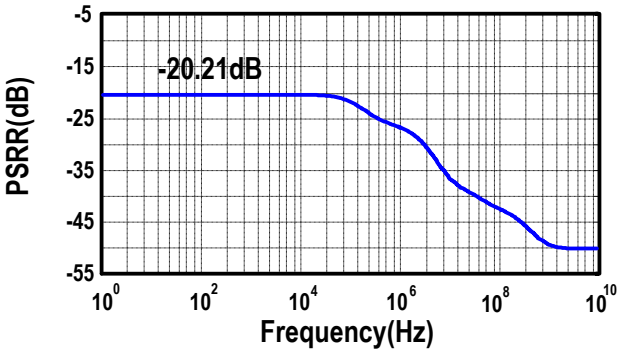
Since the OTA's output voltage is almost unaffected by using such a double differential pair, the PSRR is related only to the equivalent output loading R_L ($R_{1\text{-}3}$ and M_{10}-M_{11}) as well as the output resistance of M_5, where R_L can be expressed as,

$$R_L = (R_1 + 1/g_{m11})\|(R_2 + R_3 + 1/g_{m10}) \quad (10)$$

where R_1=R_2, node voltages A and B are forced to have the same potential to ensure an equal current passing through them. Since $1/g_{m11} = 1/g_{m10} + R_3$, they can be neglected when compared with the value of R_1 and R_2. Thus, R_L can be simplified as



(a)



(b)

Fig. 3 Simulated (a) v_{ref} versus temperature, (b) PSRR variation with frequency.

$$R_L \approx R_1\|R_2 = \frac{R_1}{2} \quad (11)$$

Based on it, the PSRR in DC range can be expressed as,

$$PSRR = \frac{R_L}{r_{o5} + R_L} \approx \frac{R_1}{2r_{o5} + R_1} \quad (12)$$

For high frequency, dominant parasitic capacitances should be taken into consideration.

C. Power Supply-Independent Bias and Start-up Circuit

In [9], the bias current entails the MOSFETs to be biased into the strong inversion region thus the voltage drop across the resistor is large. To reduce the bias current, a large resistance is unavoidable, taking more space and inducing more noise.

For the employed solution, a power supply-independent bias is applied. With it, the bias current is resisting to EMI from the power supply as long as its level is within the transistor's voltage swing,

$$I_{out} = \frac{2}{(W/L)_N \mu C_{ox}} \frac{1}{R_s^2}(1 - \frac{1}{\sqrt{K}})^2 \quad (13)$$

where K is the ratio of device size for M_{b4} to

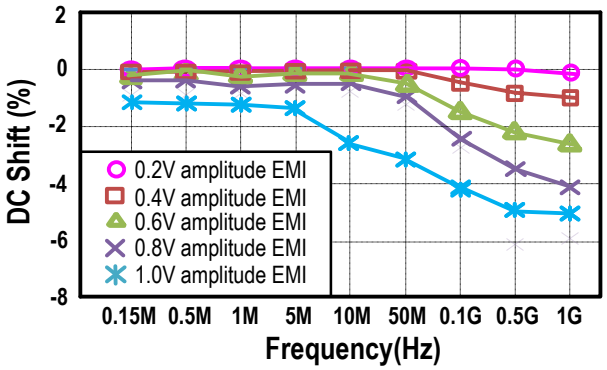


Fig. 4. DC shift of V_{ref} against different EMI amplitudes.

TABLE I.
SIMULATED PERFORMANCE

Parameter		Value
TC (ppm/°C)		10.65
Power Consumption (μW)		104
Max EMI resisting amplitude (V)		2
DC Shift under 4dBm EMI (%)		< 5
PSRR (dB)	@150 kHz	-21.61
	@1 GHz	-49.53

$M_{b3}(=(W/L)_{M_{b4}}/(W/L)_{M_{b3}})$. It is assumed that V_{TH} is the same for all the transistors and the channel length modulation is neglected. Thus, the current is only related to the size and the resistor value. Yet, the pre-condition to get it is that I_{out} cannot be zero. In this case, to ensure $I_{out} \neq 0$ and prevent operation in the undesired operation point, the start-up circuit (M_{st}) is added [10].

For the start-up circuit [1] given in Fig. 2, once the voltage at V_{ref} is close to zero, the gate of M_6 is pulled down by M_{st}, which in turn pulls up the voltage at the gate of the PMOS pass device M_5. Consequently, this forces V_{ref} to go up. Once V_{ref} arrives to the wanted bandgap voltage, M_{st} enters automatically in the cut-off region.

III. SIMULATION RESULTS

The proposed BGR was design and simulated in 1.2V 65nm CMOS. Fig. 3(a) plots the simulated V_{ref} as a function of the temperature which varies from –45° to 125°C. The maximum and minimum V_{ref} are 441.78mV and 441.31mV, respectively. Thus, the TC is 10.65 ppm/ °C. Fig. 3(b) plots the simulated PSRR versus frequency, from 1Hz to 10GHz. The low-frequency PSRR is roughly –20dB and it increases to –49.53dB at 1GHz. The TC and PSRR are traded-off against each other, as the equivalent R_L is related to both PSRR and TC.

Fig. 4 plots the simulated DC shift of V_{ref} with different EMI levels. The DC shift is <5% under a 4dBm EMI level. For a larger EMI, the large swing will force the MOSFET to clipping or rectification. For higher frequencies, this will be due to parasitic capacitances in the circuit which change the signal value and affect the DC shift. Table I summarizes the circuit performances.

IV. CONCLUSIONS

An EMI-resisting Bandgap Voltage Reference has been presented, which is based on the substitution of BJT by MOSFET for lowering the output voltage, and an OTA with a double differential pair and a power supply-independent bias to improve the EMI robustness. Simulated in 65nm CMOS, the output voltage is 441.3mV and the TC is 10.65ppm/ °C. The DC shift is <5% against a 4dBm EMI level with a total power consumption of 104μW.

ACKNOWLEDGEMENTS

This work is partially funded by the University of Macau Research Committee - MYRG114(Y1-L4)-FST13-MPI and the Macao Science and Technology Development Fund (FDCT) SKL fund.

REFERENCES

[1] J.-M. Redouté and M. Steyaert, *EMC of Analog Integrated Circuits*, Springer, 2009.

[2] A. Pretelli, A. Richelli, and Z. M. Kovacs-Vajna, "Reduction of EMI susceptibility in CMOS bandgap reference circuits," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 4, pp. 760–765, Nov. 2006.

[3] J.-M. Redouté and M. Steyaert, "M. Kuijk bandgap voltage reference with high immunity to EMI" *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 57, no.2, pp.75-79, Feb. 2010.

[4] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge Univ., 2002.

[5] I. Lee, G. Kim, and W. Kim. "Exponential curvature-compensated BiCMOS bandgap references," *IEEE Journal of Solid-State Circuits*, vol. 29, no.11, pp. 1396-1403, Nov. 1994.

[6] F. Fiori "Operational amplifier input stage robust to EMI," *IET Electronics Letters*, vol.37, no.15, pp. 930-931, 19 Jul. 2001.

[7] Measurement of E/M Immunity 150 kHz to 1 GHz-Part 4: Direct RF Power Injection Method, IEC 62132-4, Ed.1: ICs, 2004.

[8] Redouté, J-M., and Michel Steyaert. "EMI resisting CMOS differential pair structure." *Electronics Letters*, 42.21: 1217-1218, 2006.

[9] J.-M. Redouté and M. Steyaert, "Current mirror structure insensitive to conducted EMI," *IET Electronics Letters*, vol. 41, no. 21, pp. 1145–1146, Oct. 2005.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education, 2002.