Jitter-Resistant Capacitor Based Sine-Shaped DAC for Continuous-Time Sigma-Delta Modulators

Da Feng*, Franco Maloberti†, Sai-Weng Sin*, Seng-Pan U*‡, and R.P.Martins*§
*State-Key Laboratory of Analog and Mixed-Signal VLSI
Faculty of Science and Technology, University of Macau, Macao, CHINA
†Department of Electrical, Computer and Biomedical Engineering
University of Pavia,Via Ferrata, 1-27100 Pavia-ITALY
‡Also with Synopsys - Chipidea Microelectronics (Macao) Limited
§On leave from Instituto Superior Técnico/TU of Lisbon, PORTUGAL

***Abstract*—A novel current mode Capacitor Based Sine-Shaped (CBSS) Digital-to-Analog Converter (DAC) for Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulators, enabling smooth zero current transitions and greatly reducing the clock jitter noise, is described. The circuit is switched capacitor based and uses a cosine-wave voltage reference instead of constant current. The output is a sine-shaped waveform with precise zero transitions. Locking the reference cosine-wave voltage and the clock employed for data sampling ensures a virtual immunity to clock jitter. The use of a cosine-wave as reference and a constant capacitance loading the reference generator facilitates impedance matching thus making the scheme suitable for very high sampling rate. Moreover, the good matching between capacitors determines the accuracy of the integrators' time constant and multi-bit linearity of the proposed DAC. The feature of the method has been verified with behavioral simulations and tested in a second order $\Sigma\Delta$ modulator.**

I. Introduction

Continuous-time $\Sigma\Delta$ modulators integrate the charge into capacitors in a smooth way. On the contrary, sampled data schemes inject entire charge packets sharply at the clock transitions. This imposes the operational amplifiers (op-amps) to have high slew-rates being necessary to avoid non-linearity. Even the DACs of CT schemes deliver charge in a smooth manner: this is typically done with a current generator which value is constant over the entire of the sampling period (or a large fraction of it). However, CT $\Sigma\Delta$ DACs are critical because of various reasons. One is that clock jitter causes inaccuracy, which corresponds to unshaped noise and causes a degradation in the Signal-to-Noise-Ratio (SNR) of the modulator [1]. The power of this noise over the entire Nyquist interval equals the full scale power attenuated by the ratio between jitter time and period of the current pulse. A second drawback comes from the poor linearity in multi-bit current steering converters, where unity elements become inaccurate when the full-scale currents is in the few μA range. In addition, there is a low accuracy in the absolute value of the current which is unrelated to the capacitor inaccuracy. The result is a time-constant error of the CT integrators, which causes noise transfer function alteration.

There are several solutions in the literature to address the above mentioned issues; they are able to compensate for one or two of them but not capable to fix all the limits. One solution is to distribute charge injection during the sampling period through RC network. For example, the switched capacitor with switched series resistor (SCSR) DAC with time constant that changes during the injection period is used to keep the current at a suitable level [2]. The idea uses capacitors, so ensures good matching, but the current waveforms are not optimal and the implementation is critical because of the need of a clock with very high frequency. Also, the use of resistors in series with capacitors smoothes the transients, but the switchings cause multiple sharp transitions anyway.

Another solution is the sine-shaped method proposed in [3]–[9], shapes the current with a control of the transistor gate by sinusoidal voltage in a way that bit transitions occur when current is the minimum (or zero). Because all these implementations generate the sine-shaped like current by transistor, here we name this kind of sine-shaped DAC as Transconductance Based Sine-Shaped (TBSS) DAC. Although in theory the solution of Sine-Shaped DAC is more effective [10], obviously, the implementation of TBSS DAC is not able to achieve the accurate, symmetrical and without bias term sine-wave current because the voltage-current relationship of transistors is not linear, so the amounts of the positive and negative charge for "0" and "1" are not completely equal, which results in a non-linear error. A key limit also comes from the accuracy of the large-signal transconductance g_m. It has a large absolute error, which can be as much as $20-30\%$ during fabrication, and a mismatch error, given by the quadratic superposition of the error caused by capacitor and g_m mismatch, which can be $2-3\%$. Inaccuracy of g_m is not related to the capacitor inaccuracy in the integrator, thereby results in the time constant inaccuracy and multi-bit applications nonlinearity. As a result, the implementations based on TBSS DAC are not able to provide large SNR [5] and Signal-to-Noise-and-Distortion Ratio (SNDR) [7], [9].

The solution of CBSS DAC proposed in this paper avoids all the above mentioned limits while ensuring a smooth charge injection. The circuit minimizes the clock jitter influence. Moreover, being the operation based on capacitors, matching between them determines multi-bit linearity and time constant accuracy.

II. Proposed CBSS DAC

It is well known that a cosine-wave voltage across a capacitor gives rise to a sine-shaped current. The capacitive

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current is positive during one semi-period and negative during the other. This observation is the basis of the DAC proposed here. With suitable current switching it is possible to deliver the positive or the negative semi-periods toward the virtual grounds of a fully differential integrator under the control of the bit under conversion and its complement. The use of an array of unit capacitors driven by the same cosine-wave signals enables multi-bit DAC implementations. A key feature of the idea is that the circuit doesn't utilize a constant voltage or a constant current as the reference as it is done by conventional schemes but employs a differential cosine wave voltage whose frequency is half of the clock rate. That choice involves a side benefit because the use of sinusoidal signals facilitates matching between source and load thus permitting very-high switching frequency. This is, from a practical point of view, a big advantage.

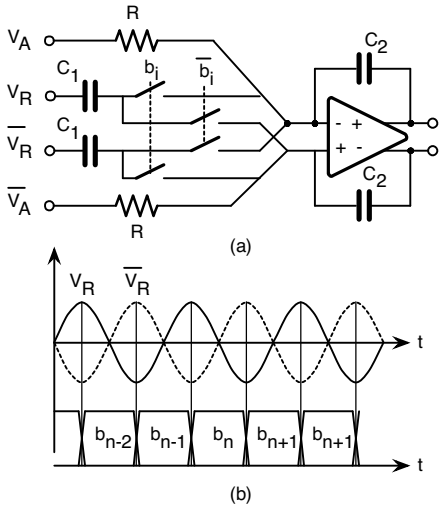


Fig. 1. (a) Block diagram of an integrator with a 1-bit CBSS DAC at input. (b) Waveforms and bit timing.

Fig. 1 (a) illustrates the schematic of the proposed fully differential integrator with single-bit DAC at input. There are two switched structures driven by the bit and its complement (b_i and $\bar{b}_i$) and two differential reference cosine waves (V_R and $\bar{V}_R$). The bit transitions occur at the zero crossings of the current and the switches direct the current toward the proper virtual grounds for injecting the current into the positive or the negative terminal, depending on the bit value. Matched resistors connected to the virtual grounds realize the integration of the analog voltages V_A and $\bar{V}_A$. Fig. 1 (b) shows the references and the bit transitions timing. Since the bit transition occurs when the current crosses zero, a possible jitter in the clock determines a minimum error. If the amplitude of the cosine wave is V_{FS}, the current injected into the virtual ground is

$$I(t) = V_{FS}C_1\pi/T_s \cdot sin(\pi t/T_s) \tag{1}$$

with an average value over the sampling period T_s of $2V_{FS}C_1/T_s$. The maximum is therefore $\pi/2$ times bigger than the average.

A jitter t_{ji} in the clock driving a conventional DAC used in a CT $\Sigma\Delta$ causes a noise proportional to the jitter. The noise voltage, considering the entire Nyquist interval is

$$\sqrt{\sigma^2_{n,ji,c}} = V_{n,ji,c} = \sqrt{2}V_{FS}t_{ji}/T_p \tag{2}$$

where $\sqrt{2}$ accounts for uncorrelated jitter of the rise and falling sides of the current pulse and T_p is the pulse duration. For a non-return-to-zero (NRZ) DAC $T_p = T_s$.

For a sine-wave shaped current with switching transition at the zero crossing, the noise voltage is

$$\sqrt{\sigma^2_{n,ji}} = V_{n,ji} = \frac{\sqrt{2}\pi^2}{4}V_{FS}\left(\frac{t'_{ji}}{T_s}\right)^2 \tag{3}$$

The jitter t'_{ji} used by (3) is not the absolute jitter but the difference between the jitter of the sine wave current and the clock jitter. This error can be minimized by locking clock and reference cosine waves. In this case the limit does not come from two unrelated jitters but from the error caused by the locking operation. The result is a de-sensitization of the jitter error compared to the NRZ case ($T_p = T_s$) by a factor $(\pi t'_{ji})^2/(4t_{ji}T_s)$, which is small even because t'_{ji} is lower than t_{ji}.

The peak to peak amplitude of the cosine waves used as reference determines the injected charge. Introducing a slight clipping of the cosine wave causes irrelevant consequences. However, it determines a short period with zero current through the capacitor. This ensures jitter immunity if jitter fits within the zero current period.

III. Use in a CT $\Sigma\Delta$ Modulator

The jitter sensitivity of the CBSS DAC has been tested with a conventional second order $\Sigma\Delta$ modulator. The simulation vehicle is Matlab. At the same time, the same simulation study was performed using the traditional switched-current rectangular NRZ (SI-NRZ) DAC.

A. Charge error caused by the clock jitter

In the ideal case, the CBSS DAC and the SI-NRZ DAC produce perfect current waveforms like ones shown in Fig. 2(a).

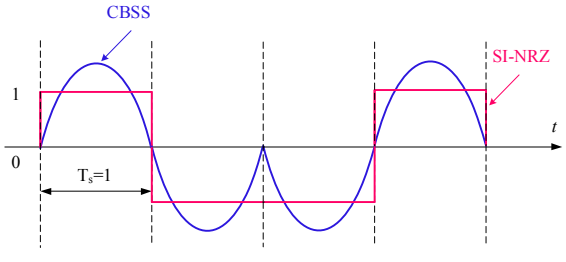
To simplify the analysis, we normalized all parameters and suppose that two references are 1 and -1 for the SI-NRZ DAC. The sampling period is 1. The SI-NRZ DAC current pulse determines the total feedback charge in one sampling period. It is given by

$$Q_{SI-DAC} = \int_0^1 1dt = 1 \tag{4}$$

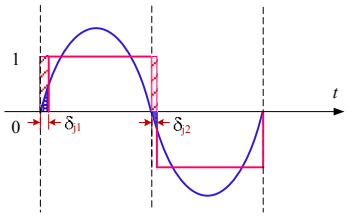
The CBSS DAC should feed back the same amount of charge during the same sampling period as the SI-NRZ DAC. Suppose the amplitude of the sine-shaped current is A, so we have

$$Q_{CBSS} = \int_0^1 Asin(\pi t)dt = 1 \tag{5}$$

That is $A = \pi/2 \approx 1.57$, being only 57% larger than in the SI-NRZ case, that means the op-amp slew rate requirement is also relaxed significantly using the CBSS DAC, compared



(a) Ideal DAC current waveforms



(b) Jittered DAC current waveforms

Fig. 2. Output current waveforms from the DACs.

with sampled data scheme with switched capacitor techniques. The use of the CBSS DAC augments the peak value and costs a limited increase of the driving capability of the op-amp, but having a 57% higher driving capability is not a significant limit because the currents necessary to ensure the required unity gain frequency are capable to sustain the necessary driving capability. Also the use of CBSS DAC brings two benefits compared with the traditional SI-NRZ DAC: (1) The initial current starts always from zero thus greatly relax the op-amp slew-rate requirement; (2) the DAC current is zero also in the end of the injection and this can even relax the op-amp small-signal bandwidth requirement and increased the integration accuracy.

In a real situation, the current waveforms are affected by clock jitter, for example, they may become the waveforms shown in Fig. 2(b), where only the first two jitter errors are outlined. For the SI-NRZ DAC, the charge error in one sampling period can be given by

$$\triangle Q_{SI-NRZ} = \pm \int_0^{|\delta_{j1}|} 1dt \mp \int_0^{|\delta_{j2}|} 1dt = \delta_{j1} - \delta_{j2} \quad (6)$$

where δ_{j1} and δ_{j2} are the clock jitter errors at the rise and falling edge of the current pulse. They can be expressed by uniformly distributed random numbers which can be positive or negative.

For the CBSS DAC, the charge error in the same sampling period can be given by

$$\begin{aligned} \triangle Q_{CBSS} &= \pm \int_0^{|\delta_{j1}|} \tfrac{\pi}{2} sin(\pi t)dt \pm \int_0^{|\delta_{j2}|} \tfrac{\pi}{2} sin(\pi t)dt \\ &= \pm sin^2(\tfrac{\pi}{2}\delta_{j1}) \pm sin^2(\tfrac{\pi}{2}\delta_{j2}) \end{aligned} \quad (7)$$

Because $\delta_{j1} \ll 1$ and $\delta_{j2} \ll 1$, we have $sin(\delta_{j1}\pi/2) \approx \delta_{j1}\pi/2$, and $sin(\delta_{j2}\pi/2) \approx \delta_{j2}\pi/2$, so (7) can be written as

$$\triangle Q_{CBSS} = \frac{\pi^2}{4}(\delta_{j1}|\delta_{j1}| + \delta_{j2}|\delta_{j2}|) \quad (8)$$

B. Proposed jitter Simulink model

Based on (6) and (8), we built the jitter error Simulink models for the two different DACs in a conventional second order CT $\Sigma\Delta$ modulator to compare the sensitivity to the jitter in the clock between the SI-NRZ and the proposed DAC, as shown in Fig. 3 and Fig. 4.

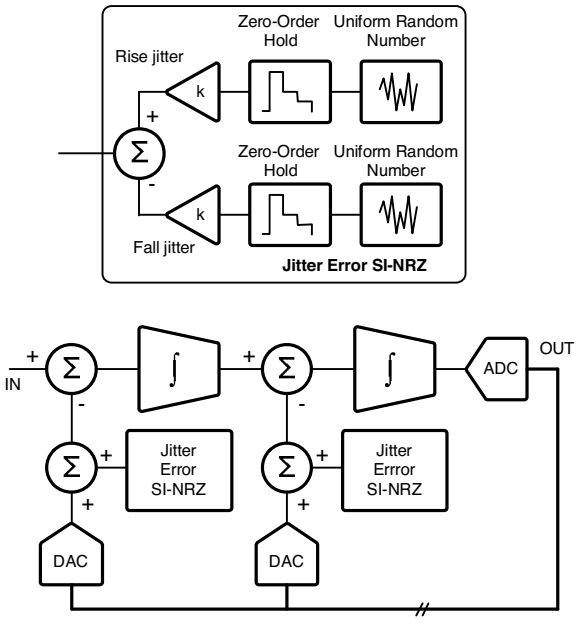


Fig. 3. Jitter error Simulink models for the SI-NRZ DAC.

Four "Uniform Random Number" Simulink modules with different seeds in two DACs are used to generate four uniformly distributed random numbers between -1 and 1. After sample and hold modules, they are multiplied by a gain coefficient k to simulate δ_{j1} and δ_{j2}. Then, by changing the coefficient k, we can emulate different jitter errors. In order to compare each other with the same jitter error, for SI-NRZ DAC and the CBSS DAC, the corresponding seeds in "Uniform Random Number" Simulink modules are the same.

Also, four function blocks are needed to give the charge errors of (8) in the jitter error Simulink model with the CBSS DAC, as shown in Fig. 4; while in the jitter error Simulink model with SI-NRZ DAC, as shown in Fig. 3, simply combining the two parts of clock jitters can get the result of (6), so no extra function blocks as in Fig. 4 are necessary.

C. Simulation results

The band of the signal is 20 MHz, the oversampling ratio is 16, so the sampling frequency is 640 MHz with a 4-bit DAC. The foreseen SNR is 71.6 dB, ($V_{ref} = \pm 1V$ and the amplitude of the input sine wave is $0.9V$). The two modulators in Fig. 3 and Fig. 4 were simulated, and the clock jitter was swept from 0.01% to 10% of the clock period by changing

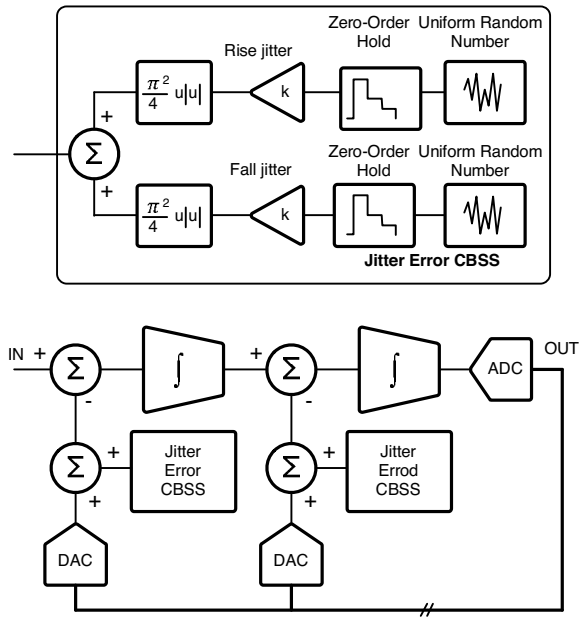


Fig. 4. Jitter error Simulink models for the CBSS DAC.

gain coefficient k. For each value of the clock jitter, the SNR of two modulators was measured and recorded.

Fig. 5 shows the simulation results. The SNR is at the expected value until a given jitter. Then the SNR drops significantly. From Fig. 5, it can be concluded that the CBSS DAC jitter-resistant performance is much better than the SI-NRZ DAC. If we consider the point where SNR decreases 3 dB as the standard of comparison, the CBSS DAC is able to tolerate the range of 2% of the clock jitter; while it is only 0.08% for the SI-NRZ DAC. That, with 640 MHz clock means a jitter should less than 1.25 ps, on the contrary, for the CBSS DAC it is 31.25 ps, 25 times larger than the one with a conventional DAC. To ensure a clock jitter in the ps range is challenging. For higher resolutions or higher clock frequency the jitter request is in the sub ps range.

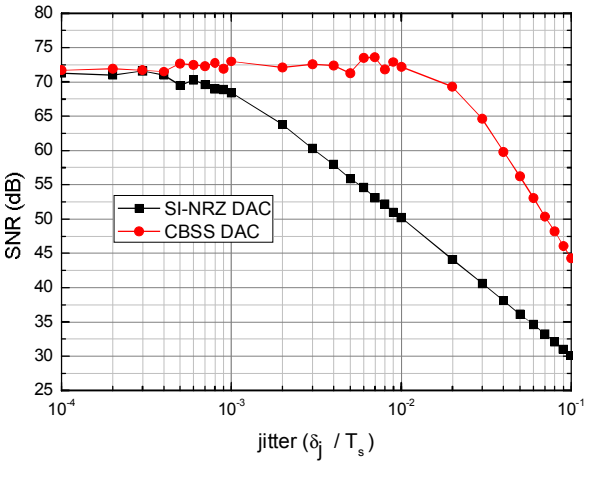


Fig. 5. SNR versus the clock jitter with a conventional SI-NRZ DAC and the CBSS DAC.

The gain of the integrator with the CBSS DAC is quite precise as the accuracy of the output voltage depends on the matching between the capacitor in the DAC and the integrating element. This avoids the need of time constant trimming often necessary in continuous CT $\Sigma\Delta$ modulators.

IV. Conclusion

In this paper, a novel CBSS DAC is proposed. Unlike the TBSS DAC, the CBSS DAC is able to generate real sine waveform current. The use of the CBSS DAC significantly reduces the drawbacks caused by clock jitter, time constant inaccuracy and multi-bit nonlinearity. The op-amp slew rate requests are also relaxed significantly at the same time. The method preserves the benefits of a conventional CT architecture.

Acknowledgment

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