Micropower Two-Stage Amplifier Employing Recycling Current-Buffer Miller Compensation

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***Abstract*—Proposed is a two-stage amplifier exploiting *recycling* current-buffer Miller compensation (CBMC). By reusing the most current-consuming devices in the 1st stage as current buffer, such an amplifier not only can preserve the merits of typical CBMC implementation in creating the beneficial left-half-plane (LHP) zero, but also can avoid the drawbacks of typical CBMC scheme from degrading the power efficiency, DC gain, dc offset and noise performances. Optimized in 0.18µm CMOS via a low-power design procedure, the amplifier achieves >90dB DC gain, 4.5MHz unity-gain frequency and 57.2° phase margin at a 100pF capacitive load. The average slew rate and 1% settling time are 2.68V/µs and 0.239µs, respectively. The amplifier draws 22µA at a 1.2V supply.**

I. INTRODUCTION

Two-stage amplifiers have underpinned a wide range of applications in analog circuits and subsystems due to its high DC gain and large output swing. The closed-loop stability is often secured via traditional Miller compensation (MC). The Miller capacitor, yet, induces a non-inverting feedforward signal path from the input of the 2nd stage to its output, creating an undesirable right-half-plane (RHP) zero [1]. The RHP zero can be eliminated by using a voltage buffer, nulling resistor, or adding a transconductance stage to cancel the feedforward signal. However, the scheme based on current buffer, i.e. current-buffer Miller compensation (CBMC), offers more design freedom in optimizing the gain-bandwidth product (GBW), power and area, while enhancing the capacitive load (C_L) drivability [2]. CBMC also exhibits significant power supply rejection ratio (PSRR) improvement over that of MC [3]-[4].

Existing implementation of a two-stage CBMC amplifier invariably employs a PMOS input folded-cascode (FC) stage for its lower flicker noise, farther non-dominant pole and wider input common-mode level that can reach the ground, in comparison with its NMOS FC stage counterpart. The current buffer is either separately realized, or embedded in the FC stage, as shown in Fig. 1(a) and (b), respectively [5]. Yet, both have a number of drawbacks: the former [Fig. 1(a)] consisting of M_{9a}-M_{11a} suffers from increased offset voltage owing to the inevitable DC current mismatch between M_{9a} and M_{11a}. Replica biasing can alleviate the current mismatch [6], but it entails add-on bias circuitry and shows supply dependence. Another critical issue is the current buffer M_{10a} burns a large portion of power; as M_{10a} should generate at least 2x g_{m1a} to guarantee reasonable stability margin [7], while g_{m1a} is generally set high, for noise consideration. This leads to significant current drawn by M_{10a} and the output resistance reduction in the FC stage, degrading the DC gain

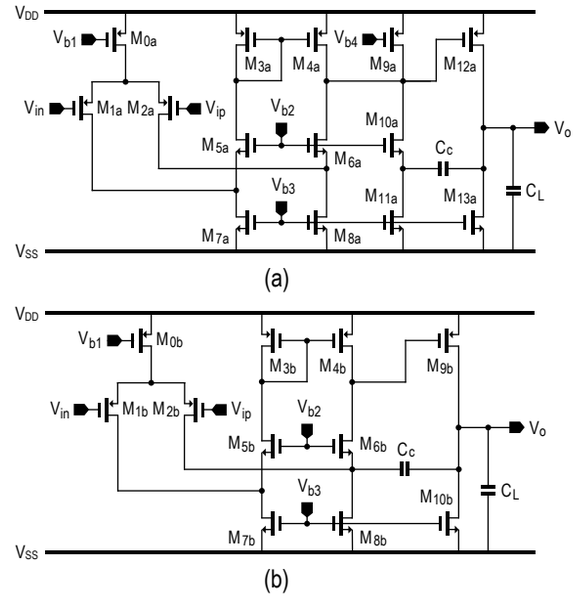

Fig. 1. Conventional two-stage CBMC amplifier implementations via: (a) a separate current buffer, and (b) an embedded one.

and hence the dc offset performance. M_{9a} and M_{10a} also add parasitic capacitance penalizing the maximum attainable GBW. They and their biasing circuitry also contribute significant noise due to their large bias current and noise amplification. The latter [Fig. 1(b)] embodies the current buffer M_{6b} in the FC stage and avoid the mismatch problem and extra circuit overhead in Fig. 1(a). However, the removal of RHP zero is incomplete, even being placed higher than that in traditional MC [5]. Moreover, the left-half-plane (LHP) zero is far beyond that of Fig. 1(a), benefiting little to the phase margin (PM). Similarly, the issue of M_{6b} dominating the power of the FC stage has yet to be solved. Instead, M_{5b} drains the same amount of current as M_{6b} to balance the two folded branches, doubling the power budget. Thus, Fig. 1(b) is inferior to Fig. 1(a) in terms of power efficiency.

This paper proposes a power-efficient recycling CBMC amplifier by recycling the most power-hungry devices in the FC stage as current buffer. The concise implementation not only inherits the advantages of both embodiments in Fig. 1 but also eliminates their drawbacks. Moreover, the proposed amplifier consumes less power and preserves a key LHP zero to benefit the PM, while being free from mismatch, extra auxiliary circuitry and gain reduction. A low-power design procedure is also described, which essentially leads to low power dissipation of the entire amplifier.

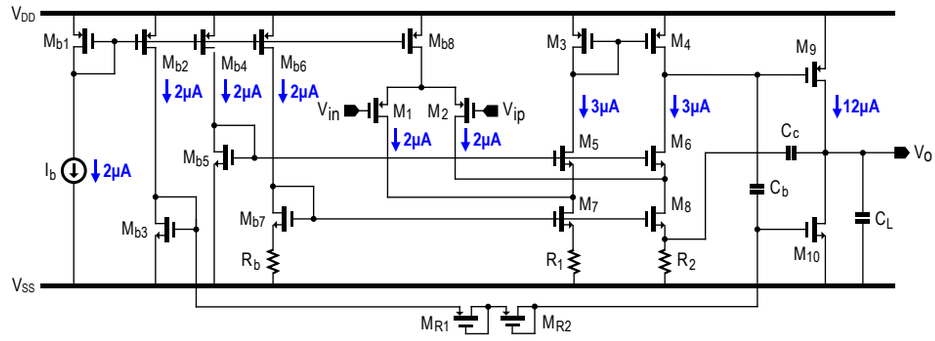

Fig. 2. The schematic of proposed two-stage recycling CBMC amplifier.

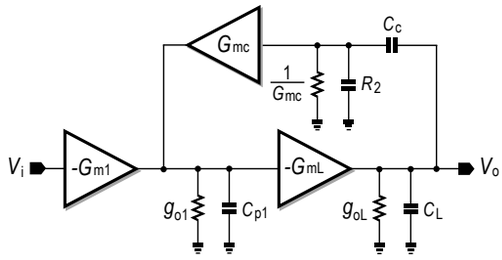

Fig. 3. Small-signal diagram of proposed recycling CBMC amplifier.

II. Proposed Recycling CBMC Two-Stage Amplifier

Recalling Fig. 1, M_{7a}-M_{8a} and M_{7b}-M_{8b} in the FC stages conduct most of the current and contribute a big amount of transconductances, but their roles are only limited to provide the folded nodes. In fact, these transistors can be degenerated to form current buffers, recycling their transconductances. Fig. 2 shows the schematic of the proposed two-stage recycling CBMC amplifier; M_1-M_8 together with R_1 and R_2 form the modified input FC stage where C_c, M_8, and R_2 implement the recycling CBMC. Instead of using transistors, degenerating M_7 and M_8 via small values R_1 and R_2 avoid the large voltage drop across them. Also, they induce no flicker noise and less thermal noise, while suppressing both generated by M_7 and M_8. The 2nd stage is realized by M_9-M_{10}. Since CBMC offers targets on applications that have to drive a large C_L, a class-AB output stage is necessary to obtain a symmetrical slew rate (SR). This is achieved by adding C_b and two diode-connected transistors M_{R1}-M_{R2}, which act as pseudo resistors to provide AC resistance on the order of 100GΩ. They are in series with C_b operating like a level shifter that dynamically transfers the signal variation at the gate of M_9 to that of M_{10}. Unlike [8], one more diode-connected transistor is cascaded, preventing M_{R1}-M_{R2}, and their parasitic devices, from conducting when experiencing doubled transients.

A. Transfer Functions

The small-signal equivalent model of the recycling CBMC two-stage amplifier is depicted in Fig. 3. G_{m1} denotes the effective transconductance of the FC input stage, which is approximated by g_{m1}. G_{mL} is the sum of M_9 and M_{10}'s transconductances because of their class-AB operation. G_{mc} models the recycling current buffer with its input resistance being $(1/G_{mc})//R_2$. $g_{o1,L}$ and $C_{p1,2}$ denote, respectively, the lumped output conductance and parasitic capacitance of each stage, where C_{p2} is grouped into C_L. With the assumptions: 1) the DC gain of each stage is >> 1; 2) $C_L >> C_c$ and $C_c >> C_{p1}$, the open-loop and closed-loop transfer functions $A_v(s)$ and $A_{cl}(s)$ are derived, respectively,

$$A_v(s) \approx \frac{G_{m1}G_{mL}}{g_{o1}g_{oL}} \frac{1+s\frac{R_2C_c}{G_{mc}R_2+1}}{\left[1+s\frac{G_{mL}C_cG_{mc}R_2}{g_{o1}g_{oL}(G_{mc}R_2+1)}\right]\left[1+s\frac{C_{p1}C_L(G_{mc}R_2+1)}{G_{mL}C_cG_{mc}R_2}+s^2\frac{C_{p1}C_L}{G_{mc}G_{mL}}\right]} \quad (1)$$

$$A_{cl}(s) = \frac{A_v(s)}{1+A_v(s)} \approx \frac{1+s\frac{R_2C_c}{G_{mc}R_2+1}}{1+s\frac{(G_{m1}+G_{mc})C_cG_{mc}R_2}{G_{m1}G_{mc}(G_{mc}R_2+1)}+s^2\frac{C_{p1}C_L}{G_{m1}G_{mL}}+s^3\frac{C_{p1}C_cC_LG_{mc}R_2}{G_{m1}G_{mc}G_{mL}(G_{mc}R_2+1)}} \quad (2)$$

B. Stability Analysis, GBW, and Phase Margin

To stabilize the amplifier, the denominator of (2) is configured as the 3rd-order Butterworth polynomial, yielding,

$$G_{mc} = 3G_{m1}, \quad (3)$$

$$G_{mL} = \frac{9C_{p1}C_L}{8C_{eq}^2}G_{m1}. \quad (4)$$

where $C_{eq} = C_cG_{mc}R_2/(G_{mc}R_2+1)$ is the equivalent Miller capacitor. From (1), the amplifier's DC gain and dominant pole are $A_{DC} \approx G_{m1}G_{mL}/g_{o1}g_{oL}$ and $p_{-3dB} \approx G_{mL}C_cG_{mc}R_2/g_{o1}g_{oL}(G_{mc}R_2+1)$, respectively. Hence, the GBW is $A_{DC}\cdot p_{-3dB} \approx G_{m1}/C_{eq}$. Substituting (3) and (4) into (1), $A_v(s)$ is simplified as,

$$A_v(s) \approx \frac{A_{DC}\left(1+\frac{s}{3GBW}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left[1+\frac{8}{9}\frac{s}{GBW}+\frac{8}{27}\left(\frac{s}{GBW}\right)^2\right]}. \quad (5)$$

TABLE I
DEVICE SIZES AND VALUES OF THE RECYCLING CBMC AMPLIFIER.

Devices	Sizes (μm/μm)	Devices	Sizes (μm/μm)	Devices	Values
M_1/M_2	7.2/0.5 (x4)	M_{R1}/M_{R2}	0.5/0.5	R_1/R_2	16 kΩ
M_3/M_4	3.15/0.7 (x2)	$M_{b1}/M_{b2}/M_{b4}/M_{b6}$	6/2	R_b	40 kΩ
M_5/M_6	1.4/0.4 (x4)	M_{b3}	1.6/0.8	C_c	2.15 pF
M_7/M_8	1.2/0.6 (x5)	M_{b5}	0.5/10	C_b	1 pF
M_9	3.15/0.7 (x8)	M_{b7}	1.2/0.6 (x2)		
M_{10}	1.6/0.8 (x6)	M_{b8}	6/2 (x2)		

(5) indicates that the non-dominant complex poles $p_{2,3}$ locate around at 1.84x GBW with a damping factor ζ of 0.816 while the LHP zero z_{LHP} lies at 3x GBW that is critical to enhance the amplifier's PM. The exact PM is evaluated by solving (5) to obtain the unity-gain frequency (UGF) ω_μ, which is equal to 0.94GBW. Therefore, the PM is calculated as

$$PM = 90^\circ - \arctan\frac{2\zeta\frac{\omega_\mu}{|p_{2,3}|}}{1-\left(\frac{\omega_\mu}{|p_{2,3}|}\right)^2} + \arctan\frac{\omega_\mu}{z_{LHP}}$$

$$\approx 90^\circ - 49.2^\circ + 17.4^\circ = 58.2^\circ . \quad (6)$$

C. Slew Rate

With a class-AB output stage, the SR of the proposed amplifier is limited by the available current to charge or discharge C_c, which can be several times higher than the counterparts shown in Fig. 1. Supposing a large positive step occurs at V_{ip}, it follows that M_2 turns off and M_{b8} directs almost all its current into M_7. Consequently, M_3 drains only the difference current between M_7 and M_{b8}, which is further mirrored into M_4. To sink this mirrored current, the source voltage of M_8 has to rise since its gate voltage generated by M_{b7} is fixed. As a result, the current flowing R_2 is increased and most of them charges C_c. For a large negative step, M_8's source voltage must be reduced to support more current that discharges C_c. Depending on the bias current of M_8 and M_{b8} as well as M_8's size, the boosted current can be significant. Thus, the SR may not be smaller than that of typical implementation, even the proposed amplifier entails a bigger Miller capacitor (i.e. $C_c > C_{eq}$).

D. Proposed Low-Power Design Procedure

For given GBW and C_L, the current drawn by an amplifier can be minimized via optimizing the figure-of-merit (FOM): $IFOM_S = GBW \cdot C_L/I_Q$ [9], where I_Q stands for the amplifier's total quiescent current. Specifically, the $IFOM_S$ of the proposed amplifier is expressed as

$$IFOM_S = \frac{\frac{G_{m1}}{C_{eq}} \cdot C_L}{\frac{2G_{mc}}{(1+\eta_8)(\frac{g_m}{I_D})_{M8}} + \frac{G_{mL}}{(\frac{g_m}{I_D})_{M9} + (\frac{g_m}{I_D})_{M10}}} \quad (7)$$

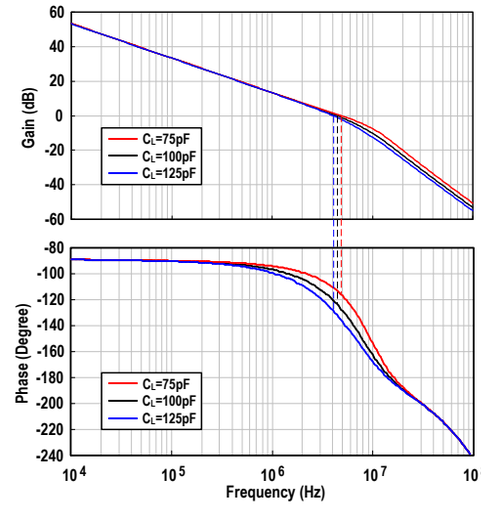

Fig. 4. Simulated AC responses of proposed recycling CBMC amplifier.

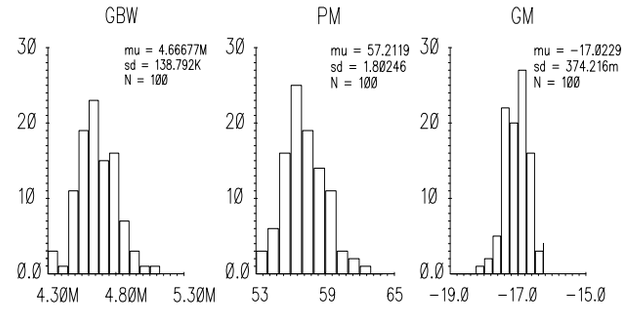

Fig. 5. Monte Carlo histograms for GBW, PM, and GM at 100pF C_L.

where $(g_m/I_D)_{M8\text{-}M10}$ are design variables to set the current-to-transconductance efficiencies of M_8-M_{10}. η_8 equals g_{mb8}/g_{m8}. Using (3) and (4), (7) is modified as

$$IFOM_S = \frac{C_L}{\frac{6C_{eq}}{(1+\eta_8)(\frac{g_m}{I_D})_{M8}} + \frac{9C_{p1}C_L}{8[(\frac{g_m}{I_D})_{M9} + (\frac{g_m}{I_D})_{M10}]C_{eq}}} \quad (8)$$

The maximum $IFOM_S$ is obtained by zeroing the derivative of (8) with respect to C_{eq}, which gives a concrete condition to determine G_{mL},

$$G_{mL} = \frac{6[(\frac{g_m}{I_D})_{M9} + (\frac{g_m}{I_D})_{M10}]}{(1+\eta_8)(\frac{g_m}{I_D})_{M8}} G_{m1} . \quad (9)$$

Since both g_{m9} and g_{m10} contribute to G_{mL} while C_{p1} is dominated by the parasitic capacitances at the gates of M_9 and M_{10}, $\omega_T \approx G_{mL}/C_{p1}$ can be defined as the composite cut-off frequency of M_9 and M_{10} operating as a class-AB stage. ω_T is almost a constant once the channel lengths of M_9-M_{10} and $(g_m/I_D)_{M9\text{-}M10}$ are specified. So, it can be used to select C_{eq} via transforming (4), as shown below,

$$C_{eq} \approx \frac{9GBW}{8\omega_T} C_L . \quad (10)$$

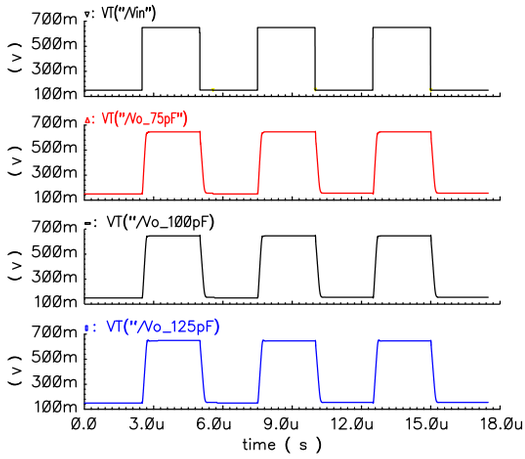

Fig. 6. Simulated step responses of proposed recycling CBMC amplifier.

With the above equations, the proposed design procedure is easy-to-use, as summarized in the following steps: first, estimate C_{eq} according to (10) with specific GBW and C_L; determine G_{m1} from GBW and C_{eq}; finally, obtain G_{mc} and G_{mL} according to (3) and (9), respectively.

TABLE II
PERFORMANCE SUMMARY OF THE AMPLIFIER AT DIFFERENT C_L.

	This Work (Simulation)			Ref. [9]
Load C_L (pF)	75	100	125	150
GBW (MHz)	4.9	4.5	4.1	4.4
Phase Margin (°)	64.8	57.2	51.9	57
Gain Margin (dB)	**15.9**	**17.0**	**17.9**	5
Average SR (V/μs)	**2.76**	**2.68**	**2.47**	1.8
Average 1% T_S (μs)	**0.258**	**0.239**	**0.245**	1.23
DC Gain (dB)	92			110
Power (μW) @ V_{DD} (V)	**26.4@ 1.2**			**30@ 1.5**
Input-Ref. Noise Density (nV/√Hz @ 100KHz)	58			N/A
Total Capacitance (pF)	3.15			1.6
CMOS Technology	0.18 μm			0.35 μm
$IFOM_S$ [(MHz·pF)/mA]	16,705	20,455	23,295	33,000
$IFOM_L$ [(V/μs·pF)/mA]	9,409	12,182	**14,034**	13,500

III. SIMULATION RESULTS

To validate the recycling CBMC scheme, a two-stage amplifier is designed in 0.18μm CMOS using the proposed low-power design procedure. The amplifier driving a C_L of 100pF targets about a 5MHz GBW under a 1.2V supply. Since MOS transistor has fundamental trade-offs among its intrinsic gain, speed, and (g_m/I_D), carefully selecting the M_9-M_{10}'s channel lengths and $(g_m/I_D)_{M9\text{-}M10}$ is necessary to balance these metrics, which leads to a C_{eq} of only 1.43pF in this design. The bias current of each stage and its biasing circuitry are shown in Fig. 2. R_1 and R_2 are set to 16kΩ, producing 80mV voltage drops. Table I summarizes the sizes and values of all the devices. At the typical corner the simulated key parameters: G_{ml}, G_{mL}, and G_{mc} are 43.6, 383 and 124.1μS, respectively. Fig. 4 shows the typical AC responses. The DC gain is >90dB (not shown). At C_L=100pF, the UGF, PM and gain margin (GM) are 4.5MHz, 57.2˚, and 17dB, respectively. The PM is 1˚ less than that predicted by (6), which is mainly attributed to the parasitic pole associated with M_5-M_6 that not modeled in Fig. 3. The three metrics show less than 14% degradation when the nominal 100pF C_L deviates ±25%. The robustness of the amplifier has been verified by Monte Carlo simulations (Fig. 5). The standard deviations in GBW, PM and GM are reasonably small, validating the feasibility of the Butterworth stabilization scheme and the proposed design procedure. In unity-gain configuration, the step responses of C_L at 75, 100 and 125pF are shown in Fig. 6, respectively. The average SR and 1% settling time are 2.68V/μs and 0.239μs for C_L=100pF. The detailed performance is summarized in Table II. The achieved small- and large-signal FOMs: $IFOM_S$ and $IFOM_L$ are well-comparable with recent three-stage amplifier with similar C_L drivability [9].

IV. CONCLUSIONS

Recycling the power-consuming devices in the common FC input stage as current buffer is proposed. It offers a concise and power-efficient CBMC solution for two-stage amplifiers. The recycling scheme overcomes the drawbacks of typical CBMC embodiments, while preserving their advantages. The effectiveness is confirmed via designing a two-stage amplifier with the proposed low-power design procedure. Simulation results suggest that the FOMs achieved are well-comparable with advanced three-stage amplifiers.

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