Switched-Current-Assisting and Pre-Charging Techniques for SC Low-pass Filters

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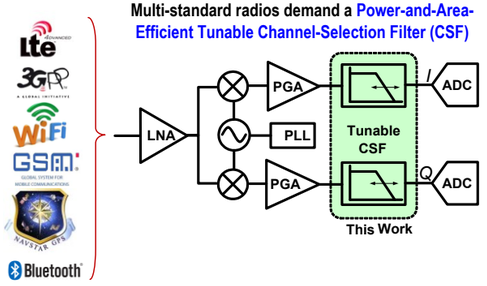
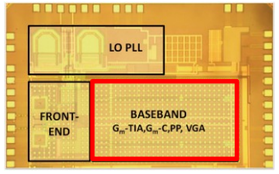
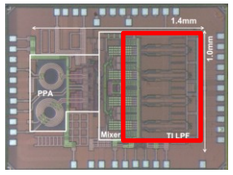
Research Backgrounds

Multi-standard radios demand a Power-and-Area-Efficient Tunable Channel-Selection Filter (CSF)

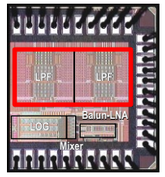




SDR Receiver [J. Borremans ISSCC'11]



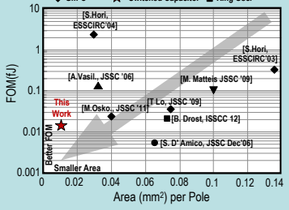
Multi-band LTE RX [M. Ingels ISSCC'13]



Mobile-TV RX [P. Mak ISSCC'11]

Entered into the nanoscale CMOS regime, the die area of wireless chips is dominated by the baseband I/Q channel-selection lowpass filters (LPFs). To address this issue, this work revisits the switched-capacitor (SC) LPF for its unique benefits of *clock-rate-defined bandwidth*, *cutoff accuracy* and *compact implementation*. The main challenges are the speed, linearity and power tradeoffs, which are surmounted here via two circuit techniques: the first is a ***Switched-Current-Assisting (SCA) path*** aiding the charging of *integration capacitor* passively, leaving only the final error correction to be performed by the main OTA. The second is a ***Pre-Charging (PC) path*** for speedily charging the *load capacitor* with simple hardware reuse from the SCA path. Both techniques are embedded into the design of a 5th-order Butterworth SC LPF. At the same power (5.6 mW) and bandwidth (10 MHz), the IIP3 reaches **+23.5 dBm** (+15.3 dBm) and the -3dB cutoff accuracy is **97%** (82%) with (without) the SCA + PC paths. The clock-defined bandwidth is scalable from **1.5 to 15 MHz**. A favorable **Figure-of-Merit (0.014 fJ)** is measured when compared with the state-of-the-art. The die area is merely **0.127mm²** in 65-nm CMOS.

	This Work	JSSC Jul'11 S. V. Thyagarajan	ISSCC'12 B. Drost	JSSC Sept'09 T. Lo
Technology	65 nm	90 nm	90 nm	180 nm
Architecture	Active SC + SCA + PC	Gm-C	Ring-Oscillator Integrator	Gm-C
Filter Order, *N*	5th, Butterworth	6th, Butterworth	4th, Butterworth	3rd, Butterworth
Bandwidth, BW (MHz)	1.5 to 15	8.1 to 13.5	7 to 30	0.5 to 20
BW Tuning	Clock Rate	Coarse (Cap Bank) Fine (Current)	Supply Voltage	Bias Current
In-Band IIP3 (dBm)	+23.5 @ 10MHz BW	+22.1 @ 10MHz BW	+16.7@ 7MHz BW	+20.5 @ 10MHz BW
IRN (nV/√Hz), P_N	35	75	23.7 to 32.8	12 to 425
Area/Pole (mm²/Pole)	0.0254	0.04	0.0725	0.077
Power (mW), P_C	2.3 to 7.8	4.35	2.9 to 19.1	4.1 to 11.1
FOM (fJ) *	0.014	0.024	0.0228	0.072

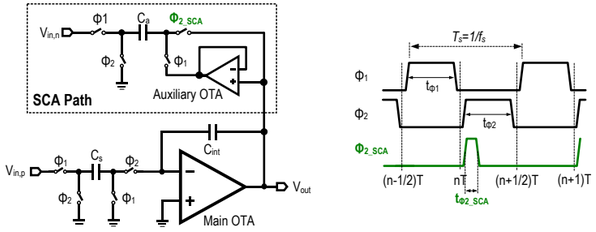


* $\text{FOM} = \frac{P_C/f_N}{BW \cdot \left(\left(\frac{IIP3}{P_N}\right)^{2/3} \cdot N^{4/3}\right)}$

This work achieves higher IIP3, better area efficiency, and better FOM with respect to the state-of-the-art.

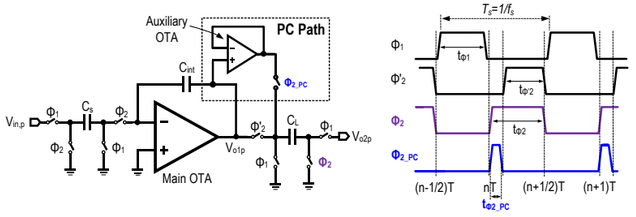
Proposed Switched Current Assisting (SCA) Technique

A **high-speed SCA path** sensing the anti-phased input (V_{in}) aids the main OTA to charge the integration capacitor (C_{int}) at **Φ_{2_SCA}**, leaving the main OTA only works for the final error correction. The auxiliary OTA acts as a low-power unity-gain buffer.

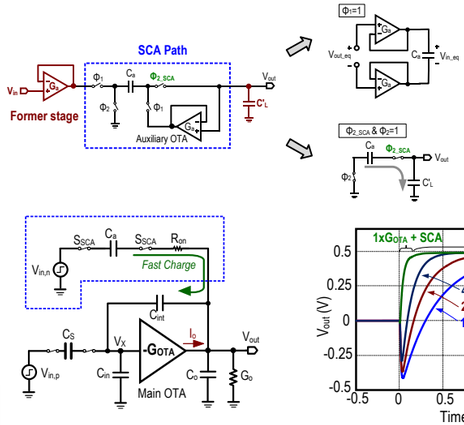


Proposed Pre-Charging (PC) Technique

When charging the load capacitor (C_L), a **PC path** clocked at **Φ_{2_PC}** can be added to relax the linearity requirement of the main OTA. Here, the high-speed auxiliary OTA from the SCA path (slide 6) can be reused for this purpose, rendering the SCA and PC techniques combinable in one SC integrator. Thus, the charging speed of both C_{int} and C_L are accelerated power-efficiently.

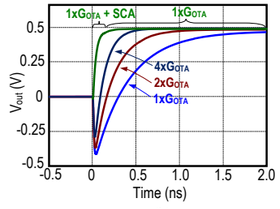


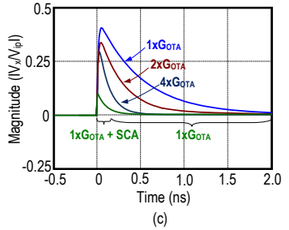
Simulated Improvement – SCA Technique



With the SCA path the G_{OTA}, the simulated **speed-to-power efficiency** is improved by **1.76x**.

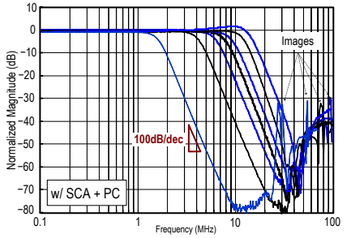
The main OTA is relaxed as it is only responsible for the rest error correction.



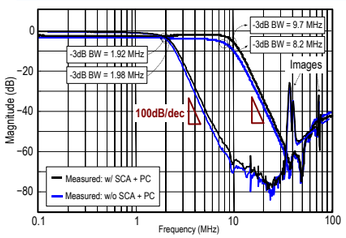


(a) Integrator with SCA path (b) Transient Output (c) Virtual Ground Transient Waveform

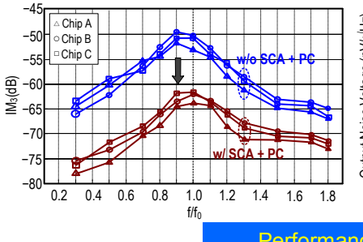
Clock-Defined Bandwidth



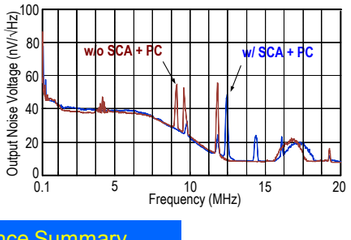
Bandwidth Accuracy



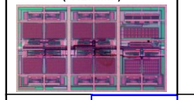
IM3

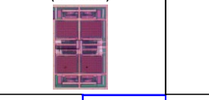


Output Noise



Performance Summary





		5th-Order Lowpass Filter (0.127mm²)		Biquad (0.048mm²)		Uniquad (0.032mm²)	
		w/o SCA + PC	w/ SCA + PC	w/o SCA + PC	w/ SCA + PC	w/o SCA + PC	w/ SCA + PC
Power @ 10 MHz Bandwidth	Main OTA	4.2 mW	3.0 mW	1.68mW	1.2mW	0.84mW	0.6mW
	Auxi. OTA	N/A	1.2 mW	N/A	0.48mW	N/A	0.24mW
	CLK Gen.	1.4 mW	1.4 mW	1.0mW *	1.0mW *	1.0mW *	1.0mW *
	Total	5.6 mW	5.6 mW	2.68mW	2.68mW	1.84mW	1.84mW
Cutoff Accuracy @ 10 MHz		82%	97%	94%	98%	97%	99%
In-band IIP3		+15.3 dBm	+23.5 dBm	+17.2 dBm	+26.8 dBm	+21.5 dBm	+32.6 dBm
-1-dB Compression Point		+5.2 dBm	+7.9 dBm	+6.4 dBm	+9.4 dBm	+7.4 dBm	+11.5 dBm
IRN		35 nV/√Hz	35 nV/√Hz	30 nV/√Hz	30 nV/√Hz	21.4 nV/√Hz	21.4 nV/√Hz

*: Uniquad and Biquad share the same clock generator

Two circuit techniques, SCA and PC, have been proposed for improving the speed and linearity of active-SC LPFs without penalizing the power. Both are carefully designed to assist the main OTA to deliver most of the charge to the integration and load capacitors. Only one auxiliary OTA is entailed for implementing both SCA and PC paths. Three SC LPFs (Uniquad, Biquad and 5th-order Butterworth) were designed and fabricated in 65-nm CMOS for verification. Both circuit techniques are applicable to other SC circuits like analog-to-digital converters.