A 10.4-ENOB 120MS/s SAR ADC with DAC Linearity Calibration in 90nm CMOS

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Abstract - **This paper proposes a DAC linearity calibration and a phase-splitting bit register for a SAR ADC. The calibration corrects the conversion nonlinearity of the bridge DAC structure in the digital domain leading to higher accuracy and insensitivity to comparison offset. Moreover, a phase-splitting bit register is presented to optimize the speed of the digital circuitry. Measurements obtained from a 90nm CMOS prototype operating at 120MS/s and 1.2V supply achieve a SNDR of 64.3dB with 3.2mW power dissipation.**

I. INTRODUCTION

The conversion linearity of a SAR ADC relies basically on the capacitive DAC that samples the input signal and subtracts the reference voltage for subsequent comparisons. Binary-weighted [1]-[2] and bridge structures [3] are two conventional DAC structures used in SAR ADCs. The total capacitance of a binary DAC is usually above the value that is required by kT/C noise, especially for high resolution, because the desired matching of the unit capacitor dominates. The bridge structure leads to much larger units with reduced total capacitance. The capacitor matching is better, although it suffers even more serious nonlinearity caused by the mismatch of the non-unit attenuation capacitor, as well as the top-plate parasitic of the DAC array. Since the nonlinearity is caused by the metal capacitor, which is static and insensitive to temperature variation, it can be calibrated in the foreground [3]. However, the existing solution [3] is sensitive to the comparator offset, which needs to be suppressed within 1/2 LSB before performing the linearity calibration. The offset calibration, which is not required in conventional SAR ADCs, becomes a design limitation when targeting higher resolution.

This paper presents a SAR ADC that achieves, as design goals, both high conversion resolution and speed. Two circuit techniques are proposed to improve the conversion linearity, speed and robustness of the digital circuitry. A bridge structure DAC built with MOM capacitor is used, of which the conversion nonlinearity is estimated and corrected in the digital domain through the proposed linearity calibration. To optimize the speed of the feedback loop a phase-splitting bit register is used in the SA-controller, which simplifies the circuitry and routing of the main signal path. The experimental results of a 90nm CMOS prototype verify the effectiveness of the linearity calibration with state-of-the-art results in terms of high resolution and conversion speed.

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II. ADC ARCHITECTURE

The ADC architecture is shown in Fig.1, which is a conventional SAR ADC mainly consisting of a bridge-DAC, a comparator, a SA controller and the internal clock generator. The SAR logic controls the DAC by utilizing a V_{cm}-based switching [4]. The sampling frequency of the ADC is 120MS/s and the sampling takes 1ns. There is a total 12 comparison cycles for one conversion. A switching detector [5] is embedded in the SA internal time loop. Each bit cycling runs asynchronously according to the time consumed with the comparison and the logic processing. When conversion is completed the digital code enters the calibration engine to correct the conversion error, leading to the final digital output.

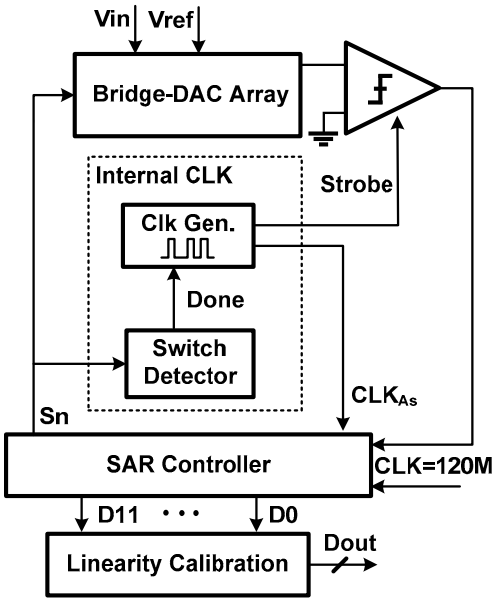

Fig.1: Overall ADC architecture.

III. PROPOSED LINEARITY CALIBRATION

The bridge-DAC structure is very sensitive to the mismatch of the attenuation capacitor and top-plate parasitic capacitance, which degrades the conversion linearity [3]. As shown in Fig.2 a 4-bit (2b MSB array + 2b LSB array) example of a bridge-DAC, with a 20% top-plate parasitic capacitance C_{PB} of the LSB array is considered, and DAC is otherwise ideal. The least significant bits of the MSB array and LSB arrays are B3 and B1, respectively. Ideally, the ratio between two outputs $V_{out}(0100)$ and $V_{out}(0001)$ is 4:1. As there is C_{PB}, the ratio increases to 4.6:1. This ratio

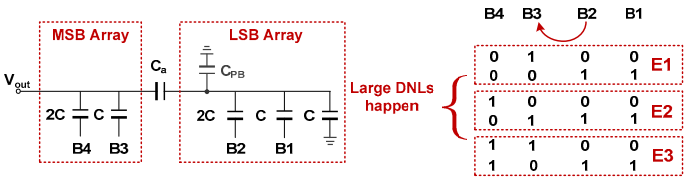

Fig.2: A 4-bit bridge-DAC and the transitions where large DNLs occur.

mismatch causes periodical large DNLs at 3 pairs of two adjacent inputs E1, E2 and E3 as listed in Fig.2. Each contains the carry from the LSB array to the MSB array (B2 to B3). The corresponding DAC outputs versus its digital inputs are plotted in Fig.3. At 3 transitions of E1,E2 and E3 the DNL is 1.6LSB. To compensate the nonlinearity the step size of the LSB should be increased simultaneously, which can be achieved by enlarging the ratio α of C_a according to

$$\alpha = 1 + \frac{C_{PB}}{C_{sum,LSB}} \tag{1}$$

where $C_{sum,LSB}$ is the total capacitance in the LSB array. Since C_{PB} is assumed as 20% of $C_{sum,LSB}$, the ratio α should be 1.2. Fig. 4 illustrates the percentages of the top-parasitic capacitance corresponding to their ratio α for the compensation. However, in practice it is difficult to guarantee the compensation accuracy of C_a, because of the process variation value of the C_{PB} and mismatch of non-unit capacitance of Ca.

The proposed calibration is not dependent on the accuracy of C_a, which is initially designed to be large enough to cover the variation of C_{PB}. According to Fig.4, if the ratio α further increases

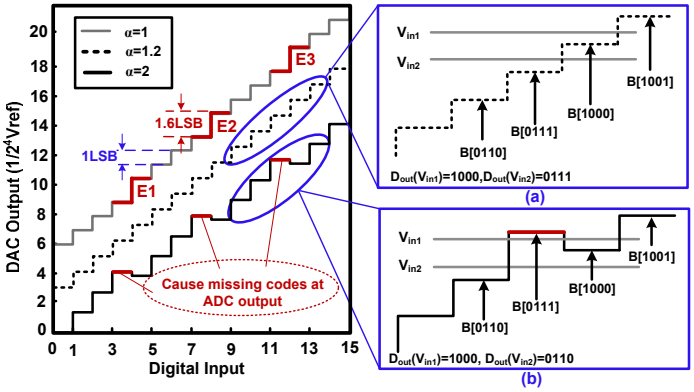

Fig.3: The output characteristic of the DAC in Fig.2 with different ratio α of C_a. For clarification, offsets are added to the cases, where α equal to 1 and 1.2.

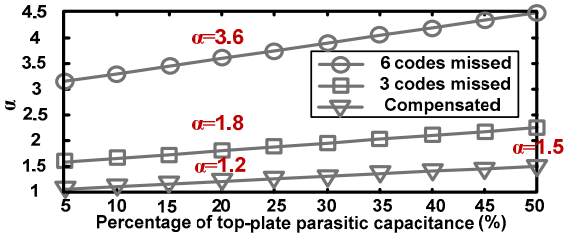

Fig.4: Parasitic capacitance versus the ratio α of C_a

to 1.5, it can cover the compensation range of 0-50% parasitic capacitance. Assuming the 4b bridge-DAC built with α between 1.8 to 3.6 contains 20 % parasitic capacitance after the fabrication, the nonlinearities of the DAC cause 3 missing codes at the digital outputs of the ADC. The effect can be explained by an example shown in Fig. 3 with α of 2. The output voltages of the DAC, at 3 digital inputs in red, exceed the value of their right adjacent inputs. As seen in Fig.3(a) and Fig.3(b), two sampled input signals V_{in1} and V_{in2} are converted to the digital codes D_{out} through different bridge-DACs, which are built with α of 2 and 1.2, respectively: 1) When $V_{in1}>V_{out}(1000)$, according to the switching sequence, the MSB B_4 of D_{out} is determined by comparing the value of V_{in1} with $V_{out}(1000)$, which is set as "1" due to $V_{in1}>V_{out}(1000)$. Then, the 3b remaining (B_3 to B_1) are compared in sequence with $V_{out}(1100)$, $V_{out}(1010)$ and $V_{out}(1001)$, respectively. As V_{in1} is within $V_{out}(1000)$ and $V_{out}(1001)$ in both cases, the final digital outputs are the same code of "1000"; 2) When $V_{out}(0111)<V_{in2}<V_{out}(1000)$, similarly to the previous comparison procedure, V_{in2} is resolved by the comparisons with $V_{out}(1000)$, $V_{out}(0100)$, $V_{out}(0110)$, $V_{out}(0111)$, respectively. The first 3b (B_4-B_2) digital output in both cases are "011", while the results of B_1 are different. In Fig.3(a), as $V_{in2}>V_{out}(0111)$, B_1 is set as "1" (The digital output $D_{out}(V_{in2})$ is "0111"). In Fig. 3(b), the nonlinearity causes $V_{out}(0111)>V_{out}(1000)$, which results in $V_{in2}<V_{out}(0111)$. Accordingly, B_1 is set as "0", and the digital output is "0110". It can be found that in Fig. 3(b) the digital output "0111" is missed with either of the input signals. The conversion characteristics of the ADC with α of 2 and a ramp input signal is plotted in Fig. 5. As expected three digital codes are missed due to the nonlinearities in DAC.

The proposed calibration corrects the conversion nonlinearities in the digital domain, through the multiplication of all the bits in LSB array by a gain factor β :

$$D_{out,cal}[B_4...B_1] = 2^3 B_4 + 2^2 B_3 + \beta(2B_2 + B_1). \tag{2}$$

The calibrated outputs can be found in Fig. 5, the step of the LSB is multiplied by a gain ratio β to best fit the interval of LSB_{MA}, where β can be obtained as

$$\beta = \frac{LSB_{MA,id}}{LSB_{MA,err}}. \tag{3}$$

The $LSB_{MA,id}$ is the ideal least significant bit of the MSB array, which represents the step sum in one interval of LSB_{MA}, and $LSB_{MA,err}$ is the actual step sum of the ADC. The calibration corrects the conversion nonlinearities in digital domain by shifting the missing codes to upper boundary of the digital outputs as seen in Fig.5. The solution sacrifices a little bit output range of the

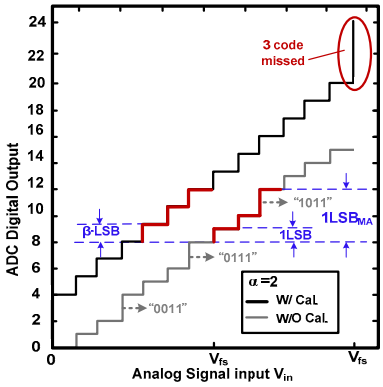

Fig.5: The output characteristic of the ADC with and without the proposed linearity calibration.

full-scale, but effectively compensating the conversion nonlinearities. The missed range can be minimized by properly designing the ratio α of C_a well below the value that causes more missing codes. As shown in Fig.4, e.g. if 20% parasitic capacitance is extracted after the layout routing, the ratio α should be set between 1.2 and 3.6.

The proposed calibration is verified in a 12b SAR ADC, which is implemented with a bridge-DAC array shown in Fig. 6. The V_{cm}-based switching [4] is used that can reduce 1 bit in the DAC. The output equivalent capacitance of the bridge-DAC is only 64C, and the unit capacitance is 20fF, which results in a total sampling capacitance of 1.28pF. According to layout extraction tools the top-plate parasitic capacitance is around 3% of the LSB array.

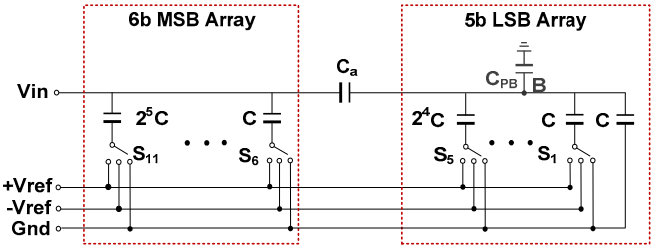

Fig.6: 11-bit Bridge-DAC array.

Thus, the attenuator C_a is implemented with 25Ff (Ideal vale should be 20.6fF, α=25/20.6=1.2) that guarantees the calibration to cover a 0 to 20% top-plate parasitic capacitance. The gain factor β is applied to the digital output from B_6 to B_1, because the nonlinearities occur at carry from B_6 to B_7. The $LSB_{MA,id}$ is 64, while the $LSB_{MA,err}$ is estimated via codes histogram statistic. Since the nonlinearity has a periodical interval of 64 outputs, the range for statistic is set as 64 from D_{out} [2100] to D_{out}[2163]. There is a total number of 1280 codes within the range that are collected for the gain estimation. Thus, the average number N_{avg} of each D_{out} is 20. The calibration compares the number of each output $N(D_{out})$ with the one half average value $N_{avg}/2$, which is defined as a threshold of error output. If $N(D_{out}) \geq N_{avg}/2$, the D_{out} is counted as 1LSB. If $0 \leq N(D_{out}) < N_{avg}/2$, the D_{out} is counted as $(N(D_{out})/N_{avg})$LSB. When the comparisons are completed, $LSB_{MA,err}$ is obtained by summing the 64 counts of LSBs. Therefore, the gain factor β finally acquired by eq.(3) is multiplied to all the 6 bits of each output. The gain estimation is based on the statistic of the consecutive 64 outputs, which is input dependent. The collection range is not specified. In this design the outputs at middle are selected, which are more equally distributed with a sinusoidal input. In addition, the number of 1280 outputs is sufficient for statistic, as the calibration can run repeatedly to approximate to the desired gain factor β at background.

IV. Proposed Phase-Splitting Bit Register

Once the comparator makes the decision, as shown in Fig. 7(a), it first goes through the latch to prevent the glitch and subsequently to a series of buffers to drive the bit register afterwards. Fig.7(a) shows a dynamic bit register [4] composed by 12 units of BR to save the corresponding decision of each bit from the comparator output (Comp_out). Each unit contains only 4 transistors with a simple logic function to cope for higher speed. According to the switching nature both outputs of the comparator are used, where the complementary decision of Comp_out is also applied to the other similar 12 units, which is not shown here. In the beginning, the outputs of bit register B1 to B12 and node A1 are pre-charged to "1" by signal Rst1. Then, the transistor M13 stays on until B1 is properly set according to Comp_out. It would be important to highlight that the nodes A2 to A12 will be discharged simultaneously, if the Comp_out is high. Consequently, before the next bit comparison node A2 needs to be pre-charged by the complementary signal of L1. The operation repeats 11 cycles until the conversion is completed. As mentioned before, the Comp_out drives a series of units BR, and due to high-speed concerns the size of M1 to M12 cannot be minimized. Therefore, a large buffer is required. In a low resolution SAR the propagation delay of the buffers is negligible, while in high resolution the buffer needs to drive larger gate capacitance and routing parasitic due to increased number of BR.

To optimize the loop delay a phase-splitting solution is proposed as shown in Fig. 7(b). The bit register in Fig. 7(a) is separated into two time-interleaved registers, of which every 6 odd (BR1, BR3…BR11) or even (BR2, BR4…BR12) units share a common NMOS transistor (M14 or M15) that is connected to Comp_out. The one in the left works in every odd phase and resets the node B1 high via M16 in every even phase, and vice versa for

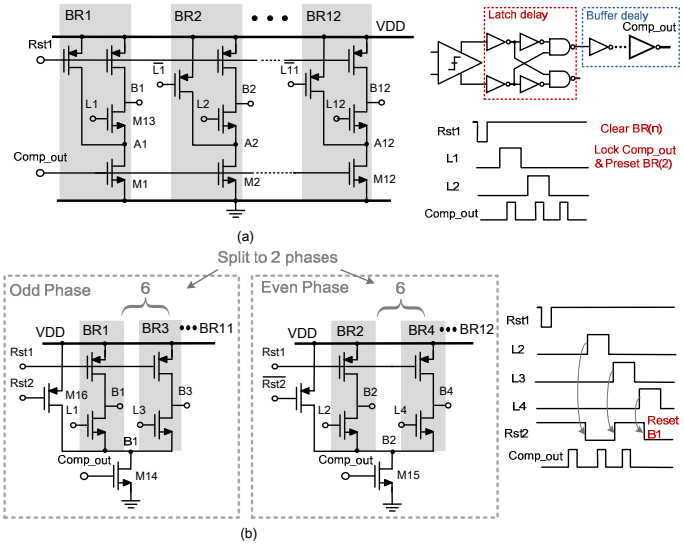

Fig.7: (a) The conventional bit register and comparator output logic. (b) The proposed phase-split bit register.

its right counterpart. The phase-splitting solution requires extra signal generation of Rst2, which is triggered by every rising edge of L2 to L12. Since the circuit is not implemented in the main signal path, it will not affect the speed of the register.

V. Measurement Results

The proposed SAR ADC was implemented in 1P9M 90nm CMOS process with metal-oxide-metal (MOM) capacitor. Fig.8(a) shows the die photograph; the active area is 0.042mm^2. Fig.8(b) illustrates the measured performance of total available 16 chips at a low input frequency (693kHz) with a 120MS/s sampling rate. The average SNDRs before and after linearity calibration are 62.6dB and 64.3dB, respectively. The thermal noise of the comparator and the switching noise limit the performance of ADC at low input frequency. Fig. 9 shows the measured FFT plotted @Nyquist input frequency (59.7MHz) with a SNDR of 61.2dB. At high input the 3rd harmonic distortion dominates, because the sampling nonlinearity is relatively high under a rail-to-rail signal input. Fig.10 shows the measured dynamic performances before and after calibration. Fig.11 shows the measured static performance. The proposed calibration improves DNL from 0.65/-1LSB to 0.6/-0.63LSB and the INL from 1.95/-2.5LSB to 1.9/-1.3LSB. The linearity calibration is implemented off-chip. Table I summarizes and compares the overall measured performance with state-of-the-art SAR ADCs. The total power consumption is 3.2mW, at 120MS/s from 1.2V supply, where the analog and digital blocks consume 0.8mW and 2.4mW, respectively. This work exhibits an excellent FoM of 28fJ/conv.-step for the high-resolution and speed that is obtained.

VI. Conclusions

A linearity calibration and a phase-splitting bit register for a SAR ADC have been presented. The calibration effectively estimates and corrects the conversion nonlinearities in digital domain, which obtains high accuracy with simple calibration algorithm. The phase-splitting bit register optimizes the loop delay and speeds up the conversion. The measured results demonstrate the effectiveness of the proposed methods for a combined design target of high-speed and high-resolution.

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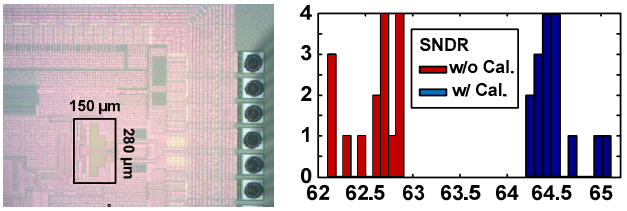
Table I Summary of performance and comparisons

	[1] ISSCC' 10	[3] CICC' 12	[6] VLSI' 10	This work
Architecture	SAR	SAR	Zero-crossing	SAR
Technology (nm)	130	90	90	90
Resolution (bit)	12	12	12	12
Sampling Rate (MS/s)	45	50	100	120
Supply Voltage (V)	1.2	1.2	1.2	1.2
Input Swing (V_{P-P})	2.4	2.4	2	2
SNDR (dB)	68.3	66.5	65	64.3
Area (mm^2)	0.059	0.046	0.32	0.042
Power (mW)	2.8	3.3	6.2	3.2
FOM=Power/$2^{ENOB@DC}$*f_s (fJ/conv-step)	30	38	43	20
FOM=Power/$2^{ENOB@Nyq.}$*f_s (fJ/conv-step)	36	45	53	28
Calibration	Off-chip	Off-chip	Off-chip	Off-chip



(a) (b)

Fig.8: (a) Die microphotograph of the ADC, (b) Measured SNDR of total available 16 chips w/o and w/ proposed calibration.

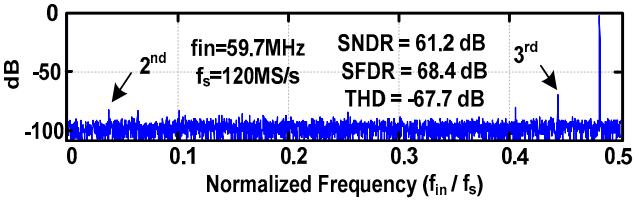


Fig.9: Measured FFT of the digital output (decimated by25)

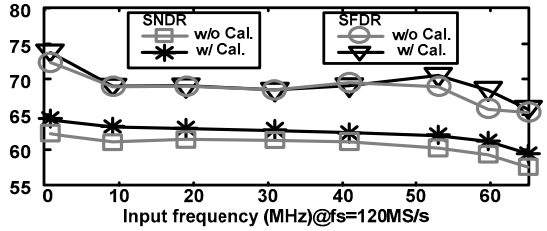


Fig.10: Measured dynamic performances w/o & w/ calibration.

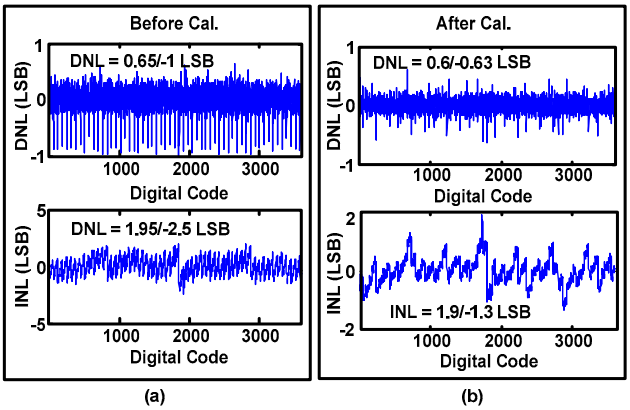


Fig.11: Measured static performance w/o & w/ calibration.