A Wideband Multi-Stage Inverter-Based Driver Amplifier for IEEE 802.22 WRAN Transmitters

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Abstract

This paper proposes a wideband multi-stage inverter-based driver amplifier (DA) suitable for IEEE 802.22 wireless regional area network (WRAN) transmitters. In order to optimize the voltage gain, power, linearity and load drivability, the DA employs two cascaded inverters followed by a source follower, in which the second inverter employs resistive feedback and an inverter-based active load to achieve linearization. Simulated in 65 nm CMOS, the achieved voltage gain is 17.6 dB and the power is 14.6 mW at 1.2 V. The –3 dB bandwidth is 5.6 MHz to 2.17 GHz. For a 3rd-order intermodulation distortion (IMD3) of –45 dBc, the output power reaches –7.3 dBm.

Keywords

WRAN transmitters, wideband, inverter-based, DA, linearity, IMD3, and sweet spot.

1. Introduction

High-performance wideband RF circuits are of great importance for emerging wireless protocols, e.g., the IEEE 802.22 wireless regional area network (WRAN). It employs the cognitive radio [1] technique to enable communications flexibly over a wide spectrum covering 54 to 862 MHz, which is overlapped with the common TV bands. Yet, wideband transmitters with a high spectral purity are challenging, complicating the design tradeoffs between gain, power and linearity.

In this paper, a wideband multi-stage inverter-based driver amplifier (DA) with proper resistive feedback and distortion cancellation techniques is proposed. With just 14.6 mW of power, the DA achieves a high voltage gain (17.6 dB) and an excellent IMD3 (–45 dBc) at an output power of –7.3 dBm.

2. Proposed wideband DA

The schematic of the proposed DA is depicted in **Figure 1**. There are three stages in cascade to ease the gain and linearity optimization. The first stage (M_{N1}, M_{P1}) is an inverter with a big feedback resistor (R_{BIG}) for the bias purpose, contributing most of the gain. The second stage is another inverter (M_{N2}, M_{P2}), but with a downsized feedback resistor (R_{F2}) to boost the linearity effectively via negative feedback. For an inter-stage DA, the third stage is a source follower (SF) (M_{SF1}, M_{SF2}) to drive the power amplifier (PA), which can pose a very big input capacitance (C_L). This cascaded topology allows a high voltage gain with low power due to the high g_m/I_d ratio of inverter and proper distribution of voltage gain. To further enhance the linearity, an inverter-based active load (M_{NC}, M_{PC}) [2] is employed for the second inverter, by which the non-linearity can be further enhanced at a small expense of power. The DC blocking capacitors (C_1, C_2) essentially minimize the performance variations of the DA against process, voltage and temperature (PVT) variations. To reject the even-order harmonic distortion, the DA can be duplicated to allow differential operation. For the odd-order harmonic distortion, we focus on the third-order term to simplify the circuit analysis.

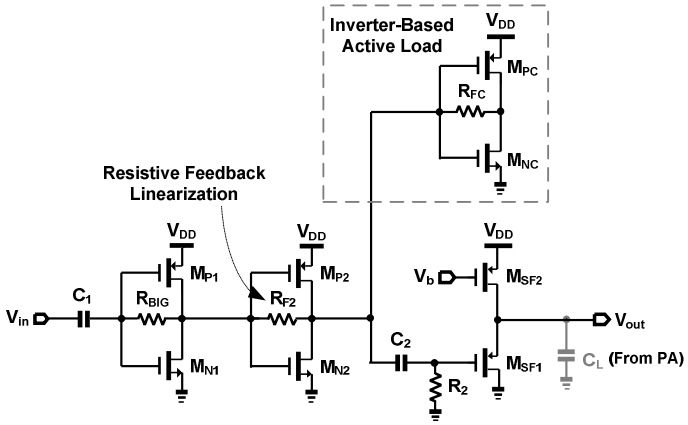

Figure 1: Schematic of the proposed DA.

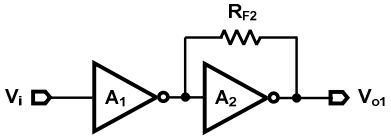

Figure 2: Cascade of two inverters with proper resistive feedback in the second one.

The use of negative feedback can linearize a circuit at the expense of gain. Thus, to balance the gain with linearity, the resistive feedback can be applied to the second inverter only. For a typical single-stage amplifier, the input-referred third-order intercept point (IIP3) without (A_{IIP3}) and with ($A_{\text{IIP3,f}}$) feedback is given by [3],

$$A_{\text{IIP3}} = \sqrt{4a_1/3a_3}\,, \tag{1}$$

$$\text{and } A_{\text{IIP3,f}} = \sqrt{4a_1(1+T)^3/3a_3}\,, \tag{2}$$

where the terms a_1 and a_3 are the fundamental and third-order coefficients of the input-output (v-v) characteristic, respectively, and T is the loop gain created by the feedback. Accordingly, the total IIP3 ($A_{\text{IIP3t,f}}$) of the two cascaded inverters in **Figure 2** can be calculated,

$$\frac{1}{A_{\text{IIP3t,f}}^2} = \frac{1}{A_{\text{IIP3,1}}^2} + \frac{1}{A_{\text{IIP3,2}}^2}\frac{a_1^2}{(1+T_2)^3}. \tag{3}$$

It clearly shows that the loop gain T_2, controlled by the size of R_{F2}, can be used to enhance $A_{\text{IIP3,2}}$, so as the $A_{\text{IIP3t,f}}$.

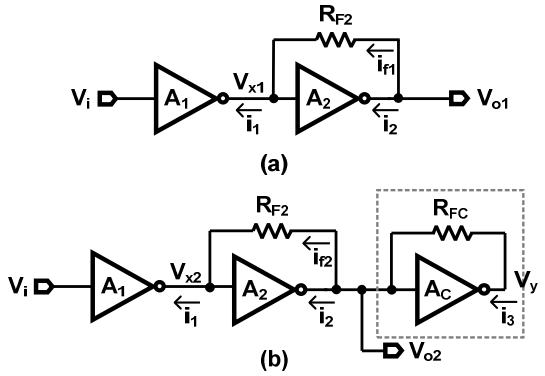

Figure 3: Cascade of two inverters (a) with resistive feedback on the second stage for linearization; (b) with resistive feedback and inverter-based active load on the second stage for better linearization.

3. Inverter-based active load for distortion cancellation

With proper sizing, the inverter-based active load can be used to cancel the third-order nonlinearity within some input power levels (i.e., a sweet spot in the IMD3 plot). To describe its basic principle, the output voltages with and without compensation by such an active load are compared, through both small- and large-signal analysis. For the former, to simplify the calculation, only the third-order nonlinear terms are considered. Moreover, we also define $g_m = g_{mn} + g_{mp}$.

3.1. Small-Signal Analysis of non-Compensated DA

As shown in **Figure 3(a)**, we can express the node voltages v_{x1} and v_{o1} using the Taylor series,

$$v_{x1} = A_1 v_i + A_3 v_i^3, \tag{4a}$$
$$v_{o1} = B_1 v_i + B_3 v_i^3, \tag{4b}$$

where A_1, B_1, A_3 and B_3 represent the first- and third-order coefficients of v_{x1} and v_{o1}, respectively. The showed currents i_1 and i_2 are given by

$$i_1 = g_{mx1} v_i + g_{mx3} v_i^3, \tag{5a}$$
$$i_2 = g_{mo1} v_{x1} + g_{mo3} v_{x1}^3, \tag{5b}$$

where g_{mx1} and g_{mo1} are the first-order terms of the first stage's and second stage's transconductances (see **Figure 1**), respectively; g_{mx3} and g_{mo3} are the third-order nonlinear terms. The drain-source effects are ignored.

Neglecting the gate current, $i_1 = -i_2$ can be obtained. (6) is deduced by putting (4a) into (5b), and connecting with (5a),

$$g_{mx1} v_i + g_{mx3} v_i^3 = -(g_{mo1} A_1) v_i - (g_{mo1} A_3 + g_{mo3} A_1^3) v_i^3. \tag{6}$$

With (6), the terms A_1 and A_3 of v_{x1} can be solved, based on the coefficients' mapping relationship. In addition, the relationship between v_{o1} and v_{x1} is built,

$$i_{f1} = i_1 = (v_{o1} - v_{x1})/R_{F2}. \tag{7}$$

Another relationship is obtained via substituting (4) and (5a) into (7),

$$B_1 v_i + B_3 v_i^3 = (g_{mx1} R_{F2} + A_1) v_i + (g_{mx3} R_{F2} + A_3) v_i^3. \tag{8}$$

Consequently, combining (6) and (8), the coefficients of the v-v characteristic of non-compensated DA are computed,

$$B_1 = \frac{g_{mx1}(g_{mo1} R_{F2} - 1)}{g_{mo1}}, \tag{9}$$
$$B_3 = \frac{g_{mo3} g_{mx1}^3 + g_{mx3} g_{mo1}^3 (g_{mo1} R_{F2} - 1)}{g_{mo1}^4}. \tag{10}$$

3.2. Small-Signal Analysis of Compensated DA

With the inverter-based active load [**Figure 3(b)**], the current i_3 can be expressed as

$$i_3 = g_{my1} v_{o2} + g_{my3} v_{o2}^3, \tag{11}$$

where g_{my1} and g_{my3} represent the first- and third-order terms of transconductances of the inverter-based active load. The currents i_1 and i_2 still follow (5a) and (5b). The node voltages v_{x2} and v_{o2} are expressed as

$$v_{x2} = C_1 v_i + C_3 v_i^3, \tag{12a}$$
$$v_{o2} = D_1 v_i + D_3 v_i^3, \tag{12b}$$

where C_1, D_1, and C_3, D_3 represent the first- and third-order coefficients of v_{x2} and v_{o2}, respectively. Similarly, i_{f2} can be calculated as

$$i_{f2} = i_1 = -(i_2 + i_3) = (v_{o2} - v_{x2})/R_{F2}. \tag{13}$$

Using the same method of coefficients' mapping, we obtain D_1 and D_3,

$$D_1 = \frac{g_{mx1}(g_{mo1} R_{F2} - 1)}{g_{mo1} + g_{my1}}, \tag{14}$$
$$D_3 \approx \frac{g_{mo3} g_{mx1}^3 + g_{mx3} g_{mo1}^3 (g_{mo1} R_{F2} - 1)}{(g_{mo1} + g_{my1})^4}. \tag{15}$$

The linearity improvement can be assessed by comparing the relationship of coefficients B_1, D_1, B_3 and D_3. To this end, if the proposed DA has a better linearity, $|B_1/D_1|$ should be smaller than $|B_3/D_3|$. After some calculations, the condition is expressed as

$$\left|\frac{B_1}{D_1}\right| = \left|1 + \frac{g_{my1}}{g_{mo1}}\right| < \left|1 + \frac{g_{my1}}{g_{mo1}}\right|^4 = \left|\frac{B_3}{D_3}\right|. \tag{16}$$

Since g_{my1} and g_{mo1} are positive, (16) is easy to be proved. It also shows that a bigger g_{my1} can lead to better linearity.

3.3. Large-Signal Analysis

To understand better the advantages and limitations of such an active-load compensation technique, the large-signal analysis was conducted as well. We analyze the coefficients of the IMD terms. In the two-tone test, considering up to the fifth-order's effect, the coefficients are

$$\text{1st: } a_1 A + \frac{9}{4} a_3 A^3 + \frac{25}{4} a_5 A^5, \tag{17a}$$

$$\text{IMD3:}\quad \frac{3}{4}a_3A^3+\frac{25}{8}a_5A^5, \tag{17b}$$

$$\text{IMD5:}\quad \frac{5}{8}a_5A^5, \tag{17c}$$

where A is the amplitude; a_1, a_3, and a_5 are the first-, third- and fifth-order coefficients of the v-v relation. In (17), the lower-order terms are affected by the higher-order terms. For example, the first-order term is affected by both the third- and fifth-order terms. If the input power goes up, the effect of higher order terms gets larger, leading to the sweet spot. Referred to [4], the sweet spots for the higher-order IMD terms will shift to higher power level accordingly.

Essentially, for the non-compensated DA, according to (17b) there should be a sweet spot on IMD3 curve with the input power, which is mainly affected by the fifth-order term. Whereas for the compensated DA, when the input power increases to a certain level, the amplified third-order term passes back through R_{FC} to cancel the original third-order term at node v_{o2} in **Figure 3(b)**, which results in a sweet spot on the IMD3 curve in a lower power level. If the input power is increased further, the fifth-order's effect will get severe then, yielding another sweet spot for higher power level due to the effects of both third- and fifth-order terms. For higher-order IMD curves, e.g., fifth- and seventh-order, the same principle applies.

4. Simulation results

The proposed DA with single-ended implementation was designed in 65 nm CMOS with a 1.2 V supply. In simulations, it shows a voltage gain of 17.6 dB and the power consumption is 14.6 mW, of which 0.5 mW is due to the inverter-based active load. With a load capacitor of 3 pF, the –3 dB bandwidth covers 5.6 MHz to 2.17 GHz.

The linearity simulations are based on the two-tone test with the center frequency set at 500 MHz, and the tone offset frequency is 5 MHz. As shown in **Figure 4**, the proposed DA is better linearized when comparing with the non-compensated DA. To provide an output power of –7.3 dBm (refer to 50 Ω), the IMD3 of the proposed DA is –45 dBc, improved by 5 dB compared with the non-compensated DA, though the linear gain is reduced by around 2.4 dB. It is inappropriate to compute the IIP3 due to the sweet spot of the proposed DA in Fig. 4, but in the region that the input power varies from –40 to –33 dBm, it is reasonable to estimate the IIP3 of the proposed DA as 0 dBm, which is 5.6 dB better than that of the non-compensated DA. Additionally, the sweet spot analysis in large-signal operation is presented in **Figure 5**. For the proposed DA, there are two sweet spots on the IMD3 curve along a range of input power as expected, and the positions of the sweet spots depend on the transconductance and R_{FC} of the inverter-based active load.

In most cases, the spectrum purity of a circuit considers both the linearity and noise, and the related measure is the intermodulation free dynamic range ($IMFDR_3$) [3]. For the proposed DA, the circuit noise power is only –132 dBm, which should be much lower than that contributed by the front-end digital-to-analog converter (DAC). Supposing a 12-bit DAC, its noise floor should be –81.3 dBm/Hz (**Figure 5**),

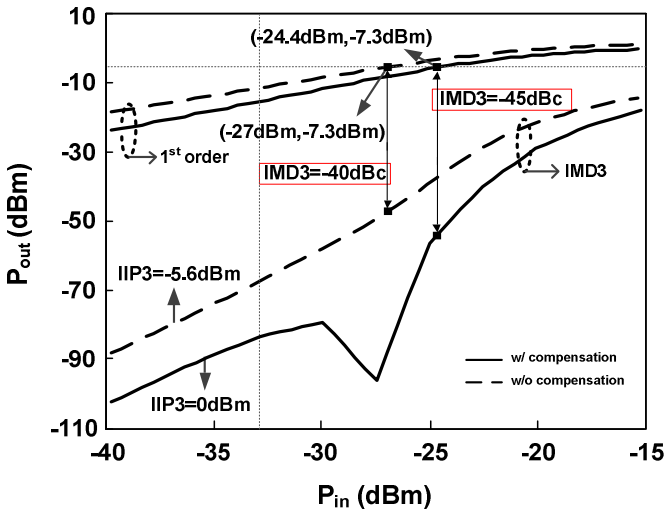

Figure 4: Simulated linearity metrics of both the compensated (proposed) and non-compensated DAs in terms of IMD3.

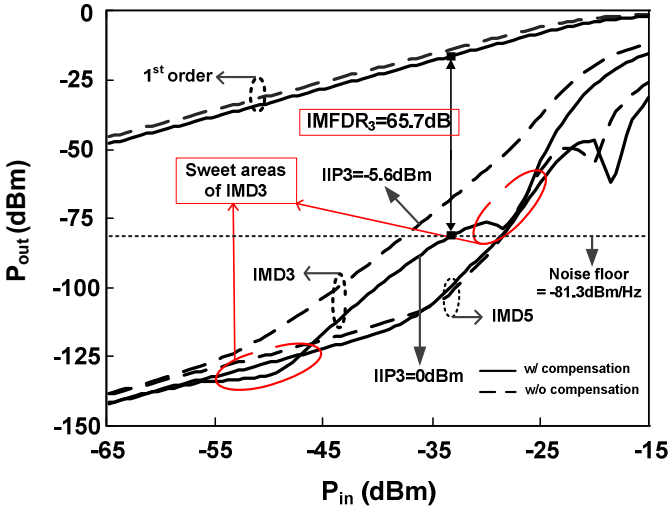

Figure 5: The linearity metrics under a wide input range in terms of IMD3 and IMD5.

referred to the output power at –7.3 dBm. Thus, the $IMFDR_3$ of the proposed DA should be 65.7 dB.

For the effects of PVT, the performances are shown in **Figure 6**. The results are compared to the values in typical conditions (TT, 1.2 V, and 27 ^{o}C) at an output power of –7.3 dBm with an IMD3 of –45 dBc. **Figure 6(a)** presents the effect of the process corners (FF, SS, FS, and SF) on linearity, in which although the SS corner has a disruptive effect on the sweet spot, it does not impact the IMD3. In **Figure 6(b)**, given the supply voltage changes from 1.1 to 1.3 V, the linearity is impacted mainly by the lower one. **Figure 6(c)** shows the results under temperature of –30 to 100^{o}C, and the IMD3 is relatively stable.

5. Conclusion

This paper described a wideband multi-stage inverter-based DA with optimized gain and linearity suitable for an IEEE 802.22 WRAN transmitter with an integrated PA. The

DA is built via cascading two power-efficient inverters, and followed by a SF to maintain a high load drivability. Resistive feedback and an inverter-based active load are exploited concurrently to linearize the second inverter, which dominates the nonlinearity. As analyzed, such an active load can generate two sweet spots to the IMD3 curve at the expense of only 0.5 mW. Besides, it has been proved that, with proper uses of the DC blocking capacitors, the performances of the DA can be effectively stabilized against PVT variations.

6. Acknowledgement

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7. References

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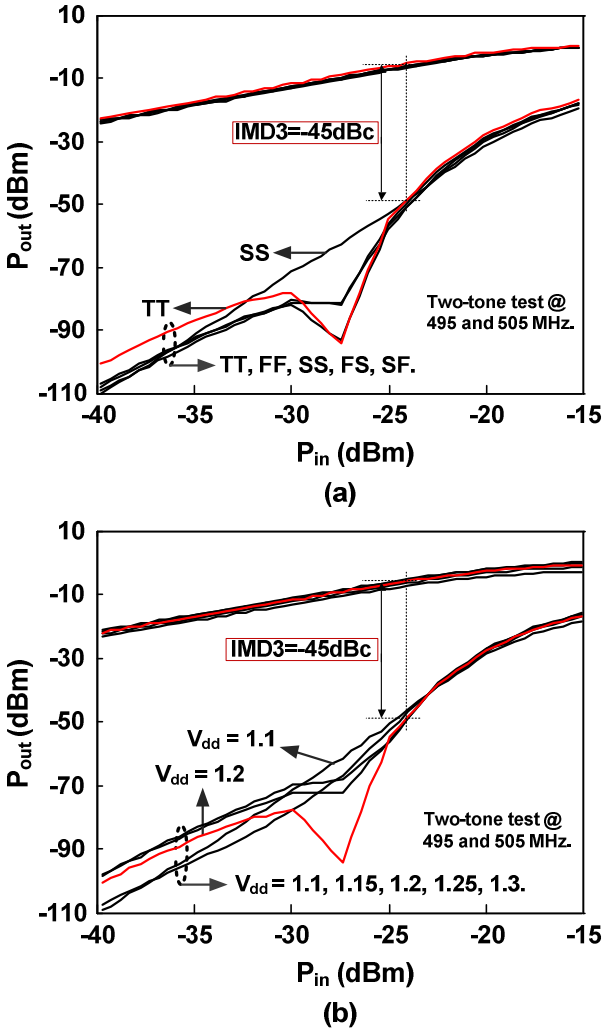

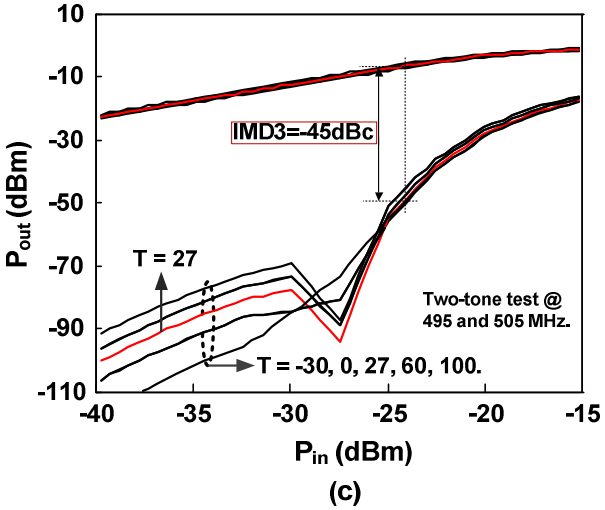

Figure 6: Simulated linearity performances of the proposed DA at different (a) process corners, (b) supply voltages and (c) temperatures.