A Background Gain- Calibration Technique for Low Voltage Pipelined ADCs Based on Nonlinear Interpolation

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Abstract— **In the design of green circuit, the most effective way for low power is to reduce the supply voltage. However, the accuracy of pipelined ADC is limited by the residue amplification. The inaccurate residue amplification is much worse in an ultra-low voltage condition because of the lack of the headroom for transistors in the opamp. This paper describes a new background calibration technique for the pipelined ADCs designed in the ultra-low supply voltage. Based on the Least Mean Square (LMS) algorithm and the digital nonlinear interpolation, the proposed calibration technique corrects the interstage gain error. It is a fully digital approach and only needs very little analog modifications, which increases the design flexibility and reduces the production cycle.**

Keywords: Pipelined ADCS, digital calibration, LMS algorithm, nonlinear interpolation.

I. INTRODUCTION

In the family of Analog to Digital Converters (ADCs), pipelined ADCs, with their high speed and high resolution performances, are very popular in many modern systems. Making the pipelined ADCs low power matches the green-circuit design concept and becomes a hot research topic. Lowering down the supply voltage is one of the efficient ways to reduce the power consumption. In pipelined ADCs, the conversion accuracy is highly related to the precision of the residue amplification. In ultra-low supply voltage condition, the operational amplifier can hardly achieve the required gain because the voltage headroom is not enough for each stacked transistor. The low-gain opamp introduces large interstage gain error, which distorts the output of the pipelined ADCs. Recently, digital calibration techniques are proved to be able to reduce this error successfully [1]-[11]. Based on adaptive signal processing theory, digital calibration techniques first measure the interstage gain error and compensate it by post processing the output code. Besides of the accuracy improvement, digital calibration technique also benefits its low cost. With the CMOS process shrinking rapidly digital circuits become highly integrated and very efficient. It is preferred that the design focus is moved from highly power-hungry analog part to low cost digital part. To maximize the impact of the digital calibration technique, it is preferred not to modify the analog circuit too much when digital calibration technique is applied. The less the analog circuit modification is, the less the additional power and design effort is. In addition, keeping the analog circuit almost the same speeds up the design and production cycle, this also cuts down the cost. The paper presents a digital background calibration technique which compensates the interstage gain error in pipelined ADCs. The proposed technique creates a dummy A/D channel by modifying the ADC transfer curve. Based on nonlinear interpolation, the LMS algorithm is able to find the interstage gain error which is then compensated in digital domain.

II. PIPELINED ADC ARCHITECTURE AND INTERSTAGE GAIN ERROR COMPENSATION

The proposed calibration technique can be applied on the traditional pipelined ADCs, shown in Fig.1. It comprises totally 6 pipeline stages. Each stage contains a sub-ADC, DAC and a residue amplifier. Except the first and last stage, each pipeline stage uses conventional 2.8 bit/stage with the nominal interstage gain of 4. For the first stage, it has two conversion modes, which is designed specific for the proposed calibration technique. The last stage is traditional 3-bit flash ADC, containing 7 comparators. Since each stage outputs 3-bit digital code, 1 bit for redundancy, there are totally 6 stages; the ADC has a resolution of 13-bit. The ADC is defined to have an input range of V_{ref}, which is from $-1/2V_{ref}$ to $1/2V_{ref}$. In the ideal case each stage outputs an analog residue from $-1/4V_{ref}$ to $1/4V_{ref}$, which implies the ADC has an over-range margin of $-1/4V_{ref}$ to $1/4V_{ref}$. The over-range margin is used to accommodate the sub-ADC error and opamp offset.

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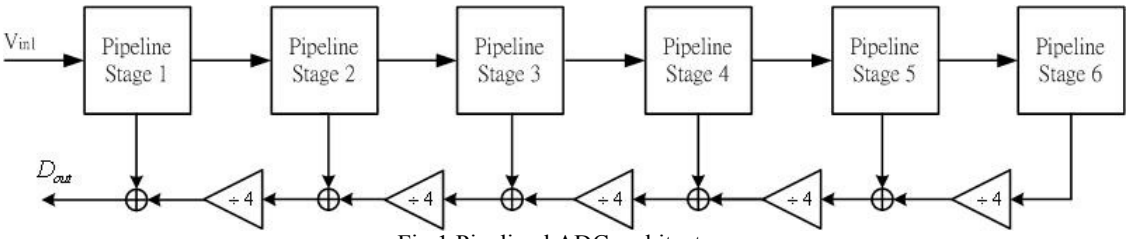

Fig.1 Pipelined ADC architecture

In pipelined ADC, the dominant error is the interstage gain error. To explore its effect, Fig.2 shows a simplified ADC model with the non-ideal effects. For the brevity of the derivate of the formulas, an ideal quantizer is model as [6]

$$D = (\frac{V_{in}}{\Delta} + e_{ADC})\Delta \tag{1}$$

where Δ is the step size of the quantizer, and $e_{ADC}\Delta$ is the normalized quantization error. In Fig.2, the pipelined stages 2~6 are simplified as a single backend ADC, which contributes quantization error of the last stage.

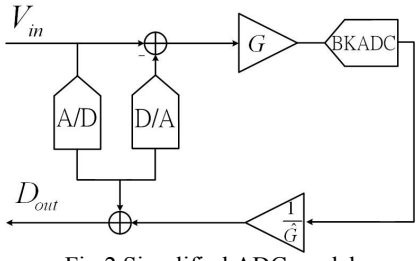

Fig.2 Simplified ADC model

From (1), with considering the interstage gain error, the digital output of the pipelined ADC is represented as

$$\begin{aligned} D_{out} &= D_1 + \frac{1}{\hat{G}} D_{BK} \\ &= (\frac{V_{in}}{\Delta_1} + e_{ADC1})\Delta_1 + \frac{1}{\hat{G}}(\frac{-e_{ADC1}\Delta_1 \cdot G}{\Delta_{BK}} + e_{ADC,BK})\Delta_{BK} \\ &= V_{in} + (1 - \frac{G}{\hat{G}})(e_{ADC1}\Delta_1) + \frac{1}{\hat{G}} e_{ADC,BK}\Delta_{BK} \end{aligned} \tag{2}$$

where $-e_{ADC1}\Delta_1$ is the first stage quantization error, or the residue, G is the nominal interstage gain and $\hat{G}$ is the actual one. In the above equation, it is obvious that if $\hat{G}$ is equal to G, the digital output is the same as input with only the quantization error left. Usually, the digital output of pipelined ADC is the sum of the first stage digital output and the backend digital output D_{BK} divided by G. Any mismatch between G and $\hat{G}$ causes large nonlinearity. Therefore, replacing G with $\hat{G}$ as shown in (2) could remove the interstage gain error. The key job of the calibration technique is to find $\hat{G}$ without much analog modification and interrupting the A/D conversion.

III. Extracting Error Parameters

A. Calibration Concept

LMS algorithm is proved to be an efficient way to find the error parameters both in foreground [7] and background calibration techniques [3]. The basic parameter update formula is

$$\varepsilon(n+1) = \varepsilon(n) + \frac{1}{2} \cdot \mu \cdot e(n) \cdot \nabla(n) \tag{3}$$

Generally, when LMS is applied on the calibration of the pipelined ADC, e(n) represents the difference between the un-calibrated ADC output and the ADC expected output. When e(n) is equal to zero, that means the output of the calibrated ADC equals the expected output hence the errors in the ADC are fully calibrated. As a result, e(n) is parameter to be minimized. However, in reality the expected output is what the ADC converts. Therefore, to get the information of e(n) is the key point of calibration. In the foreground calibration, since the injected test signal is known in advance, e(n) can be obtained easily. However, in the background calibration, the expected value is not known beforehand. Traditionally people use a slow but accurate ADC to get the ideal output. In another way, known as split architecture, a single channel ADC is splitted into two channels, e(n) is defined as the difference between two channels, if and only if the difference is zero, both of the channels are fully calibrated [8], [9]. All the above solutions have a common drawback that they need a lot of additional analog circuit and modifications, which is costly. On contrary, this paper suggests a solution without requiring a reference ADC or splitting the main ADC. Similar in [10], in the proposed method, as shown in Fig.3, the pipelined ADC virtualizes another ADC channel. Although there is only one ADC channel physically, the original ADC and the virtualized ADC allow the use of split architecture calibration concept. The error between them is the minimization parameter which drives the LMS engine to find the interstage gain error. The virtual ADC is realized by modifying the first stage into two residue generation modes, shown in Fig.4. Unlike [10], the proposed method actually implements the two ADCs. Therefore the dynamic range is not reduced because there is no test signal intentionally injected.

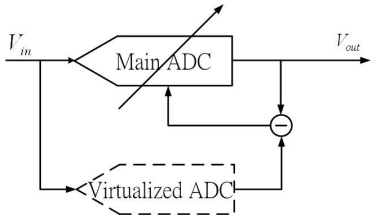

Fig.3 Calibration using virtualized ADC

Comparing the ADC transfer curves, the residue transition points are different. It guarantees that the main ADC differs from the virtual one where LMS algorithm could be applied.

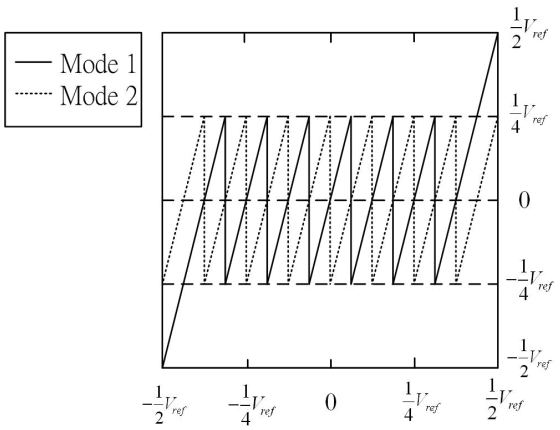

Fig.4 Dual mode residue transfer curve

B. Nonlinear Interpolation

As discussed above, the LMS engine is driven by the difference between the original ADC and virtual ADC. Suppose that at nth sample, the ADC works in mode 2, giving the output according to the virtual ADC. At that sample, if the output of mode 1 ADC could be known, the difference is valid for the calibration. In this proposed technique, the output for mode 1 ADC is estimated by nonlinear interpolation. In signal processing theory, a single missing point in a band limited signal can be interpolated. The interpolation accuracy is determined by the number of adjacent points used. The interpolation is realized by a digital nonlinear interpolation filter [5]. The tap coefficients are

$$C(k) = \frac{n!n!}{(n+k)!(n-k)!}(-1)^{k+1} \tag{4}$$

With the background calibration enabled, the ADC converts N samples in mode 1, and it is switched to mode 2 for one sample, after that it is switched back to mode 1 for N samples. Therefore, the output has the following pattern.

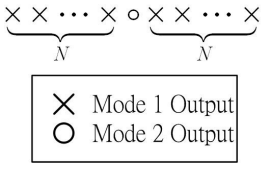

Fig.5 ADC output pattern

When the ADC works in mode 2, the missed point in mode 1 is interpolated. The corresponding difference is sent to LMS engine. To avoid division, the reciprocal of interstage gain is defined as a single parameter β. Applying (3), the update equation can be derived.

$$\beta(n+1) = \beta(n) + \mu_g \cdot e(n) \cdot D_{BK} \tag{5}$$

It is obvious that mode 1 misses one sample every N samples, the period of LMS adaptation is 2N+2 samples. Notice that although the ADC serves as two channels, each channel has the same interstage gain error, the correction parameters can be combined together in a single update equation. For the following stages, the interstage gain error can be compensated in the same way with different gradient parameter D_{BK}.

IV. Circuit Building Block Details

The modified MDAC circuit with dual mode residue curve is shown in Fig.6. In mode 1, six comparators are used to determine 7 levels with the threshold voltages of $\pm 5/16V_{ref}$, $\pm 3/16V_{ref}$, and $\pm 1/16V_{ref}$. In mode 2, 7 comparators are used to determine equally spaced 8 levels with the threshold voltages of $\pm 6/16V_{ref}$, $\pm 4/16V_{ref}$, $\pm 2/16V_{ref}$, and 0. The switching of different mode is performed by selecting different reference voltages of each comparator. In the modification of the MDAC, two capacitors are added to provide one extra level. In the absence of circuit non-idealities, the output of the MDAC is given by

$$V_{out} = V_{in}\frac{\sum_{i=1}^{4} C_i}{C_4} + V_{ref}\sum_{i=1}^{3}(Z_i - X_i)\frac{C_i}{C_4} + V_{ref}\frac{C_5}{C_4}\cdot SEL \tag{6}$$

where $C_1:C_2:C_3:C_4:C_5=3:2:1:2:1/2$, and SEL is control signal for mode 2. When SEL=0 and 1, the circuit operates in mode 1 and 2, respectively. A fully differential two stage opamp is used in MDAC. Running at 20MS/s, the opamp achieve a DC gain of 41dB and GBW of 260MHz with power consumption of 750uW. Under the supply voltage of 0.6V, the opamp has an output swing of -0.3~0.3V differentially.

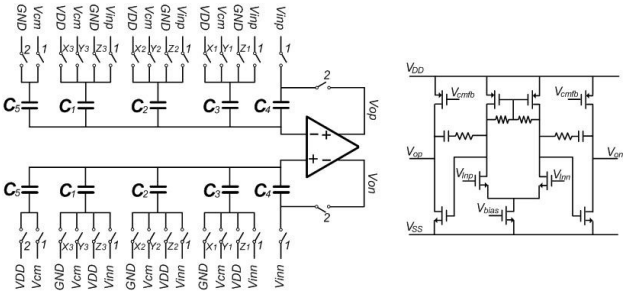

Fig.6 Circuit of MDAC and Opamp

V. Simulation Results

A behavior model of the proposed calibration technique is built. The residue amplifier is modeled by its transfer function simulated in transistor level. To test the performance of the calibration technique, the input to the ADC is chosen to be a band-limited random signal which is bounded in the bandwidth of the nonlinear interpolation filter. Designing with a tap number

of 40, the nonlinear interpolator has a bandwidth up to 80% of the Nyquist bandwidth with an accuracy of 13 bit. After the gain error is estimated, a sinusoidal signal is applied to the ADC to test the performance. Fig.7 shows the convergence performance of SNDR and SFDR versus the number of iterations. Without considering the sub-DAC error, Fig.8 shows the calibration enhances the SNDR from 49dB to 79dB. Fig.9 shows the SNDR at different bandwidths of input signals. A low pass filter with cut off frequency of 80% of the Nyquist frequency is required in front of the ADC to guarantee the input signal is in the effective band of the nonlinear interpolation filter. The limitation of the ADC bandwidth is the only drawback of the proposed technique. As long as the input is within the filter bandwidth, the estimation is accurate enough. The calibration can be finished within 2^{23} samples iteration.

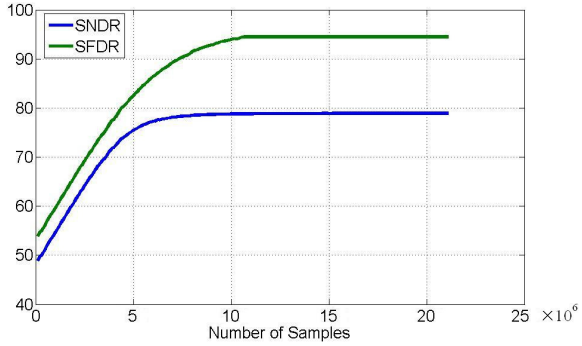

Fig.7 Convergence of SNDR and SFDR

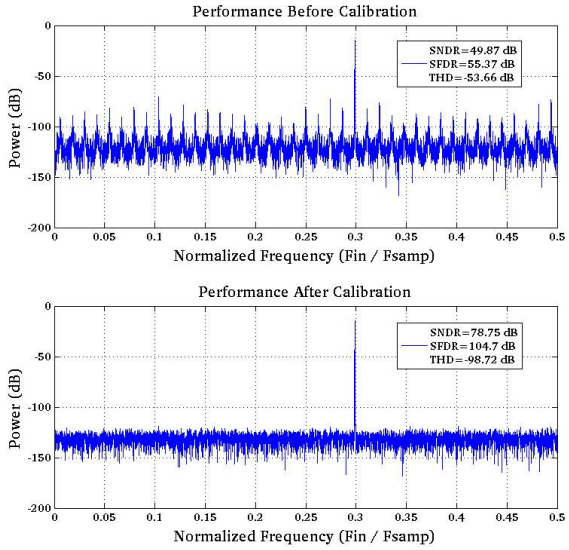

Fig. 8 Dynamic performance before and after calibration

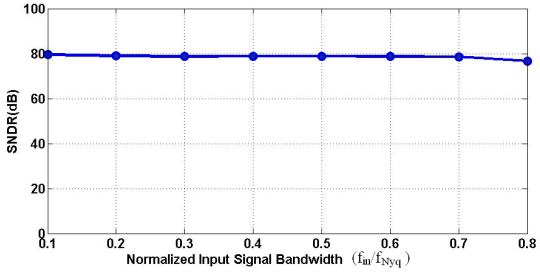

Fig.9 SNDR at different input signal bandwidth

VI. CONCLUSIONS

In the design of ultra-low voltage pipelined ADC, interstage gain error is a dominant error source. This paper presents a new digital background calibration technique to compensate these errors. In the proposed technique, a single channel ADC virtualizes another ADC by applying dual residue mode in first stage. Nonlinear interpolation is employed to find the difference between two ADCs which is used in LMS algorithm to estimate correction parameters. Comparing to traditional techniques, the proposed method takes the advantage of relaxation of analog circuit design. The design effort is mostly moved to the digital domain which exhibits low cost in deep sub-micron CMOS process and low voltage environment. Simulation results show the proposed calibration technique works successfully with a modified example pipelined ADC and improve the performance significantly.

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