Optimization of Microwatt On-Chip Charge Pump for Single-Chip Solar Energy Harvesting

Zhiyuan Chen, Man-Kay Law, Pui-In Mak and Rui P. Martins[1]

***Abstract*— In this paper, a compact single-chip solar cell with charge pump for microwatt solar energy harvesting is analyzed. Improved solar energy harvesting efficiency is achieved by utilizing lateral photodiodes. To optimize the charge pump (CP) efficiency in the microwatt level, the switch off-resistance (R_{off}) and the capacitive switching loss (P_C) are analyzed. The optimal flying capacitor size (C_{fly}) to achieve maximum power transfer is also calculated.**

I. Introduction

The emerging application of wireless sensor network continues to drive the ultra-low power system design. Solar energy harvesting has been proposed to extend the life time of these networks beyond the limitation which has been previously imposed by limited battery capacitance [1]. Since a solar cell can be easily achieved in a standard CMOS process, implementing the energy harvesting and the power management circuit in the same chip is an attractive solution. For a solar cell which has an open circuit voltage ranges from 0.4V to 0.5V [2], energy harvesting circuits normally require a DC-DC convertor to achieve a higher supply voltage. Charge pump is an attractive candidate in fully integrated SOC due to the feasibility of fabricating high-Q capacitors on silicon. In this paper, we analyze the integration of micro power photodiodes together with the charge pump circuit in the same substrate to realize an ultra-compact micro power harvesting system.

II. Photodiode Optimization

In a standard CMOS process, a photodiode is basically constructed by PN junctions. For a particular CMOS process that consists of N-Well (NW) and P-substrate (Psub), Psub/NW diode (i.e. the substrate diode) generates the largest photocurrent per unit area with a halogen light source due to its low doping level and hence increased depletion region depth [2]. Instead of using a stacked photodiode approach which can undermine the harvesting efficiency (as not all the available photodiodes can be used for harvesting energy), it is more promising to use parallel-connected photodiodes. For a typical PN junction, the current generated can be divided into two parts: the vertical current (current generated by the bottom surface) and the lateral current (current generated by the lateral surface). We can write,

This work was supported by the Macao Science and Technology Development Fund (015/2012/A1) and Research Committee of the University of Macau.

The authors are with the Department of Electrical and Electronics Engineering, Faculty of Science and Technology, University of Macau.

[1]Rui P. Martins (rmartins@umac.mo) is on leave from Instituto Superior Técnico (IST)/TU of Lisbon, Portugal.

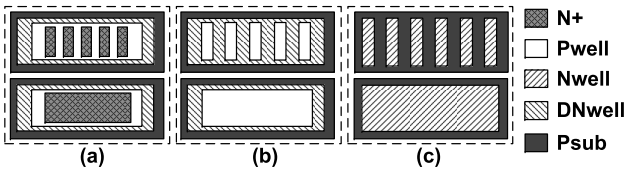

Fig. 1. Test structures used to determined the lateral current of (a) N+, (b) PW and (c) NW.

$$I_{ph} = J_{ph} \times (A + P \times D) \tag{1}$$

where J_{ph}, A, P and D denote the photodiode current density, area, perimeter and depth, respectively. For improved photodiode efficiency, the photodiode lateral current should be taken advantage of. However, due to the minimum distances imposed by the design rule, the depth of each PN-junction region becomes a key criterion in determining if increasing the lateral current is profitable. Consequently, several test structures has been fabricated in a standard $0.18\mu m$ 1P6M CMOS process (Fig.1). Three different photodiodes: 1) Psub/DNW, 2) DNW/PW and 3) Pwell/N+, are placed orthogonal to the halogen light source at $66.6mW/cm^2$. By using (1) and measurements from different test structures, the estimated depths are: N+ Depth = $0.34\mu m$, PW Depth = $0.76\mu m$, and NW Depth = $0.9\mu m$. With reference to the design rule from the process chosen, the minimum spacing for different regions are: N+ = $0.28\mu m$, PW = $0.86\mu m$, NW = $0.6\mu m$. It can be observed that only the PW/N+ photodiode can take advantage of the extra lateral current, which coincidences with the measurement result that the structure in Fig.1(a) generates the largest power.

III. Charge Pump Pptimization

As an on-chip photodiode generates a negative voltage, a CP should first reverse the input voltage followed by a boosting stage. This can be achieved by simply changing the conventional input of an n-stage CP from Vdd to ground, with V_{out} approximated by,

$$V_{out} = n(V_{in}\frac{C_{fly}}{C_{fly}+C_P} - \frac{I_{out}}{fC_{fly}} - R_{on}I_{out}) \tag{2}$$

A. Switch off-resistance

For a CP, the equivalent on-resistance is approximated by

$$R_{eq.on} = \sum R_{on} + \frac{1}{fC_{fly}} \tag{3}$$

A high efficiency CP should have $R_{eq.on} << R_L$ to minimize conduction loss. Moreover, R_{off} is responsible for the reversion loss due to the leakage current (I_{leak}). I_{leak} exists both in the charging and boosting periods of a charge pump. When

R_{off} and R_L are similar, I_{leak} cannot be neglect. $R_{eq.on}$, R_{off} and R_L should satisfy

$$R_{off} >> R_L >> R_{eq.on} \tag{4}$$

The R_{on} and R_{off} can be expressed as,

$$R_{on} = \frac{V_{ds.on}}{\beta((V_{gs}-V_{th})\times V_{ds}} \ (V_{ds.on} << V_{gs}-V_{th}) \tag{5}$$

$$R_{off} = \frac{V_{ds.off}}{Se^{\frac{V_{gs}-V_{th}}{mV_T}}} \ (V_{ds.off} >> 4V_T) \tag{6}$$

From (5), in order to achieve high efficiency, minimization of R_{on} can be achieved by reducing V_{th}. The gate programming floating gate, the body biasing technique [3] or low V_{th} device are commonly used for this purpose. However, comparing (5) and (6), lower V_{th} reduces R_{off} more rapidly than R_{on}. For micro power CP, which R_L is large, R_{off} cannot be neglected. One example is that CP using low V_{th} device suffers reduced R_{off} (e.g. R_{off} for native NMOS, $Vth = -0.28V$, is only about $0.3M\Omega$ in a standard $0.18\mu m$ 1P6M CMOS process).

B. Capacitive switching loss

Since the MOSFET switches (Mi) in the CP have to change states, their gates periodically need to be charged and discharged. Hence, it induces capacitive switching loss (P_C), which is donated as,

$$P_C = n \times \frac{1}{2} f \sum C_{Mi} V_d^2 \tag{7}$$

where n, C_{Mi}, V_d and f are the CP stage number, effective gate capacitance of M_i, the M_i gate drive voltage and the switching frequency, respectively. For an on-chip charge pump, due to the limitation in area, C_{fly} is usually small, which lead to a large f (from (3) and (4)). Hence, P_C is a significant loss, especially for micro power CP. For V_d less than or close to V_{th}, R_{on} decreases dramatically with the increase of V_d (from (5)). It is recommended to boost V_d rather than enlarge W to reduce P_C. For micro power CP, the efficiency loss due to R_{on} is small enough for minimum size MOSFET with high V_d.

C. Capacitance area optimization

Since the minimum size switch occupies little area, the main area of the CP is consumed by the on-chip capacitors. Intuitively, an ultra-small C_{fly} leads to an infinite P_C and a maximized C_{fly} leaves no area for solar cell implementation (i.e. no P_{in}). In both cases, $P_{in} - P_C$ are not optimal. Hence, there is a tradeoff between the on-chip capacitor area and the on-chip solar cell area. The input power P_{in} is determined by multiplying the solar cell conversion efficiency η, the input light power per unit area P_{opt} and the solar cell area A_{opt},

$$P_{in} = \eta P_{opt} \times A_{opt} \tag{8}$$

Assume V_d is boosted so that R_{on} can be neglected. There is a factor α between R_L and $\frac{1}{fC_{fly}}$ so that (4) is fulfilled,

$$R_L = \alpha \frac{1}{fC_{fly}} \tag{9}$$

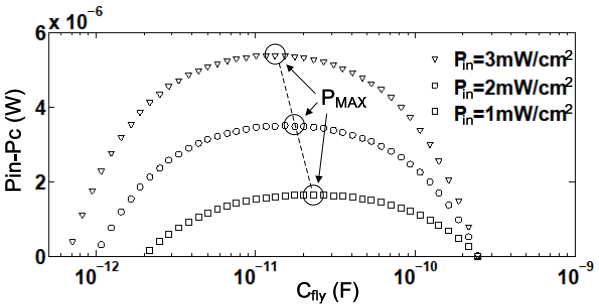

Fig. 2. Matlab plot of P_c, P_{in} and $P_c - P_{in}$ under different illuminations ($3mW/cm^2 \approx 20000Lux$), by assuming $A = 1mm^2$, $\beta = 1f/um^2$,$\eta = 20\%$, $\alpha = 100$, $n\Sigma C_{Mi} = 40fF$, $V_d = 1V$, $R_L = 0.5M\Omega$ and n=4.

The on-chip capacitance as a function of area can be obtained from the PDK as follow,

$$C_{fly} = \beta \frac{A_C}{n} \tag{10}$$

For a given area A, it is mainly composed of the capacitor and the solar cell,

$$A = A_C + A_{opt} \tag{11}$$

Combining (7) and (8-11) together,

$$P_{in} - P_C = \eta P_{opt} \times (A - \frac{nC_{fly}}{\beta}) - \frac{\alpha \sum C_{Mi} V_d^2}{2R_L C_{fly}} \tag{12}$$

Solving Eq. (12) indicates that, when $C_{fly} = \sqrt{\frac{\alpha\beta\sum C_{Mi}V_d^2}{2nR_L\eta P_{opt}}}$, $P_{in} - P_C$ has its maximum value $\eta P_{opt} \times A - \sqrt{\frac{2\alpha n \sum C_{Mi} V_d^2 \eta P_{opt}}{\beta R_L}}$. For a general on-chip CP together with solar cell, $P_{in} - P_C$ in different illuminations are plotted separately in Fig. 2. Note that a $C_{fly,Max} = 10^{-9}F$ result in $Pin = 0$ and a $C_{fly.Min} = 0$ leads to f=+∞ (e.g. $P_C = +\infty$). Also note that a larger C_{fly} is required to optimize $P_{in} - P_C$ when illumination decreases, since P_C exerts a more significant influence.

IV. Conclusion

An analysis of a micro-watt single-chip solar energy harvesting module with on-chip solar cell and charge pump is presented. By combining the charge pump and the solar cell in the same substrate, highly compact energy harvesting systems can be accomplished. Improved solar energy harvesting efficiency is achieved by utilizing N+ lateral photodiodes. Minimum size MOSFET is utilized to reduce the capacitance switching loss. The optimized charge pump flying capacitance to achieve maximum power is also analyzed.

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