A 0.5V 10GHz 8-Phase LC-VCO Combining Current-Reuse and Back-Gate-Coupling techniques Consuming 2mW

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***Abstract*—This paper describes an ultra-low-voltage low-power 8-phase voltage-controlled oscillator (VCO) for 10GHz beam-forming satellite receivers. It is composed by four 0.5V current-reuse LC-VCO cells inter-locked by direct-back-gate coupling, featuring independent sizing of coupling strength and frequency tuning, while avoiding the risk of forward bias the substrate p-n junctions. Optimized in 65nm CMOS, the 8-phase VCO draws only 2mW. The phase noise at 1MHz offset is –114dBc/Hz to –110dBc/Hz over a 32.5% tuning range from 8.55 to 11.88GHz. These results correspond to a high-and-stable FOM within –188 to –189.5dBc/Hz.**

I. Introduction

The voltage-controlled oscillator (VCO) is an essential building block of all wireless and wireline communication systems. Especially, a poly-phase local oscillator (LO) signal provided by the VCO supports a wide variety of transceivers with image-rejection [1], harmonic-rejection [2] and phased-array beamforming [3] capabilities. This paper proposes an ultra-low-voltage 8-phase LC-ring VCO which is suitable for 10GHz beamforming satellite receivers.

The design of a high-frequency 8-phase VCO is non-trivial and frequency division is a common practice to achieve it. A differential VCO followed by a div-by-4 circuit can generate the desired 8-phase LO, with the schematic presented in Fig. 1(a). However, the VCO must operate at a frequency 4 times higher than the output (i.e., 40GHz), significantly penalizing the power and tuning range. A possible alternative is depicted in Fig. 1(b), where four differential LC-ring VCO cells are coupled to construct an 8-phase VCO. This scheme has the advantage of excellent phase noise, at the expense of power and chip area.

Within the nanoscale CMOS environment, the high f_T of MOS devices allows operation in the moderate inversion region for GHz-range applications, resulting in substantial power savings. Specifically, when a 0.5V supply is adopted, the MOSFET can be considered as a four terminal device without the risk of forward bias the substrate p-n junctions. The body can be properly biased to reduce the threshold voltage (V_T) [4], thus serving as the direct coupling terminal of multiple VCOs to synthesize a poly-phase LO. Another power-reduction technique can be implemented by modifying the typical cross-coupled pair from purely NMOS or PMOS, to a PMOS-NMOS hybrid topology. As a result, the number of current paths will be halved from 8 to 4 for an 8-phase VCO. Together with the use of a minimized 0.5V supply, the power efficiency of this work would be strongly improved (i.e., 0.25mW per LO-phase at 10GHz).

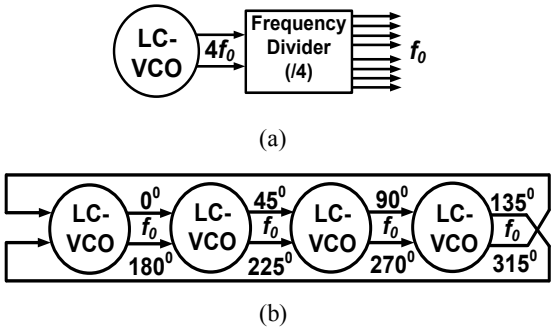


Fig. 1. 8-phase LO generation by: (a) one LC-VCO followed by divide-by-4. (b) Direct coupling of four LC-VCOs.

II. State-of-the-art Poly-Phase VCOs

Conventionally, transconductor-ring VCOs have been the choice for wideband poly-phase signal generation due to their low-power and small-area advantages. Regrettably, its phase noise is too high for most high-tier communication systems. The LC-ring VCO is more desirable for its high-quality LC tank, lowering the phase noise and allowing higher operating frequency. In [5] and [6], the poly-phase LO is generated via coupling several identical LC VCOs. The coupling transistors are in parallel with the switching ones, being the coupling strength expressed by [7],

$$\alpha = \frac{g_{CPL}}{g_{SW}} = \frac{W_{CPL}}{W_{SW}} \quad (1)$$

where g_{CPL} (g_{SW}) is the transconductance of the coupling (switching) transistor, and W_{CPL} (W_{SW}) is the width size of the coupling (switching) transistor. The coupling strength between the gain stages has a strong effect on the phase noise and phase precision. Strong coupling between the gain stages can reduce the phase error, but larger coupling transistors

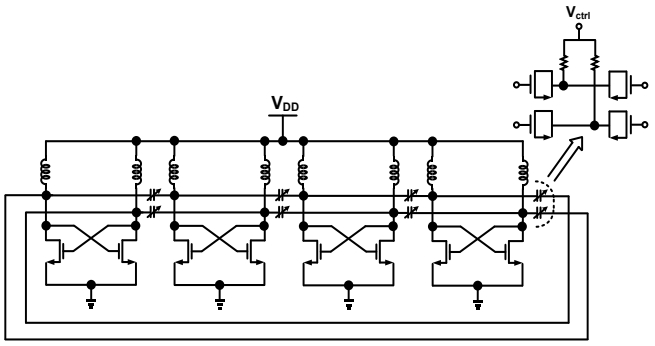
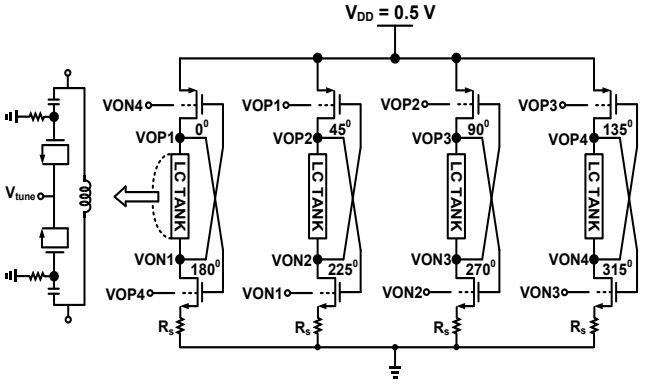


Fig. 2. Conventional 8-phase LC VCO [9].

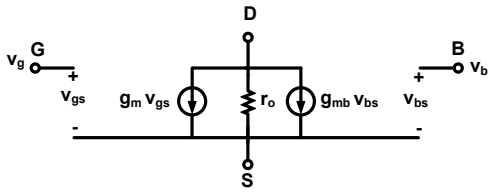
imply additional phase noise and parasitic capacitances (i.e., narrower tuning range) while drawing substantial power. In [8], the poly-phase VCO is based on differential excitation of a closed-loop transmission line. Since the LC-ladder filter exhibits a low-pass characteristic, it renders itself not suitable to sustain high-frequency signals. Besides, the complementary G_m cells necessitate more voltage headroom.

Another 8-phase LC VCO (Fig. 2) was proposed in [9] to address the abovementioned issues. It involves four LC-VCO cells coupled in a ring manner via the MOS varactors. This structure has shown an improved phase noise as no extra transistor is entailed for VCO coupling. However, since the MOS varactors combine two roles (coupling and frequency tuning), the coupling strength and LC-tank quality factor (Q_{var}) are undesirably dependent. This fact results in sizeable phase noise variation over the VCO tuning range. On the other hand, the use of four VCOs simply implies high power consumption.

Fig. 3(a) depicts the proposed back-gate-coupled 8-phase VCO. The current is reused between the NMOS and PMOS devices [10]. Thus, the bias current can be halved while providing the same negative conductance. Unlike the cross coupled LC-ring VCOs where the cross connected transistors switch alternately, in the current-reuse structure, the PMOS and NMOS are switched at the same time. Due to the voltage limited mode of operation, the large drop in dynamic current during the first half period leads to waveform distortion which results in unbalanced differential voltage swing. Furthermore, unbalanced differential outputs can deteriorate the phase noise performance which may result in a large phase error in the poly-phase output. Thus, a current control scheme is adopted to force the VCO to operate in the current limited regime with the output voltage swing limited by the current during both periods. The source resistor (R_s) controls the DC and the peak dynamic currents. The current-reuse VCO can be operated in the current limited mode to generate a balanced output voltage swing, since the voltage swing is a function of the peak dynamic current [10]. In Fig. 3(a), four current-reuse LC-VCOs are coupled through the back-gate of the switching transistors. Here, all transistors are assumed to be housed in



(a)



(b)

Fig. 3. (a) Proposed back-gate-coupled 8-phase VCO and (b) the small-signal equivalent circuit of its back-gate-coupling transistor.

separated wells, so that each transistor can be used as a four terminal device. The key concern of this topology derives from the fact that large signals, coupled through the body terminal, may forward the p-n junction between the diffusions degrading circuit performance. In typical circuit design, the body terminal should always be connected to the highest voltage for PMOS, and the lowest voltage for NMOS. To overcome this problem, a *RC* network was used in [11], through which a large output signal is applied to the body terminal. The capacitor *C* is used for coupling and *R* is used to bias the body. In the proposed back-gate-coupled 8-phase VCO, the output signal can be applied directly to the body terminal of the switching transistor since, at a 0.5V supply voltage, the coupling signals are not large enough for forward bias. The body is biased at half-scale of the 0.5V supply, reducing the threshold voltage. Fig. 3(b) shows the equivalent circuit of the back-gate-coupled device, with coupling strength given by [12],

$$\alpha_B = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2\Phi_F - V_{BS}}} \tag{2}$$

where γ, Φ_F and V_{BS} are the body-effect coefficient, work function, and body-to-source bias voltage, respectively. From (2), the coupling strength (α_B) is related to V_{BS}. Therefore, to increase the coupling strength, the body-source reverse bias should be minimized, which is achievable with a 0.5V supply and is adequate to prevent forward biasing. On the other

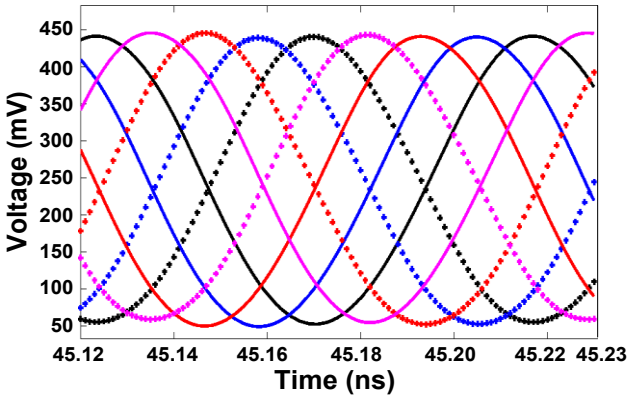


Fig.4. Simulated transient output waveforms.

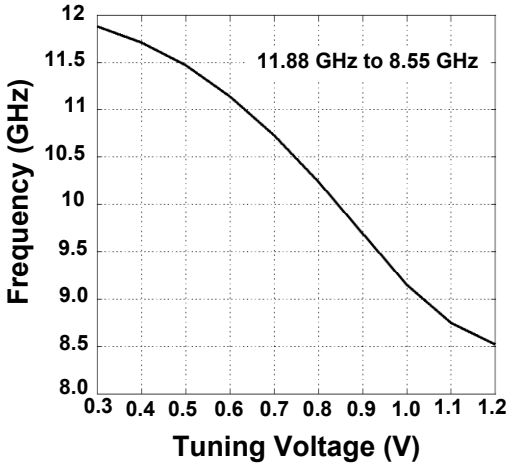


Fig.5. Simulated frequency tuning range.

hand, frequency tuning is obtained by combining MOS varactors with fixed metal-insulated-metal (MIM) capacitors. MIM capacitors show high *Q* factors at high-frequency due to their low intrinsic loss. Since the frequency tuning in first order does not the coupling, the phase-noise variation can be minimized over the tuning range.

III. Simulation Results

The proposed 8-phase VCO is designed in 65nm CMOS. A small inductor size of 0.4nH is employed for its high Q factor and compact layout. Since the PMOS and NMOS switching transistors are in series and the characteristic of the back-gate in the PMOS and NMOS transistors are different, the device sizings are critical. Specifically, the device sizes are carefully picked to generate the same transconductance in the LC tank for balancing the output swing, as well as providing the same coupling strength so as to reduce the phase error. In the simulations, the 8-phase VCO draws only 2mW at a 0.5V

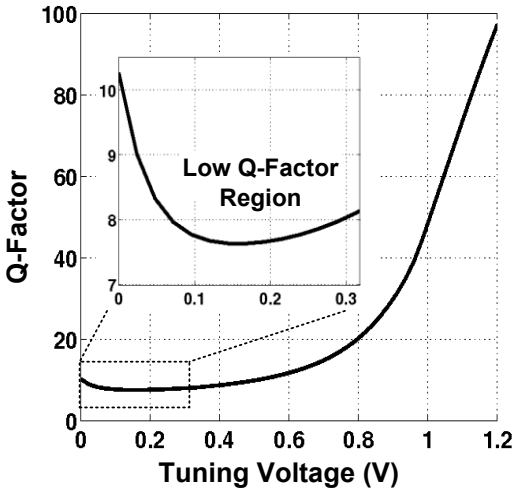


Fig.6. Q-factor of MOS varactor.

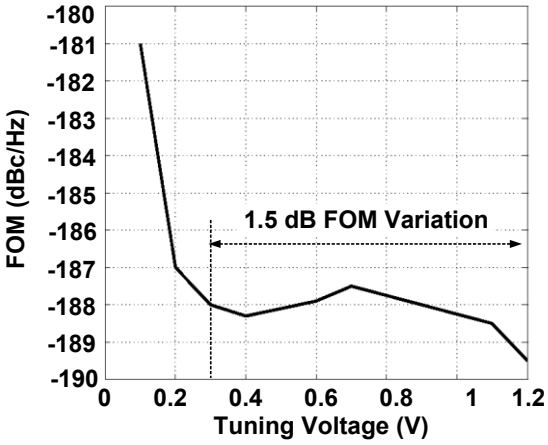


Fig.7. FOM versus tuning voltage.

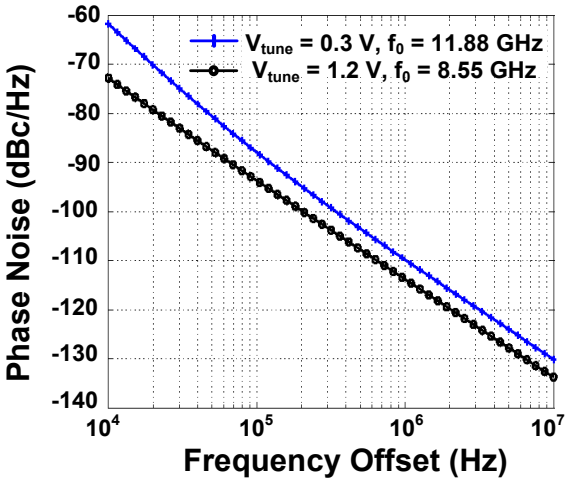


Fig.8. Simulated phase noise.

TABLE I.
Performance Benchmark of the
Proposed 8-Phase VCO with the State-of-the-Art.

	[9]	[11]	[12]	This Work (Simulation)
Technology	0.13-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	65-nm CMOS
Supply (V)	1.2	1.8	1.25	0.5
Output Phases	8	4	4	8
Tuning Range (GHz)	36.7-40.0 (8.3%)	1.047-1.39 (28%)	1.83-2.02 (9.8%)	8.55-11.88 (32.5%)
Power (mW)	16.4	5.4	2.2	2.0
Phase Noise (dBc/Hz)	–94.3 @1MHz	–120 @1MHz	–124 @1MHz	–114 @1MHz
FOM (dBc/Hz)	–174	–173.5	–186.7	–188 to –189.5

supply. Fig. 4 shows the transient output waveforms, where the amplitude difference is within a few mV. By properly sizing R_s and active devices, the voltage swing can be made very symmetric during the two half periods. Fig. 5 shows the frequency variation with the tuning voltage from 0.3 to 1.2V. At this tuning voltage the VCO is tunable between 8.55 to 11.88GHz, which corresponds to a 32.5% tuning range. The tuning voltage is started from 0.3 V due to the Q factor limitation as shown in Fig. 6, where the Q-factor profile of the MOS varactor is shown. The achieved FOM is shown in Fig. 7, showing a small variation of 1.5dB over the tuning range.

Fig. 8 shows the simulated phase noises. At a 1MHz offset, the phase noise is –110dBc/Hz at the maximum frequency (11.88GHz) and –114dBc/Hz at the minimum frequency (8.55GHz). The corresponding FOM ranges within –188 to –189.5dBc/Hz. Table I summarizes the results and exhibits a benchmark performance to the state-of-the-art. This work, at the simulation level, shows a favorable improved tuning range and FOM under a low-voltage supply.

IV. Conclusions

An ultra-low-voltage, current-reuse and back-gate-coupled 8-phase LC-VCO for 10GHz beamforming satellite receivers has been proposed. The current-reuse technique saves half of the power when comparing it with the conventional cross-coupled LC-VCOs. To alleviate the dependency of phase noise and phase precision in transistor-coupled VCOs, the direct-back-gate coupling was adopted. At a very-low-voltage supply of 0.5V it avoids any *RC* bias networks and prevents the risk of forward bias the substrate p-n junctions. The back-gate coupling also helps reducing the transistor threshold voltage. Optimized in 65nm CMOS, the 8-phase VCO shows excellent phase precision and is tunable between 8.55 to 11.88GHz. The phase noise is within –114 to –110dBc/Hz at 1MHz offset, and the total power consumption is 2mW. The FOM variation is only 1.5dB from –188 to –189.5dBc/Hz.

Acknowledgement

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