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UMCHIP - First Integrated Circuit designed in Macau

(Multifunction & Mixed A/D - 1.2 μm CMOS Technology)

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Abstract

This paper presents the results of a Research & Development Project developed in F.S.T. during the first 6 months of 1994. In this Project we designed an Integrated Circuit - IC using an advanced CMOS technology of 1.2 μm, from AMS (Austria Mikro Systeme). This project was made in cooperation with the Integrated Circuits and Systems - ICS Group from IST, Lisbon, Portugal. The IC design was carried-out by FST post-graduated students of the Master Program in Electrical and Electronics Engineering, as a final project of the course Microelectronic Circuit Design. These students, in a number of 10, were divided in 5 groups of two and each group has designed a specific digital or analog basic circuit, being the functions implemented the following : SC Biquad Filter, 4-bits D/A Converter, 16-bits SRAM & 16-bits DRAM, 4-Phases Waveform Generator, 4-bits / 7-segments Display Decoder plus a Super-buffer. After simulation and layout, the 5 different designs were integrated in a Multiproject Chip - MPC (the first to be designed in Macau) and submitted to fabrication in AMS - Austria, through the ICS Group - Portugal. The overall chip occupies a silicon area of 6mm^2 and the total number of pins is equal to 48. A Photo of the Chip and Measured Results, obtained from the prototype samples received from AMS, will also be presented.

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Introduction

The main purpose of the project UMCHIP was to motivate, first of all, a group of post-graduated students with diversified preparation in Electronics, for the acquisition of knowledge in terms of the basic electronic principles and techniques needed by the designer throughout the CMOS IC design process. This project was the last part of the evaluation process in a Master course named Microelectronic Circuit Design and it can be considered as a whole a very good result because each group of students was able to finish a complete process of calculation and design, computer simulation and layout of a specific function in IC form using an advanced CMOS technology of 1.2 μm from AMS. There were even some cases where some of the groups obtained very good measured results on the chip (after fabrication). This aspect is of significant importance because in the beginning of the course the knowledge about CMOS IC design was almost none (regardless of the fact that the students came from different Universities, either in China, Hong Kong and Macau) and the duration of the course (4 months part-time) associated with the duration of the design procedures (1.5 months also in a part-time basis) was too short to achieve a good result in a first prototype. Nevertheless, the final architecture of the chip in terms of area (less than 6 mm^2) is quite reasonable for the different Analog and Digital - A/D functions implemented. These functions constitute some of the most important functions that can be found in a high variety of IC's with applications in Telecommunication and Control Systems. The measured results obtained with the prototype samples can also be considered satisfactory for a first run of a mixed A/D circuit.

In this paper, we will present for the different projects included in this MPC the architectures, simulation results (electronic simulation - with HSPICE) layout (with MAGIC) and also some results obtained with the first prototype chip. Firstly, we will present the design and simulation results of a Switched-Capacitor Biquad Lowpass Notch Filter, including a functional simulation of the architecture with SWITCAP-2 and electronic simulations of a CMOS Class AB - Operational Amplifier - OA. Secondly, we will present the architecture, simulation results and the layout of a 4-bits D/A Converter using a charge re-distribution architecture that includes a Class A OA. After, a 16-bits DRAM and a 16-bits SRAM, including decoding logic are presented in terms of design simulations and layout. We will also present a Multiphase Switching Waveform Generator (based on D-type Flip-Flops) capable of controlling the SC Biquad Filter and a Programmable Logic Array - PLA. A 4-bits (BCD) / 7 segments display decoder is also presented together with a digital Super-buffer, including measured results obtained with the first prototype samples. Finally, we will present the Microphotograph of the Chip and the Conclusions.

Switched-Capacitor Biquad Filter

The SC Biquad Filter designed, sampled @ F_s=384kHz, was a Lowpass Notch Filter with f_p=3.08kHz, Q_p=3.9 and a notch @ f_N=8.15kHz.The architecture is presented in Fig.1-a), together with the capacitor values, the 2 non-overlapping clock waveforms and the electronic structure of a CMOS switch. In Fig.1-b) we present results of the functional simulation using SWITCAP-2. In Fig. 2 we present the structure of the class AB OA designed with a Gain=70 dB and GBW=10 MHz (>10 F_s).

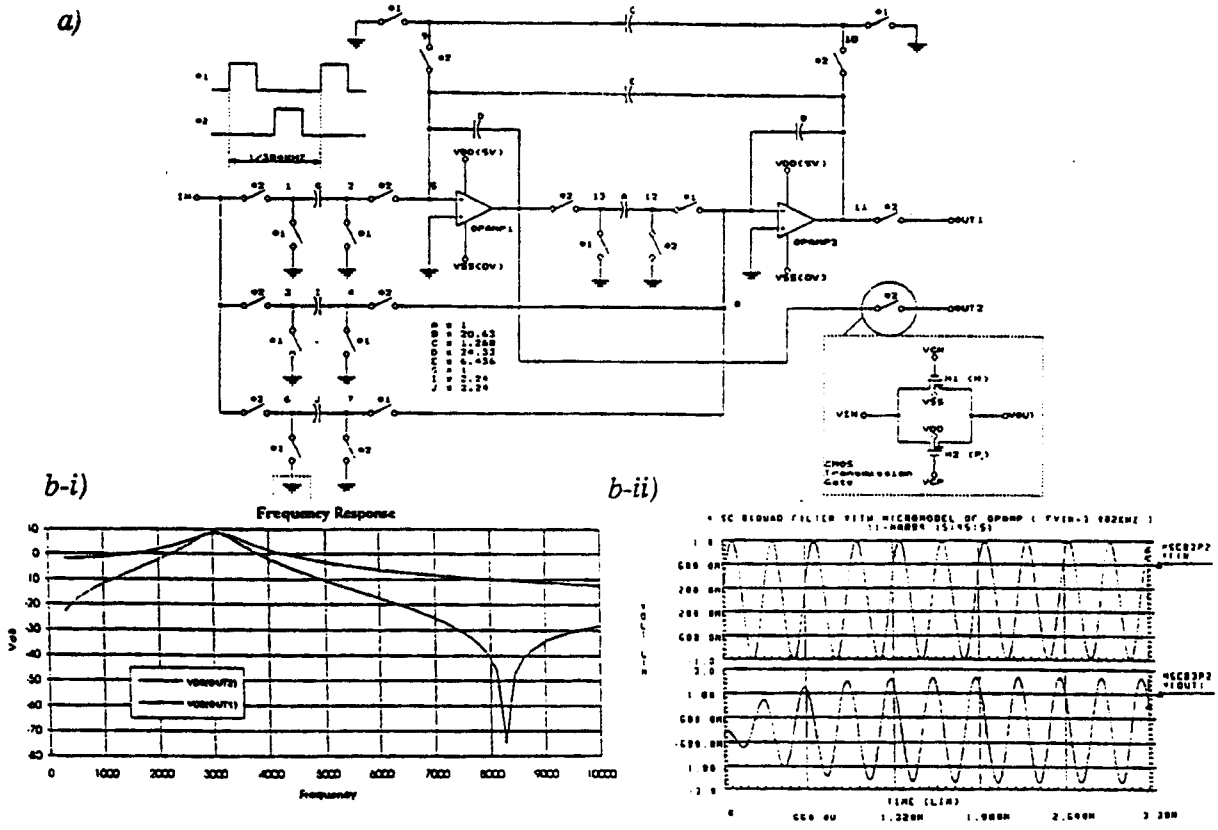
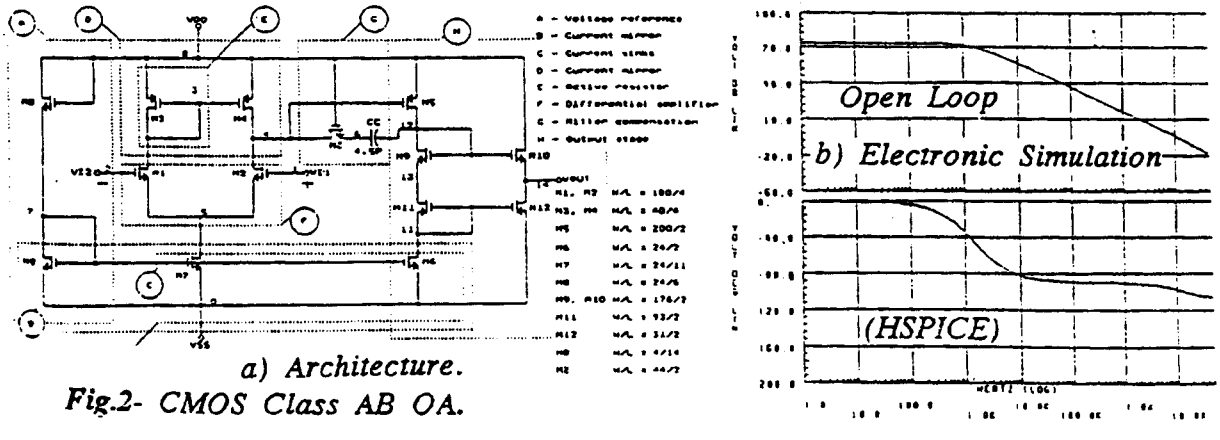


Fig.1 - SC Biquad Filter. a) Architecture, capacitor values, switching waveforms and CMOS switch. b) Functional simulation with SWITCAP-2, i) Frequency ii)Time.



a) Architecture.

Fig.2- CMOS Class AB OA.

4-bits Digital / Analog Converter

The architecture of an inverting 4-bits charge redistribution D/A Converter is presented in Fig.3-a). The electronic simulated input / output characteristic obtained by HSPICE (considering a CMOS class A OA) is presented in Fig.3-b). In Fig.3-c) we present the layout architecture where we can cleary see the OA (top) and the capacitor array (bottom right).

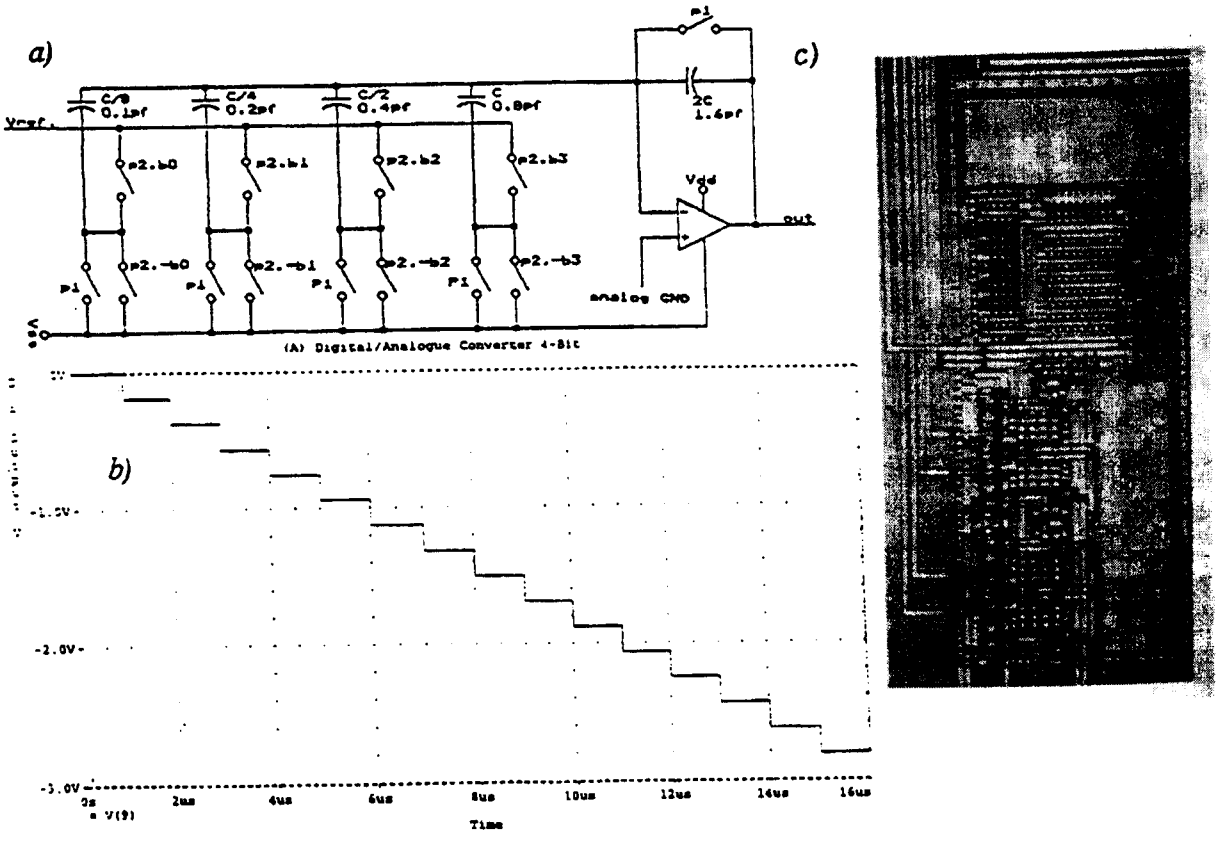


Fig.3 - 4-bits D/A Converter. a) Architecture, b) Electronic Simulated input / output Characteristic, c) Layout (photo from the chip).

16-bits Dynamic-RAM and 16-bits Static-RAM

In Fig. 4-a) is presented the transient process of the read cycle in the D-RAM and in Fig. 4-b) we can see the layout of the D-RAM and the logic decoder.

Multiphase Switching Waveform Generator

A Multiphase Switching Waveform Generator was designed to meet the necessary requirements of the 2 clock phases that control the SC Biquad Filter presented before. The architecture of the Generator, based on a Ring Counter, is presented in Fig. 5-a), being the basic

cell a Master/Slave D-Flip Flop (Fig. 5-b) . In the Fig.5-c) we present an electronic simulation where we can clearly see the two non-overlapping phases (V_{20} and V_{21}).

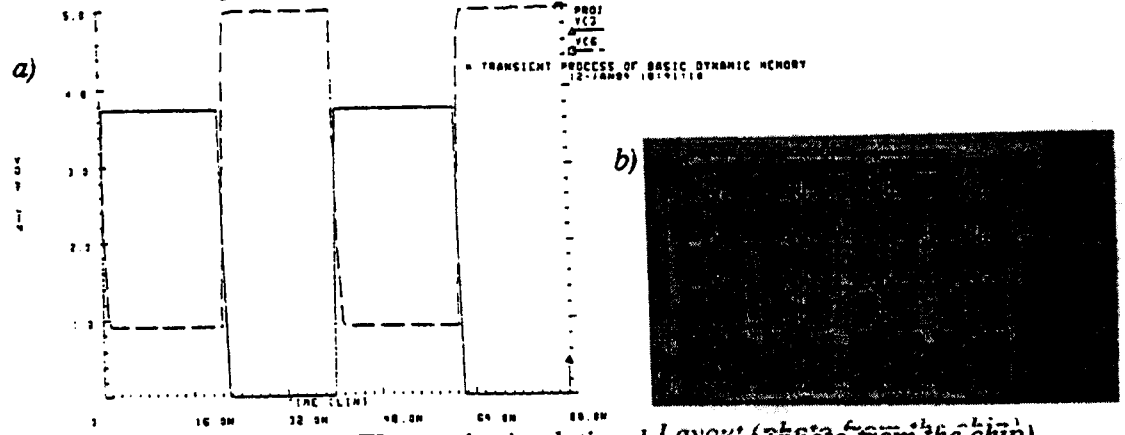


Fig.4- D-RAM. a) Electronic simulation. b) Layout (photo from the chip).

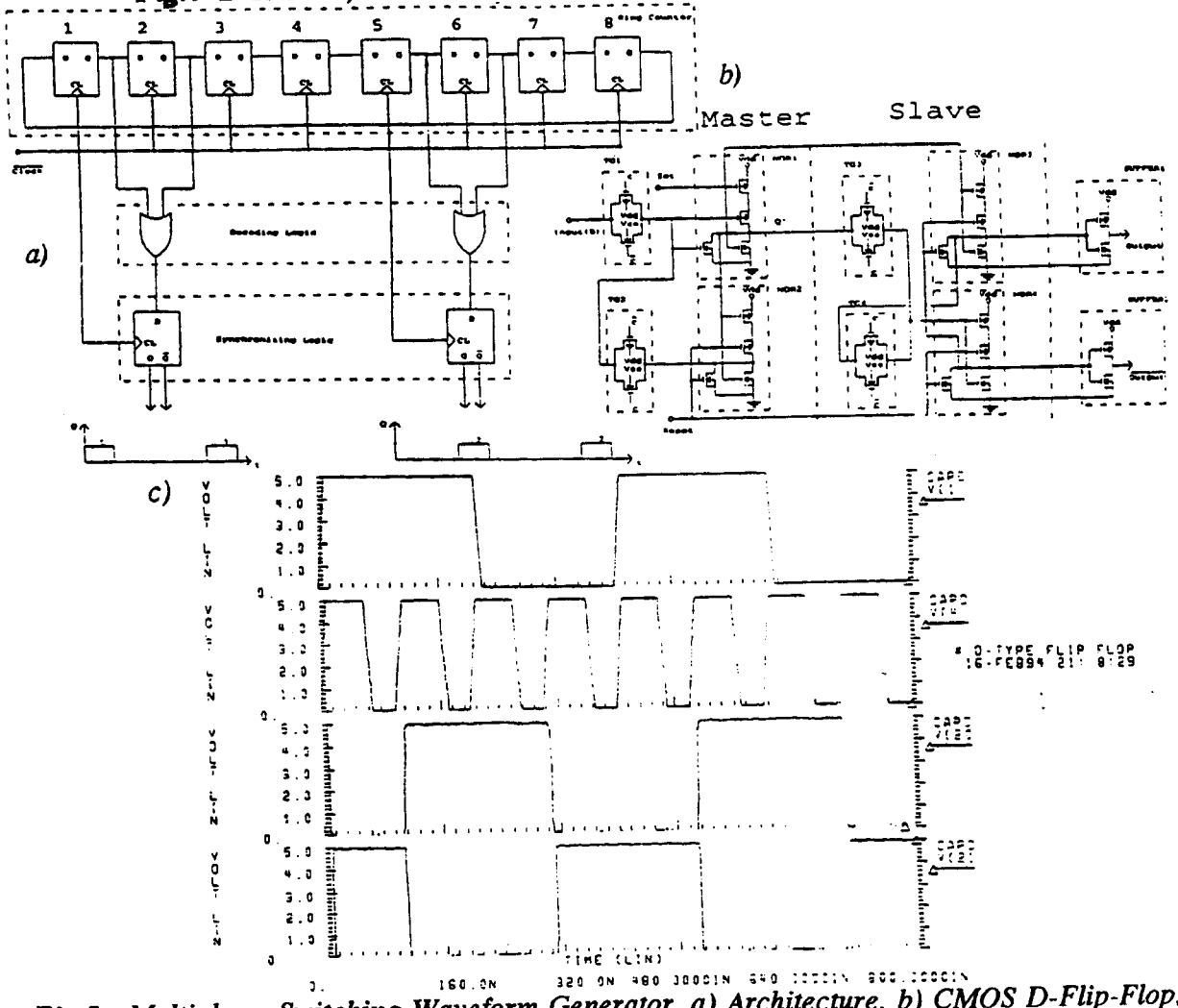


Fig.5 - Multiphase Switching Waveform Generator. a) Architecture, b) CMOS D-Flip-Flop, c)Simulation of the circuit with the 2 non-overlapping clock phases (V_{20} and V_{21}).

4-bits (BCD) / 7 segments display PLA Decoder plus a Super-buffer
(includes Measured Results)

A PLA is usually constituted by two major subsections or planes as presented in Fig.6-a). The AND plane requires double rail inputs (each independent variable and its complement) to generate the product terms required by the defining logic equations of a 4-bits / 7 segments decoder. The OR plane will make the logic adition (OR) of the different product terms to produce the dependent variables. In Fig. 6-b) we present the overall layout of the PLA decoder (as obtained from a photo of the chip) where we can clearly see the AND plane (right side-with 4 inputs) and the OR plane (left side-with 7 outputs). In Fig. 6-c) a measured result extracted from the operation of the chip (by means of a logic analyzer) is presented, where we can see the different input configurations (BCD) and the resulting outputs that switch on or off the 7 segments of a led display.

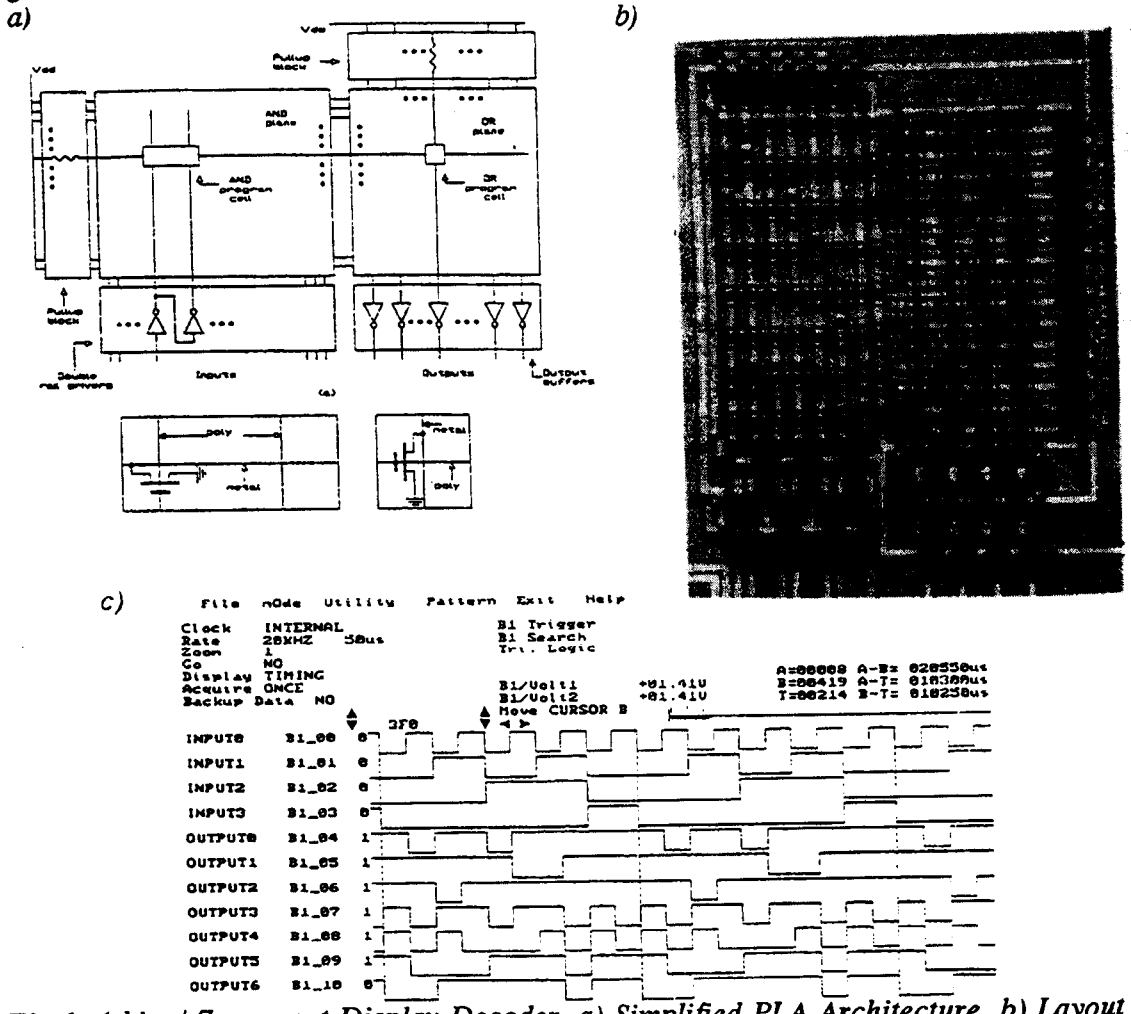


Fig.6- 4-bits / 7 segment Display Decoder. a) Simplified PLA Architecture, b) Layout of the PLA (photo from the chip),c) Measured results (logic analyzer) from the prototype chip.

It was also designed a Super-buffer that is presented in terms of layout in Fig. 7-a), with measured results (obtained in a digital oscilloscope) shown in Fig. 7-b).

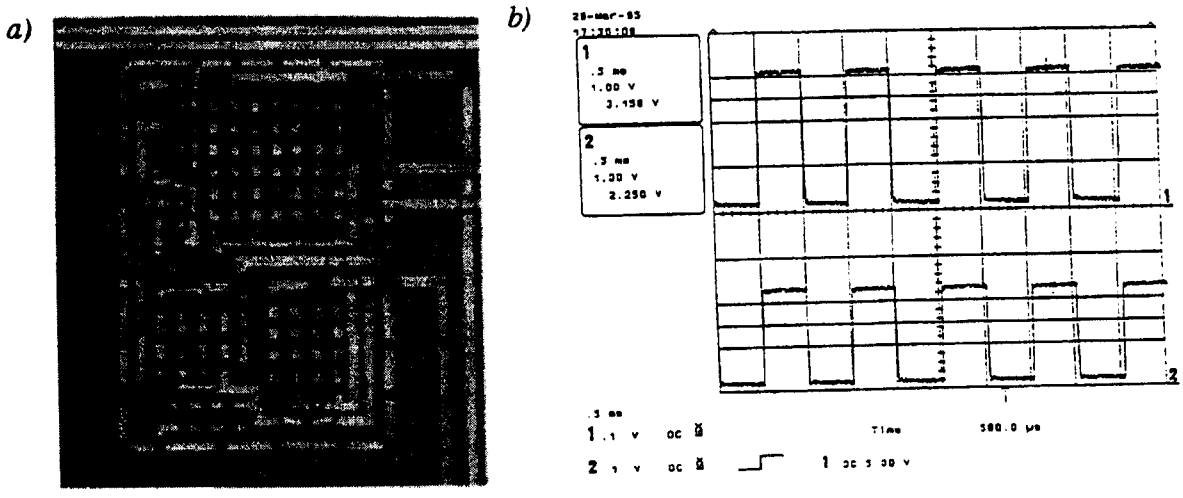


Fig.7- Super-buffer a) Layout architecture, b) Measured results (1 - Input, 2 - Output).

UMCHIP Microphotograph and Conclusions

The microphotograph of the overall UMCHIP is presented in the Fig.8, occupying a total area of 6mm2. As a conclusion we can say that, this paper presented, with good results, the first Integrated Circuit designed in Macau. The measured results obtained can be considered satisfactory for a first run of a mixed analog-digital circuit.

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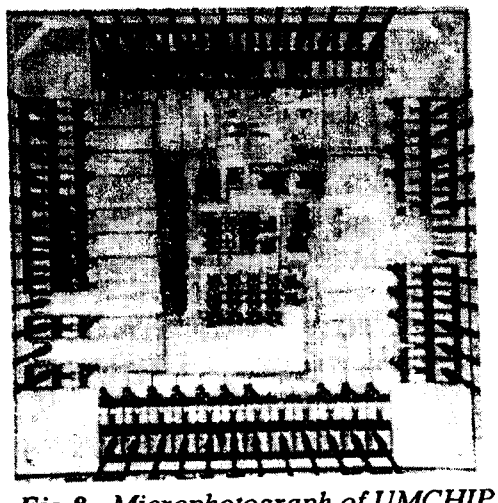

Fig.8 - Microphotograph of UMCHIP.