A DT 0-2 MASH ΣΔ Modulator with VCO-Based Quantizer for Enhanced Linearity

Tao He, Yun Du, Yang Jiang, Sai-Weng Sin, Seng-Pan U[1], R.P.Martins[2]
State-Key Laboratory of Analog and Mixed Signal VLSI (http://www.fst.umac.mo/en/lab/ans_vlsi/index.html)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail: pipfrank1988712@gmail.com, TerrySSW@umac.mo
1 - Also with Synopsys - Chipidea Microelectronics (Macau) Limited
2 - On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

***Abstract*—This paper presents a new structure of the discrete time 0-2 MASH sigma-delta modulator implemented with VCO-based quantizer in the second stage. The proposed scheme enhances the linearity of the VCO based quantizer, meanwhile it takes advantage of the intrinsic DEM function and first order noise shaping in the second stage. Besides, the matching requirement is relaxed and the digital canceling filter is largely simplified. Moreover, no additional active adder in or between two stages is needed because of the 0-2 MASH structure, which can save a lot of power. The proposedDT0-2 MASH sigma-delta (ΣΔ) modulator with 10MHz signal bandwidth for wideband applications is designed and simulated in Matlab. The performance of the modulator can reach 97dBSNDRunder a sampling rate of 1.15GHz.**

I. INTRODUCTION

Delta-sigma modulators are widely used for high resolution and moderate-bandwidth analog to digital converters. Due to the noise shaping function of the modulator, the in-band noise floor can be much lower than in theNyquist ADC. In order to enhance the ability of noise shaping, and to further reduce the noise floor, increasing the order of the delta-sigma modulator is revealed to be themost efficient way to achieve it. Nevertheless, in higher order (>3) modulator design, the stability constitutes a serious problem. To overcome it, multi-stage topology (MASH) is an efficient structure, where the noise shaping can reach higher orderwhile experiencing the stability of lower order modulators. [1]

Another method to increase the order of the noise shaping leads tothe implementation of a new-structure in the ADC with intrinsic noise shaping, like the VCO-based quantizer [2]. Due to the open loop noise shaping the implementation of theVCO-based quantizer can reach a stability of n+1 order, where n is the order of the loop filter in delta-sigma modulators. However, the main drawback of the VCO-based quantizer is related with its intrinsic nonlinearity. Extremely large harmonics always appear in the signal bandwidth, which seriously degradethe performance [3].

In this paperwe propose a DT 0-2 MASH structure which utilizes both the advantages of the MASH structure and

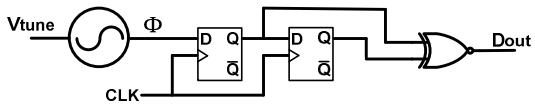

Fig.1 Block diagram of a single-bit VCO-based quantizer.

VCO-based quantizer. Furthermore, the nonlinearity of the VCO-based quantizer can be greatly reduced and the operational amplifier (OPAMP) requirement of the MASH can be significantly relaxed.

The paper is organized as follows. In section II, the main theoretical aspects of VCO-based quantizer will be reviewed. In section III, the proposed novel VCO-based quantizercombined with the DSP implementation details will be presented, followed by the description of the insertion of the quantizer in a ΣΔ modulator, and simultaneously analyzed with the DAC optimization. Next, the simulation results will be discussed in detail in section IV, and finally, the conclusions will be drawn in section V.

II. VCO-BASED QUANTIZER AND ITSMASH IMPLEMENTATION

The internal structure of the VCO-based quantizer, shown in Fig.1 uses a multi-phase ring oscillator to achieve voltage-to-frequency conversion mostly in the digital domain. As revealed in [2], the D-flip flops and XOR gate operate as counters and register (with no reset), thus allowing high-speed of operation with small latency.

The tuning characteristic of the VCO cell can be described as,

$$\Phi_{VCO}(t) = 2\pi K_v \int V_{Tune}(t)dt \qquad (1)$$

where the phase output of the VCO cell isproportional to the integration of the VCO tuning input. The K_v is the ratio of frequency to tuning voltage, which is also the source of the VCO nonlinearity, as shown in Fig. 2. The linearity of the

VCO is only adequate for very small input signal swing (less than 50mv). When the input swing becomes largerthe linearity would be considerable degraded.

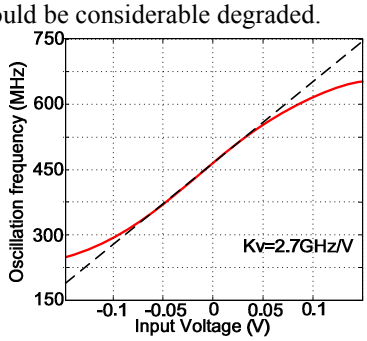

Fig.2 Tuning characteristic of the VCO.

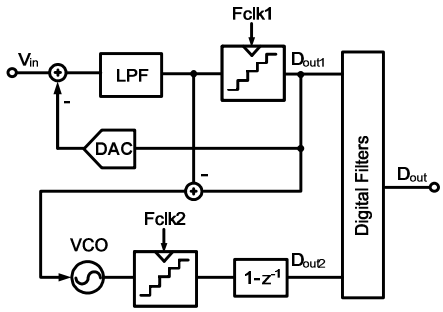

Fig.31-1 MASH implemented with VCO.

Therefore, practically, the VCO-based quantizer is not a high performance quantizer due to the serious nonlinearity of the VCO that dramatically affects the performance of the modulator. One of the highest impactsof its nonlinearity is the introduction of harmonic distortion that can significantly degrade the performance of the quantizer.Further tests within the CT ΣΔ modulator show that this nonlinearity will enhance the noise floor when mismatch and nonlinearity in the DAC feedback are increased. Then, the nonlinearity of the VCO-based quantizer has always been considered as the most important bottleneck limiting the attainmentof high resolution by the VCO-based quantizer.

In [4], a DT 1-1 MASH structure is proposed where the 1st stage is achieved with a 1st order DT delta-sigma modulator and the VCO-based quantizer is implemented in the 2nd stage, as shown in Fig. 3. There, the small quantization noise value is the input of the second stage VCO-based quantizer, therefore the nonlinearity of the VCO is significantly relaxed.

However, there are two drawbacksthat turn this MASHin a notso competitive structure. Firstly, and inherently to a MASH topology, the matchingbetween the digital and analog transfer functions should be perfect; otherwise the leakage of the quantization noise from the 1st stage will appear directly in the output of the modulator. This is one of the serious disadvantages when tryingto achieve a high-performance MASH modulator. To combat this leakage errorthe OPAMP in the first stage should obey very high requirements to improve the matching. For example, in [4] the OPAMP has a gain of 65dB and consumes 3.5mW, which is a considerable large power budget.

The second drawback comes from the lack of a stable virtual ground at the input of the VCO-based quantizer, thus an active adder has to be introduced to generate the error of the 1st stage noise. Also in [4], this active adder consumes a large power value(2.4mW).

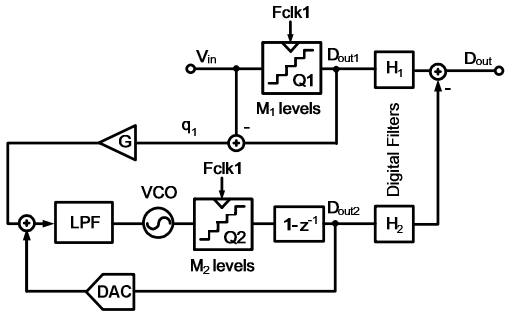

Fig.4Proposed 0-2 MASH with VCO-based quantizer.

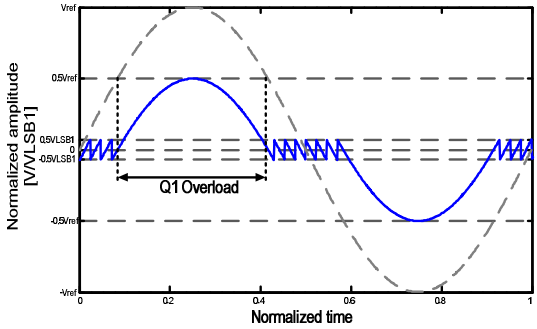

Fig.5Overload range of the 0-2 MASH topology.

III. PROPOSED0-2 MASH WITH VCO-BASED QUANTIZER

A. Proposed 0-2 MASH Architecture

The proposed DT 0-2 MASH with VCO-based quantizer is exhibited in Fig.4. The first stage is composed by a multi-bit flash ADC with M1 level referencewhile a delta-sigma modulator with an integrator and a VCO-based quantizerimplements the second stage.

The number of bits in the 1st stage is directly related with the input of the second stage, which also guarantees the stability of the 0-2 MASH topology [5]. An example of the output q1, as shown in Fig. 4, in the first stage is graphically illustrated in Fig. 5 for asinusoidal input and 8 levels in Q_1. Ifthe input does not overload the first-stage the signal q1 is only the quantization noise of that first stage. While ifthe input exceeds the reference voltage of the quantizer in thefirst stage $V_{ref,Q1}$, the signal in the second-stage will include aninput-signal component.However, the modulator is stillstable and operational after overloading Q_1 as long as themaximum input-signal level into the 0-2 MASH topologyis smaller than,

$$x_{max} = k\frac{V_{ref,Q2}}{G} + V_{ref,Q1}(1 - M_1^{-1}) \qquad (2)$$

where k is a constant ranging from 50 to 80% [4] whichdepends on the loop order and number of bits in the quantizerQ_2, and G is the inter-stage gain thatis bounded by the reference voltages of Q1 and Q2 as calculated below,

$$G \le k\frac{V_{ref,Q2}}{V_{ref,Q1}}M_1 \quad (3)$$

When compared with the traditional modulatorwhere the maximum input voltage should be$x_{max}=kV_{ref,Q}$, the stability tolerancebecomes larger by the factor $V_{ref,Q1}(1-M_1^{-1})$.

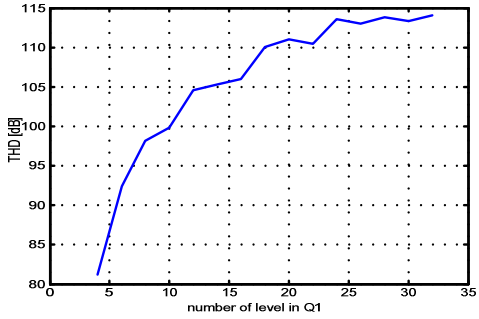

Fig.6 THD versusnumber of bits of Q1.

This means that the 0-2 MASH structure can achieve a good second order noise shaping even with an enlarged signal swing for a small number of levels in thefirst-stage quantizer. Also from Eq.(2), it is possible to conclude thatif the number of levels in the first stage is higher, then this implies enhanced tolerance in the stability of the modulator.

Because the VCO-based quantizer is implemented in the second stage, the linearity of the VCO will introduce harmonics from second stage into the overall modulator, which cannot be shaped by active filters. While the number of bitsin the 1st stage ADC directly determines the residue signal (also the input of the second stage) processed in the second stage, it would be necessary to decide it in advance.Fig.6 illustrates the curve oftotal harmonic distortion (THD)varyingwith the number of bitsin the ADC's 1st stage. From there, it can be deducted that asthe number of bits in the first stage increases, which means that theinput signal swing in the second stage reduces, the THD curve becomes flatten.Furthermore, when the number of bits reaches 16 or is even higher, the THD will no longer dominate the performance, thus promising good linearity.

Since the 1st stage is composed by a flash ADCit implies only a unit transfer function. Therefore, no mismatch between the analog and digital transfer functions will appear. Plus, due to the open-loop intrinsic noise shaping function of the VCO the loop filter is of 1st order. Hence, only a simple unit delay is needed in the digital cancellation. This advantage can also be implemented into higher order in the second stage.

For the DT 0-2 MASH,

$$y = H_1(x+\varepsilon_1) - H_2(STF_{1st}\cdot\varepsilon_1 + NTF_{1st}\cdot NTF_{VCO}\cdot\varepsilon_2) \quad (4)$$

as$NTF_{1st} = NTF_{VCO} = 1 - Z^{-1}$ and $STF_{1st} = Z^{-1}$.

The digital cancellation only contains a H_1 of Z^{-1} and a unit H_2. Hence, the final noise transfer function can become

$$y = Z^{-1}(x+\varepsilon_1) - (Z^{-1}\cdot\varepsilon_1 + (1-Z^{-1})^2\cdot\varepsilon_2)$$
$$= Z^{-1}x + (1-Z^{-1})^2\cdot\varepsilon_2 \quad (5)$$

Similarly, in 0-N MASH, the H_1 can be one order higher than in the original case, which has a function of $Z^{-(n-1)}$.

Besides, the active adder can be eliminated in this structure because it can be combined with the integrator of the second stage. Contrarily to the 1ststage's OPAMP, the requirement of 2ndstage's OPAMP can be greatly relaxed.

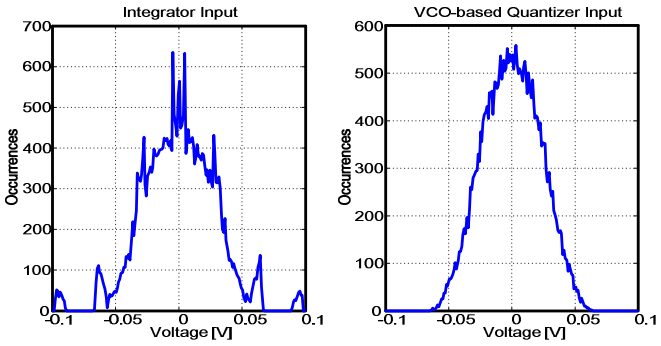

Fig.7 Input swings of the integratorand VCO-based quantizer.

B. Design Example

In the Matlab, we modeled the proposed DT0-2 MASH structure. The sampling frequencyis set at 1.15MHz and the signal bandwidth of the modulator is 10MHz, with the target of designing a modulator with SNDR over 80dB. According to Fig. 6a flash ADC that has over 4-bit in the first stage is chosen for linearity considerations. The inter-stage gain G is equal to 1. The simulated input signalswing of the second stage and input signal swing of the VCO-based quantizerare shown in Fig. 7. As it was mentioned before the swing is small enough for a good linearity of the VCO, which ensures the low distortion characteristic and high SNDR. Besides, due to the relaxed matching between the analog and the digital transfer functions, the OPAMP's requirementsare relaxed.

Fig.8shows the SNDR changing with the gain of the OPAMP in the second stage, where it is shown that when the gain is over 200 the SNDR is stabilized. Since there is only quantization noise in the 1st stage the signal swing of the OPAMP is extremely small, thus reducing its slew-rate requirements. Fig.9 shows the change of SNDR over slew-rate with different levels of the 1st stage ADC, being clear that choosing a higher bit ADC in the 1st stage also enhances the performance. The SNDRversus the Gain-Bandwidth product (GBW) of the OPAMP ispresented in Fig.10. For a GBW over 2GHz the SNDR is almost stable when the first stage quantizer has 16 levels of the reference voltage.

Hence, in the proposed DT 0-2 MASH with VCO-based quantizer a high-bit ADC is necessaryin the first stage, which can bring along benefits both in terms of increased linearity and simplification of the OPAMP in the 2nd stage. However, it is clear thata highernumber of bits in the flash ADC meana largernumber of comparators, and also amore complex DWA circuit inthe DAC. Therefore, the flash ADC in the 1st stage is set to have 4-bit.

IV. Simulation Results

The proposed 0-2 MASH with VCO-based quantizerhas been modeled with MATLAB. A 4-bit flash ADC is implemented in the 1st stage. The OPAMP in the 2nd stage is

modeled with a gain equal to 200(45dB) and GBW equal to 2GHz, which can be achieved with a single stage OPAMP structure.The output spectrum is presented inFig.11where it is shown that the SNDR of the modulator is97dB. Although it can be observed that the harmonics still appear in the signal bandwidth of interest, it is no longer the nonlinearity of the VCO-based quantizer that causes the degeneration of the performance. Instead the negative contribution to it has shifted to the finite gain of the OPAMP in the 2nd stageintegrator. In conclusion, increasing the OPAMP's gain can further enhance the SNDR without any harmonics in the power spectrum, but that will imply higher power consumption. When compared with the traditional 2ndmodulator with VCO shown in red (Fig. 11), the harmonic distortion has decreased by 33dB, and that's really a considerable improvement in VCO's linearity.The detailed summary of modulator's performance is shown in Table 1.

TABLE I

SUMMARY OF THE PERFORMANCE OF THE MODULATOR

Specification	Value
Sampling Frequency	1.15GHz
Input Bandwidth	10MHz
1st ADC	4-bit flash
2nd ADC	5-bit VCO-based
OPAMP gain	45dB
OPAMP GBW	2GHz
Peak SNDR	97dB

V. CONCLUSIONS

A DT 0-2 MASH with VCO based quantizer, that eliminates the loop filter in the 1st stage, to relax the matching requirements, has been proposed in this paper. A 4-bit flash ADC is implemented in the 1st stage, and the linearity of the VCO-based quantizer has been significantly increased due to the small residue input swing. The open loop intrinsic noise shaping function of the VCO-based quantizer allows a significant simplification of the digital canceling filter. Besides, no active adder is necessary in the proposed structure. A design example is presentedand simulated with the corresponding MATLAB model where theproposed modulator can reach a SNDR of 97dB with 10MHz bandwidth at a sampling-rate of 1.15GHz.

ACKNOWLEDGMENT

This work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT).

REFERENCES

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Piscataway, NJ: IEEE Press 2005.

[2] Matthew Park and Michael H. Perrott, "A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time ΣΔ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13µm CMOS", in*IEEEJournal of Solid-State Circuits*,Vol. 44, No. 12, pp. - , Dec. 2009.

[3] Matthew Z. Straayer and Michael H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer", in*IEEEJournal of Solid-State Circuits*, Vol. 43, No. 4, pp. - , Apr. 2008.

[4] Asl, S.Z., Saxena, S.,Hanumolu, P.K.,Mayaram, K., andFiez, T.S., "A 77dB SNDR, 4MHz MASH ΔΣ modulator with a second-stage multi-rate VCO-based quantizer,", in *Proceedings of IEEE CICC,*pp. 1-4, Sep. 2011.

[5] Gharbiya, A., Johns, D.A., "A 12-bit 3.125 MHz Bandwidth 0-3 MASH Delta-Sigma Modulator", in *IEEEJournal of Solid-State Circuits*, Vol. 44, No. 7, pp. - , Jul. 2009.

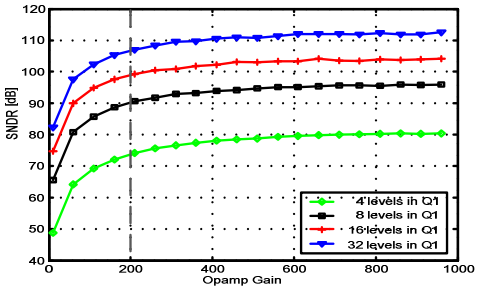

Fig.8Simulated Opamp Gain versus SNDR.

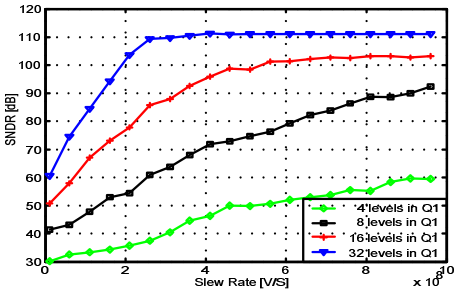

Fig.9Simulated Opamp Slew Rate versus SNDR.

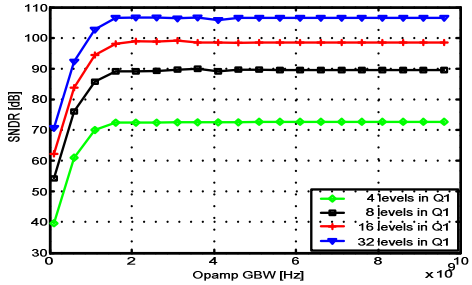

Fig. 10SimulatedOpamp GBW versus SNDR.

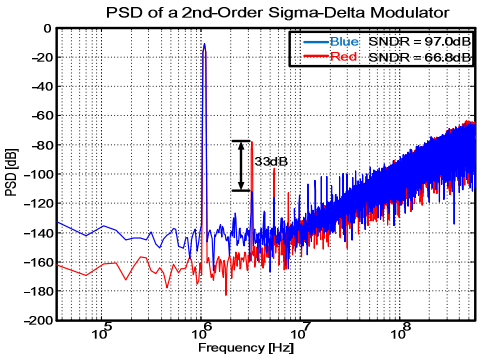

Fig. 11PSD of the proposed**DT** 0-2 MASH structure