# A 12-bit 110MS/s 4-stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique

Rui Wang[1, 2], U-Fat Chio[2], Sai-Weng Sin[2], Seng-Pan U[2, 3], Zhihua Wang[1], Rui Paulo Martins[2, 4]

1. Institute of Microelectronic, Tsinghua University, Beijing, China
2. State-Key Laboratory of Analog and Mixed Signal VLSI, FST, University of Macao, Macao, China
3. Also With Synopsys - Chipidea Microelectronics (Macau) Limited
4. On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

E-mail: raywang0923@gmail.com

*Abstract*—**This paper presents a 12-bit 110MS/s 4-stage pipelined SAR ADC integrated through a single low-gain op-amp. A ratio-based GEC (Gain Error Calibration) technique based on op-amp sharing is proposed to reduce the complexity of digital calibration circuit. Only one PN (Pseudo-random Number) signal is employed to perform the dither injection but calibrate multiple gain errors, and thus accelerates the convergence speed, gets rid of input signal reduction and minimizes the analog modification due to the background calibration. The effectiveness of the architecture is verified in 65-nm CMOS chips whose analog core area is 0.12 mm$^2$ only. The ADC obtains an average SNDR of 63 dB and SFDR of 75.2 dB at 110MS/s consuming analog power of 11.5mW from a 1.2-V supply. Only 40 thousand points are needed to achieve desirable SNDR with the proposed calibration technique.**

***Keywords- SAR ADC; pipelined; digital calibration; op-amp sharing.***

## I. INTRODUCTION

With its intrinsic lower power consumption, pipelined SAR ADC [1] [2] has already become a popular alternative topology for traditional pipeline ADC. The less power dissipation is derived from its simplified MDAC and minimized number of comparators due to the replacement of the flash with SAR in each sub-stage ADC. A single op-amp with two-step pipelined stages is frequently employed in the previous designs [1][2] for pipeline SAR ADC, but is too potentially marginal to achieve both high speed and high resolution (>10-bit) due to small swing of its residue signal. Multi-stage pipeline, on the other hand, has the benefit of gaining more headroom, which is crucial for higher resolution, through the better tradeoff among resolution allocation of each sub-stage, amplification factor for MDAC and magnitude of residue swing. Nevertheless, multiple op-amps are inevitable in the traditional multi-stage pipeline structure, unless time-sharing technique [3] is utilized, which is not applicable for pipeline SAR ADC.

As the silicon technology is keeping on moving towards deeper sub-micron scale, the design of op-amp becomes harder to achieve high open-loop gain by the lower intrinsic gain of transistor and voltage supply. Therefore, using a low-gain op-amp with the digital calibration can keep benefiting from the process downscaling. Several background calibration techniques [4][5] have been proposed for multi-stage pipelined ADCs to compensate low gain of op-amps in digital domain. The equalization-based technique [4] employs a virtual replica ADC in the digital domain using nonlinear interpolation to calibrate the real ADC, but it results in band limited input signal and large hardware for the replica ADC. The dithering-based technique [5] injects a PN pulse sequence to extract errors from MDAC without the input-signal bandwidth limitation. However, it suffers from signal range reduction and long convergence time.

This paper presents a 12-bit, 110MS/s 4-stage pipelined SAR ADC in 65nm CMOS process. A timing-derived technique is proposed to share a single op-amp for residue amplification between pipelined SAR stages, where three non-overlap phases are allocated to maximize both usable bits and op-amp amplification time in each sampling period. Besides, a ratio-based GEC technique based on op-amp sharing is proposed to employ only one PN signal to estimate multiple gain errors by one absolute gain error of the second MDAC and comparative ratios between other MDACs, which accelerates the convergence speed, minimizes the analog modification and digital overhead, and gets rid of input signal reduction due to the background calibration.

## II. PROPOSED ADC ARCHITECTURE AND TECHNIQUES

The block diagram of the proposed pipelined SAR ADC with background digital calibration is shown in Fig. 1. It consists of three 4-bit pipelined SAR stages and one 5-bit back-

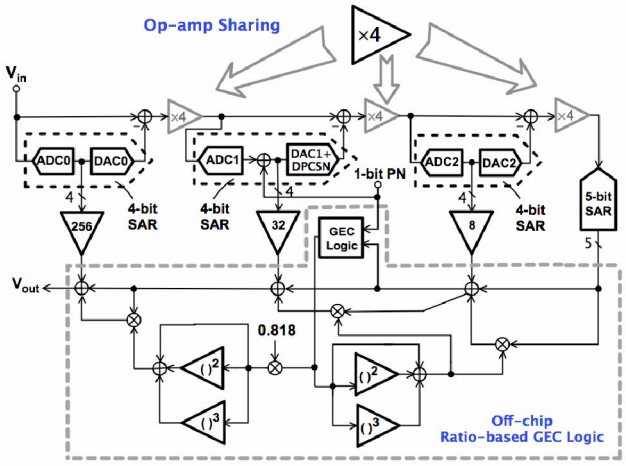


Fig. 1. System architecture

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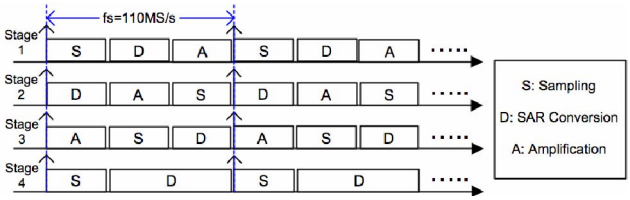

Fig. 2. Timing diagram specified for timing-derived technique

end SAR stage. Besides, with the purpose of lower power consumption, each SAR sub-stage makes use of Vcm-switching technique, and reference buffer free technique to remove reference ladders of all stages [2]. Close-loop gains of the first three MDACs are assigned identically as 4 for a better tradeoff between speed of op-amp and DNL degraded by smaller unit capacitor in MDAC.

Only one op-amp is utilized for amplifications by all four stages through the proposed timing-derived technique in Fig. 2. Due to both of the non-overlapping of amplification phase between each stage and no amplification phase for the last stage as shown in Fig. 2, a single op-amp is shared through four stages incessantly and the last stage exhibits longer SAR conversion time. Besides, three phases of the first three stages occupy the same amount of time for a better tradeoff between the system speed and op-amp linearity requirement. Therefore, the bit distribution pattern that there is the same number of bits in the first three stages and more bits in the last stage is decided from the timing diagram.

In order to alleviate the gain requirement of the single op-amp and boost the system speed, low gain op-amp is used and a ratio-based GEC technique based on op-amp sharing is proposed to calibrate its gain errors rapidly in each amplification phase, which is manifested as the following equations

$$D_{total} = D_{out,4}\times(1+\frac{R_3\times\varepsilon_2}{1-R_3\times\varepsilon_2})\times(1+\frac{\varepsilon_2}{1-\varepsilon_2})\times(1+\frac{R_1\times\varepsilon_2}{1-R_1\times\varepsilon_2})$$

$$+D_{out,3}\times(1+\frac{\varepsilon_2}{1-\varepsilon_2})\times(1+\frac{R_1\times\varepsilon_2}{1-R_1\times\varepsilon_2})+D_{out,2}\times(1+\frac{R_1\times\varepsilon_2}{1-R_1\times\varepsilon_2})+D_{out,1} \quad (1)$$

$$R_i = \frac{1-A_{CL,i}/A_{ideal,CL,i}}{1-A_{CL,2}/A_{ideal,CL,2}} = \frac{\varepsilon_i}{\varepsilon_2} \quad (2)$$

$$\frac{\varepsilon_2}{1-\varepsilon_2} \approx \varepsilon_2+(\varepsilon_2)^2+(\varepsilon_2)^3 \quad (3)$$

where $A_{CL,i}$, $A_{ideal,CL,i}$ and $\varepsilon_i$ is the actual close-loop gain, ideal close-loop gain and estimated gain error of $i^{th}$-MDAC respectively, while $R_i$ is the ratio between the close-loop gain error of the $i^{th}$ and $2^{nd}$-MDAC. Instead of estimating the three gain errors of the MDACs in traditional GEC technique [9], only $\varepsilon_2$ is required to be estimated through GEC logic. Gain errors $\varepsilon_1$ and $\varepsilon_3$ are estimated by multiplying of the absolute gain error $\varepsilon_2$ and the ratios, $R_1$ and $R_3$, which are derived from post-layout simulation. Due to op-amp sharing, the ratio $R_i$ is not sensitive to the uniform variation of both open-loop gain and input parasitic capacitance of the op-amp. Besides, the effect of MDAC capacitors' mismatch on $R_i$ is reduced drastically as long as careful floorplan like using the common centroid layout is utilized.

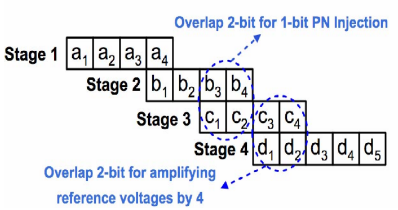

Fig. 3. Bit distribution

Since one absolute gain error is estimated through GEC logic, only one PN signal is injected into only one stage, which exerts less influence on analog circuits, as well as reduces the power overhead and the convergence time of digital calibration. The middle stage is chosen to be injected so as to both relax linearity requirements of op-amp, gets rid of input signal reduction and prevent deterioration of error estimation by noise of latter stages.

In this design, 1-bit dither signal is injected into the second stage through DPCSN technique [6] in digital domain, which cancels the disturbance from the dither injection to the analog operation of the system. Because small-residue-induced SNDR reduction cannot be calibrated digitally, at least 30dB open-loop gain is required to achieve 11.8 ENOB in Matlab analysis based on the GEC algorithm [5]. The $\varepsilon_2/(1-\varepsilon_2)$ in equation (3) is expanded to $3^{rd}$ order of Taylor series to keep this 11.8 ENOB. Due to the low gain op-amp sharing, the signal dependent charge is accumulated in the large parasitic capacitor of op-amp input. Therefore, a reset phase is induced to occupy a short slot of the amplification phase, when the input of op-amp is short to $V_{cm}$ to cancel this memory effect.

With the implementation of the two proposed techniques, bit distribution used in this design is shown in Fig. 3. As the quantization time of SAR ADC is decided by the chosen technology, the maximum speed of the total system is determined by the bit number of each sub-stage. Therefore, less bit number of each SAR sub-stage is preferred to enhance the overall speed. For 12-bit effective resolution with the inter-stage overlapping, the minimum bit number of 4 for first three stages is chosen in the proposed architecture, which renders amplifying reference voltage by 2 in $1^{st}$ stage. For error correction, at least one-bit overlap is needed between two stages. Because the dither signal is injected into $2^{nd}$ stage as mentioned before, there should be two bits overlap between $2^{nd}$ and $3^{rd}$ stage, which causes amplifying reference voltage by 4 for $2^{nd}$ and $3^{rd}$ stages. Since more than four bits in the last stage will not sacrifice the system speed due to its lack of amplification phase, two bits overlap is used between $3^{rd}$ and $4^{th}$ stages. Therefore, 5-bit is used in the last stage and reference voltages of the last stage are amplified by 4.

## III. CIRCUITS IMPLEMENATION

### *A. MDAC Arrays*

The capacitors arrays used in each MDAC of this design are implemented with flip-around architecture [2]. Each capacitive DAC array contains two sets of capacitors: sub-$DAC_C$ is used for Vcm-Switching SAR conversion while sub-$DAC_A$ is for reference voltage amplification and its portion also works as feedback capacitors [2]. According to the bit distribution and close-loop gains of the MDACs, reference voltages of $1^{st}$ stage

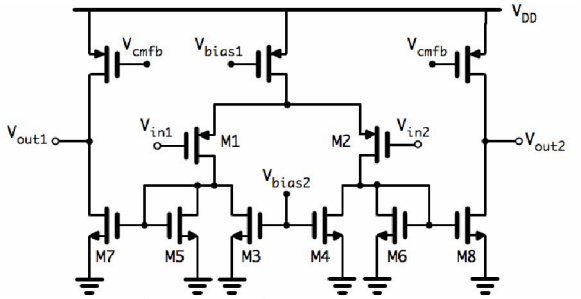

Fig. 4. Low-Gain Op-Amp Structure

are amplified by 2 and of last three stages by 4, which results in total sub-$DAC_A$ capacitances of 16C, 48C, 48C and 48C respectively. Besides, part of sub-$DAC_A$ is folded to the op-amp output so as to realize closed-loop gains of 4. During the SAR quantization, reference buffer free technique is utilized for DAC switching, which gets rid of reference ladders.

From the analysis of KT/C noise, 1.6-pF input sampling capacitors of each side are chosen for 11.7-bit SNR under 12-bit quantization noise, where the value of unit capacitor is 50fF for complying the matching requirement. In order to simplify the design of capacitive arrays, generate more headroom for capacitance mismatch and to induce less KT/C noise from the latter stages' sampling, the total capacitances of the last three stages are designed to be identical, which renders unit capacitance of 10fF in their MDACs.

### *B. High Speed Current-mirror Low-Gain Op-Amp*

As described in the previous section, the open-loop gain of the op-amp should be at least 30dB, and thus a 33dB open-loop gain op-amp is designed here for the requirement. An op-amp with rail-to-rail output is preferred to provide more headroom for higher linearity. With the purpose of achieving higher speed, higher GBW is also demanded. Therefore, in order to realize comparatively higher gain, faster settling speed and rail-to-rail output, a current-mirror op-amp is implemented in this design as shown in Fig. 4.

The open-loop gain is enhanced by the dimension ratios of M3/M4 and M5/M6. The ratio between M5/M6 and M7/M8 are designed to be larger than one in order to increase the GBW of this op-amp. Since the non-dominant pole at the gate of M5/M6 becomes nearer to the dominant pole due to gain enhancement, phase margin can be pushed near the optimum 73-degree to achieve the faster settling and to also tolerate the corner variation. With capacitive loading 1.5pF, an op-amp with a 33dB open loop gain, 2.5GHz GBW and 78-degree phase margin in working bandwidth, is achieved in the post layout AC analysis.

### *C. Gain Ratio Estimation*

Since GBW of the op-amp is designed to satisfy the speed requirement of 1st stage, close-loop gain of each MDAC is described as following equation.

$$A_{CL} = \frac{\left(\frac{C_1 + C_2}{C_1 + C_2 + C_p}\right)}{\frac{1}{A_{OL}} + \left(\frac{C_2}{C_1 + C_2 + C_p}\right)} \qquad (4)$$

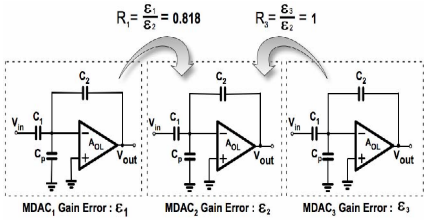

Fig. 5. Gain error ratios between each MDAC

where $C_1$ and $C_2$ is the nonflip-over and feedback capacitance of the MDAC respectively while $C_p$ is total parasitic capacitance in op-amp input and $A_{OL}$ is open-loop gain of op-amp, as shown in Fig. 5. From equations (1), (2), (3) and (4), $R_1$ and $R_3$ is derived. Since $A_{CL}$ of the second and the third MDAC are the same, $R_3$ is equal to 1. From the extraction view in this design, $C_p$ of the first two MDACs and open-loop gain of the op-amp is 439fF, 413fF and 33dB respectively, which renders the ratio $R_1$ 0.818. From the equation (4), if $A_{OL}$ varies from 33dB to 30dB, $R_1$ will only vary 1%; if the sum of $C_1$ and $C_2$, $C_p$ varies 20% respectively, $R_1$ will only vary 2% each. Therefore, capacitors and open-loop gain variation will not influence the ratio $R_1$ more than 5% in total. Besides, in post-layout simulation, the ratio $R_1$ only varies from 0.8155 of FF corner to 0.8205 of SS corner.

## IV. MEASUREMENT RESULTS

The prototype ADC analog circuit is implemented in a 65-nm CMOS process and the die photo is shown in Fig. 6. The chip occupied an active area of 0.12 $mm^2$ and consumes 11.5 mW at 110-MS/s from 1.2 V power supply. Without input signal reduction, its differential input range is full-scale 1.2 Vpp. The estimated power of the off-chip digital calibration under the power supply of 1 V and 110MHz clock frequency is 1.8mW with the estimated area of 0.1$mm^2$, rendering a total power of 13.3mW.

It takes 40 thousand samples, i.e. 0.37 ms at 110 MHz sampling rate, for the gain error to converge to the steady state performance, and the convergence speed is relatively faster compared to most correlation based algorithms [5]. As shown in Fig. 7, with the ratio $R_1$ varies from 0.785 to 0.88, more than 61.5dB of SNDR can still be achieved. The measured DNL and INL without and with calibration are depicted in Fig. 8. The un-calibrated ADC exhibits many missing codes and a peak INL of 16.4 LSB. With Calibration, the peak DNL and INL are 0.421 LSB and 1.63 LSB, respectively.

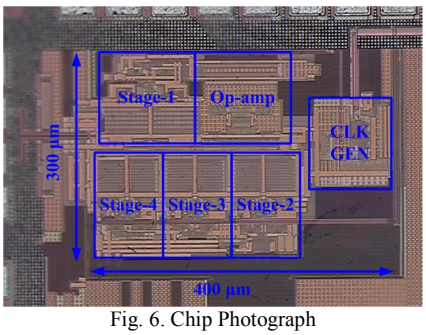

Fig. 6. Chip Photograph

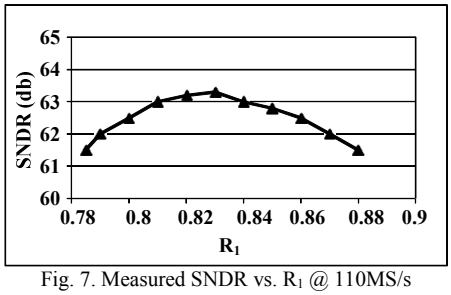


Fig. 7. Measured SNDR vs. $R_1$ @ 110MS/s

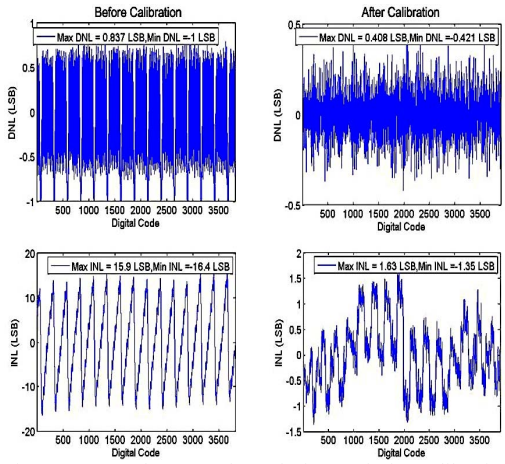


Fig. 8. Measured DNL and INL before and after calibration

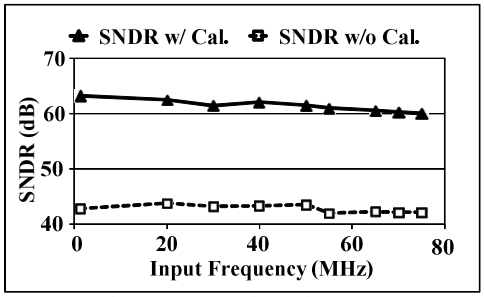


Fig. 9. SNDR vs. input frequency
before and after calibration @ 110MS/s

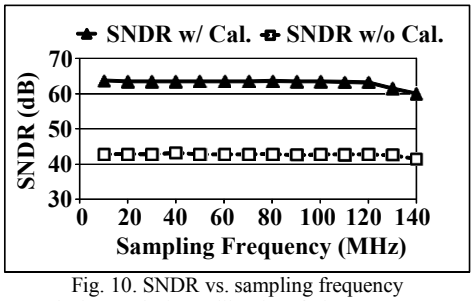


Fig. 10. SNDR vs. sampling frequency
before and after calibration @ $f_{in}$=1.2MHz

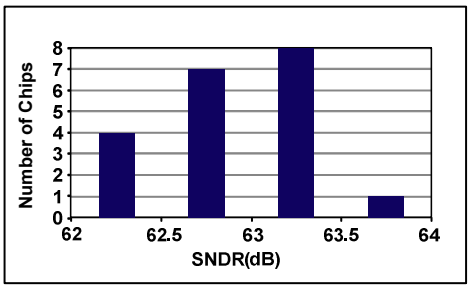


Fig. 11. Measured SNDR among 20 chips @ $f_{in}$=1.2MHz

After the digital calibration, the SNDR improved from 42.8 dB to 63 dB, and the SFDR improves from 49.5 dB to 75.2 dB. Fig. 9 shows the measured SNDR versus the input frequency at a sampling rate of 110 MHz without and with digital calibration, which shows SNDR of 63dB @ 1.2MHz and 61dB @ Nyquist. Fig. 10 shows the measured SNDR versus sampling frequency at input frequency of 1.2 MHz without and with digital calibration. The measured SNDR at 1.2MHz input among 20 chips is shown in Fig. 11 and the average SNDR is 63dB. Table I compares this work with recent reported 12-bit ADC works [4], [7]-[9].

## V. CONCLUSION

This paper presented a low-power 12-bit 110-MS/s 4-stage pipelined SAR ADC in 65-nm CMOS. This new structure features a pipelined-SAR timing-derived technique for op-amp sharing. Ratio-based GEC technique based on op-amp sharing is also proposed in order to accelerate the convergence speed and simplify the complexity of traditional digital calibration.

## REFERENCES


[1] M. Furuta, M. Nozawa, and T. Itakura, "A 0.06mm$^2$ 8.9b ENOB 40MS/s Pipelined SAR ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers,* pp. 382-383, Feb. 2010.

[2] Y. Zhu, C. H. Chan, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti, "A 35 fJ 10b 160 MS/s pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation," in proc. of *IEEE Asian Solid-State Circuits Conference (ASSCC)*, pp. 61-64. Nov. 2011.

[3] Y. C. Huang, and T. C. Lee, "A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique," *ISSCC Dig. Tech. Papers*, pp. 300-301, Feb. 2010.

[4] B. Peng, G. Huang, H. Li, P. Wan, and P. Lin, "A 48-mW, 12-bit, 150-MS/s pipelined ADC with digital calibration in 65nm CMOS", in proc of *2011 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Sep. 2011.

[5] E. J. Siragusa, and I. Galton, "A digitally enhanced 1.8V 15b 40MS/s CMOS pipelined ADC," *ISSCC Dig. Tech. Papers*, pp. 452-453, Feb. 2004.

[6] R. Wang, U F. Chio, C. H. Chan, L. Ding, S. W. Sin, S. P. U, Z. H. Wang, and R. P. Martins, "A Time-Efficient Dither-Injection Scheme for Pipelined SAR ADC," in Proc. of *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PrimeAsia)*, pp. 9-12, Oct. 2011.

[7] B. D. Sahoo, and B. Razavi, "A 12-bit, 200-MHz CMOS ADC," in *IEEE Journal of Solid-State Circuits,* vol. 44, no. 9, pp. 2366-2380, Sep., 2009.

[8] J. Chu, L. Brooks, and H.-S. Lee, "A zero-crossing based 12b 100MS/s pipelined ADC with decision boundary gap estimation calibration," in Proc. of *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 239-240, Jun. 2010.

[9] J.K.-R. Kim, and B. Murmann, "A 12-bit, 30-MS/s, 2.95-mW pipelined ADC using single-stage class-AB amplifiers and deterministic background calibration," in Proc. of *European Solid-State Circuits Conference (ESSCIRC)*, pp.378 -381, Sep. 2010.


TABLE I
PERFORMANCE SUMMERY AND COMPARISONS

| | JSSC'09 [7] | VLSI'10 [8] | ESSCIRC'10 [9] | CICC'11 [4] | This Work |
|---|---|---|---|---|---|
| CMOS Process (nm) | 90 | 90 | 65 | 65 | 65 |
| Supply Voltage (V) | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| Input Range ($V_{PP}$) | 1.2 | 2 | 1.8 | 1.5 | 1.2 |
| Area (mm$^2$) | 1.36 | 0.32 | 0.36 + N/A | 0.78 + 0.21(Est.) | 0.12 + 0.1(Est.) |
| Speed (MS/s) | 200 | 100 | 30 | 150 | 110 |
| SNDR@DC (dB) | 64 | 65 | 65.2 | 67.5 | 63 |
| SNDR@Nyquist (dB) | 61.6 | 63 | 64.5 | 55 | 61 |
| Power (mw) | 348 | 6.2 | 2.63 + 0.32 (Est.) | 36 + 12 (Est.) | 11.5 + 1.8 (Est.) |
| FOM@DC(fJ/conv) | 1340 | 42 | 65 | 194 | 103 |
| FOM @Nyquist (fJ/conv) | 1770 | 53 | 72 | 696 | 131 |