A 10MHz BW 78dB DR CT ΣΔ Modulator with Novel Switched High Linearity VCO-Based Quantizer

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***Abstract*—A novel structure of VCO-based quantizer for CT ΣΔ modulator is presented which can significantly improve the VCO linearity. Compared to the traditional methods, the proposed structure uses only one VCO in the system and it also maintains the intrinsic Dynamic Element Matching (DEM) function of the VCO-based quantizer. A first order CT ΣΔ modulator with the proposed quantizer is designed and simulated in a 65nm CMOS process. The DAC of the ΣΔ modulator is optimized, which can also save half of the DAC cells. The performance of the modulator can reach 69/67 dB SNR/SNDR and a dynamic range of 78 dB with a bandwidth of 10MHz at 1V supply voltage.**

I. INTRODUCTION

Recently, in order to design a competitive sigma-delta (ΣΔ) modulator with high resolution, low power and also wide bandwidth, increasing number of researchers place their attention on the usage of voltage controlled oscillator (VCO) based quantizer. For a ΣΔ modulator design, the VCO-based quantizer seems to be a perfect choice for the intrinsic 1st order noise shaping combined with absence of power-hungry comparator, which is an excellent power efficient characteristic. Besides, the inherited multi-bit quantization and the DEM function are also benefits of a high performance design. However, the nonlinearity of the VCO is a bottleneck for the VCO-based quantizer. In many cases, especially for large input swing, linearity becomes critical with the signal-to-noise-and-distortion ratio (SNDR) of the system even lower than that in normal quantizers.

Several works have been presented to suppress or calibrate this nonlinearity issue. In [1], the linearity of the VCO-based quantizer is improved through a tradeoff of reducing dynamic range; similarly in [2], a feedback was added in the VCO based quantizer leading to an input differential signal that significantly decreases the nonlinearity; however, this approach removes the intrinsic DEM function and the design needs external Dynamic Weighted Averaging (DWA) to alleviate the matching [3]. Recently, a dual VCO structure has been introduced which can perfectly minimize the nonlinearity of the VCO; but the dual VCO structure clearly doubles the size and the power of the digital part [4].

In this paper, a switched controlled VCO-based quantizer is proposed. It can significantly improve the linearity with a large input signal swing, while it maintains the intrinsic DEM function that greatly simplifies the circuit. Furthermore, the proposed structure contains only one VCO in the system. A 1st order CT ΣΔ modulator is designed at circuit level to verify the proposed quantizer and the DEM characteristic. In this modulator, the DAC part is also optimized to save half of the DAC cells. The proposed modulator structure that operates at a clock rate of 575MHz, achieves an SNR/ SNDR of 69/67 dB and a dynamic range of 78dB.

The paper is organized as follows. In section II, the main theoretical aspects of VCO-based quantizer will be reviewed. In section III, the proposed novel VCO-based quantizer combined with the DSP implementation details will be presented, followed by the description of the insertion of the quantizer in a ΣΔ modulator, simultaneously analyzed with the DAC optimization. Next, the simulation results will be discussed in detail in section IV, and finally, the conclusions will be drawn in section V.

II. NONLINEARITY OF VCO-BASED QUANTIZATION

The internal structure of the VCO-based quantizer, shown in Fig.1, uses a multi-phase ring oscillator to achieve the voltage-to-frequency conversion through a mainly digital implementation. As revealed in [2], the D-flip flops and XOR gate operate as counters and register (with no reset), thus allowing high-speed of operation with small latency.

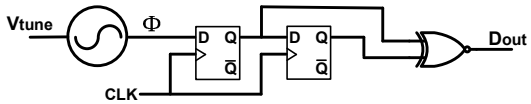

Figure 1. Block diagram of a single-bit VCO-based quantizer.

The tuning characteristic of the VCO cell can be described as

$$\phi_{VCO}(t) = 2\pi K_v \int V_{Tune}(t)dt \quad (1)$$

This work was financially supported by Research Grants of the University of Macau and the Macao Science & Technology Development Fund (FDCT).

where the phase output of the VCO cell is proportional to the integration of the VCO tuning input. The K_v is the ratio of

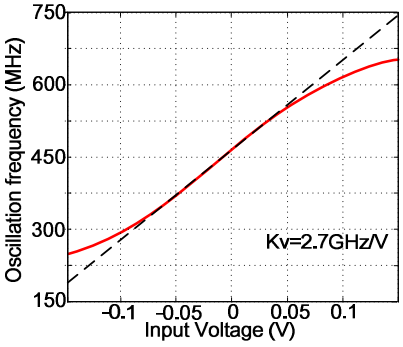

Figure 2. Tuning characteristic of the VCO.

frequency to tuning voltage, which is also the source of the VCO nonlinearity, as shown in Fig. 2. The linearity of the VCO is only good for very small input signal swing (less than 50mv), while the linearity becomes worse for a larger input signal swing.

Therefore, practically, the VCO-based quantizer is not a high performance quantizer due to the serious nonlinearity of the VCO that dramatically affects the performance of the modulator. One of the highest impacts of its nonlinearity is the introduction of harmonic distortion that can significantly degrade the performance of the quantizer. Further tests within the CT ΣΔ modulator show that this nonlinearity will enhance the noise floor when mismatch and nonlinearity in the DAC feedback are increased. Then, the nonlinearity of the VCO-based quantizer has always been considered as the most important bottleneck limiting the attainment of high resolution by the VCO-based quantizer.

III. PROPOSED VCO-BASED QUANTIZER

In this paper, we propose a switched controlled VCO-based quantizer that can significantly increase the linearity of the structure. Compared to precedent methods, this can achieve a larger input dynamic range and maintain the intrinsic DEM function without any additional digital calibration. Furthermore, the proposed quantizer is implemented in a first order ΣΔ modulator. The DAC structure of the modulator is optimized to reduce half of the DAC cells.

A. Switched controlled VCO-based quantizer

Fig. 3 shows the proposed structure of the switched controlled VCO-based quantizer. The quantization part contains a ring oscillator with 31 inverters and a counter to transform the phase signal into a digital code. The quantizer implements a feedback path with a switch producing two operating conditions. The DAC with one cycle delay is combined with a passive adder to generate the second phase input. Finally, a DSP is designed to process the signal outputs of the two phases. The clock frequency of the ADC is 1.15GHz and the frequency of the switch is half of the ADC clock of 575MHz.

According to the block diagram, the timing of switched controlled VCO-based quantizer generates two separated operating phases. As shown in the Fig.4, in the phase 1, the

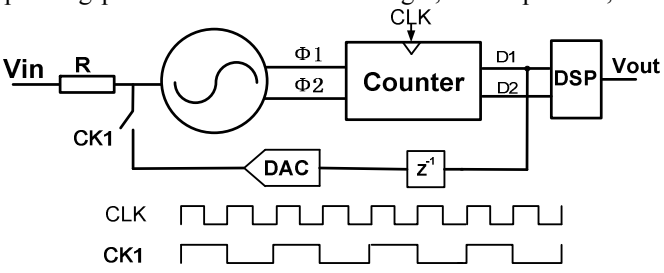

Figure 3. Proposed switched controlled VCO-based quantizer.

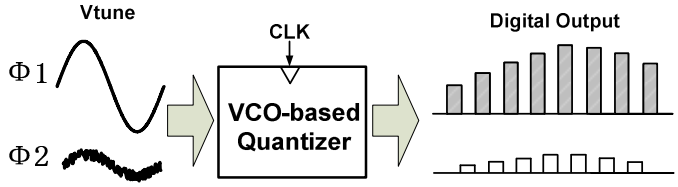

Figure 4. Flow chart of working principle.

feedback path is disconnected. The quantizer works normally, quantizing the input signal, but it generates large output signals with nonlinearity and errors in it. The nonlinearity of the quantizer in phase 1 is denoted as ε_{NL} and the V_{DAC} is the realized feedback voltage, leading to,

$$V_{out}[\phi 1] = V_{DAC}(n) = V_{in}(n) + \varepsilon_{1,NL}(n) + \varepsilon_1(n) \quad (2)$$

Then, in the phase 2, the feedback path is connected with the signal of the phase 1 passing through one delay cycle. With the passive adder, the input of the quantizer includes the noise and the nonlinearity from phase 1. In such a case, the quantizer only processes a very small signal swing in the second phase, due to the better linearity of low input range; the output of the second phase contains a significantly smaller nonlinearity error $\varepsilon_{2,NL}$, as illustrated by,

$$V_{out}[\phi 2] = V_{in}(n+1) - V_{in}(n) - \varepsilon_{1,NL}(n) - \varepsilon_1(n) + \varepsilon_2(n+1) + \varepsilon_{2,NL}(n+1) \quad (3)$$

where the input signal is related to the new period and the quantizer introduces a new quantization error. Until now, the quantizer output becomes interleaved: one phase is the nonlinear output of the quantized input signal; while another is the highly linear part of the quantized nonlinearity from the previous phase.

After that, a DSP is developed to merge the interleaved digital signal from two phases. More importantly, the output of the high linearity signal in the second phase can accurately cancel the nonlinearity part of the first phase output. Then, the high linearity characteristic can be written as,

$$V_{Qoutput} = V_{out}[\phi 1] + V_{out}[\phi 2] = V_{in}(n+1) + \varepsilon_2(n+1) \quad (4)$$

Due to this two phases working function, if the quantizer saturates in the phase 1 for an over large signal, the quantizer also can work normally in phase 2. Hence, the proposed quantizer has an enlarged dynamic range.

It is worth to note that by these discrete sampling switches, the intrinsic noise shaping function of the VCO disappeared. The reason is that a continuous input signal is necessary for the VCO-based quantizer to propagate the noise residue, which imposes also the intrinsic noise shaping

feature. In our design, for the hopping input of the quantizer, the propagation of the noise residue is weakened. However, for the whole ADC, the influence of the nonlinearity of the VCO-based quantizer has a larger dominance; the linearity of the quantizer is improved by compromising this trade off.

B. DSP design

As we introduce a slower clock which is two times of the previous period to control the pair of the switches in front of the VCO-based quantizer, the sampling frequency of the proposed quantizer has to be divided by 2, in our design it is 575MHz; correspondingly, the oversampling ratio is also halved. Here, a DSP block is proposed and designed with a transfer function of $1+Z^{-1}$ to merge interleave output signals with the continuous, which can be easily implemented with a D-FF.

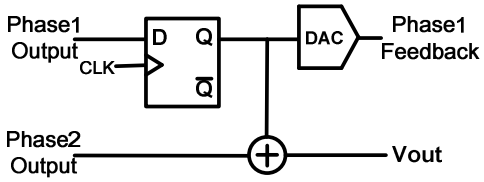

Figure 5. DSP realization.

Fig. 5 clearly illustrates the realization of the proposed DSP. A D-FF is introduced to provide one-delay feedback of the phase 1 output which combined with the phase 2 output will realize the $1+Z^{-1}$ function.

C. Sigma-delta modulator with the proposed quantizer

The proposed switched controlled VCO-based quantizer is implemented in a 1st order CT ΣΔ modulator, as shown in Fig.6. We choose an RC integrator and switched controlled current DAC2 to compose the system. Due to the presence of the DEM in the structure, the DAC2 of the modulator can be easily implemented with a high linearity.

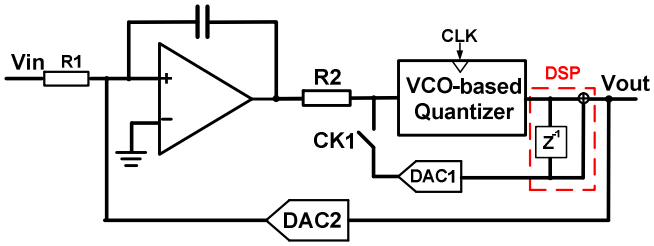

Figure 6. First order sigma-delta modulator with proposed quantizer.

D. Intrinsic DEM maintenance and the DAC design

From Fig.1, each inverter inside the VCO is connected to identical structures of 2 DFFs and one XOR gate. According to [2], the intrinsic DEM is achieved by connecting the single cell of the DAC current source after each XOR gate. The benefit is so obvious that each output level directly corresponds to one current source, so that the DAC linearity can be highly ensured. In our design, the DEM function is maintained as the interleave output signal which can drive an interleaved current output, thus easily implementing one delay cycle.

However, undoubtedly, the drawback of this implementation is doubling the number of the original DAC cells, which causes the consumption of more power and area. Moreover, higher level of feedback is used; and additional mismatch effect will affect the performance of the circuit. Here, we propose an optimization technique to eliminate the number of the current cells and also increase the performance of the modulator. For a VCO-based quantizer, the VCO cells structure already decided the phase error, as given by,

$$\varepsilon_{\phi} = F(N_p) = \frac{1}{12}\left(\frac{2\pi}{N_p}\right)^2 \frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3 \quad (5)$$

where the N_p is the number of the phase in a multiphase VCO-based quantizer which is decided by the number of single-bit VCO-based quantizer cells (in our design equal to 31). If we fix the OSR of the quantizer, the phase error will only be related to the phase number.

For a multi-phase quantizer, each phase has the same phase error, and the structure can be considered as the combination of multiple one-bit quantizers. Each of them has the noise of a multi-bit quantizer, but each individual input is only a fraction of the input signal. In the DAC design, normally, each phase output is connected to one DAC cell and added together to obtain the feedback signal. Fig.7 illustrates the output spectrum of the VCO-based quantizer with 32 level output and 16 level output (only odd levels). It is clear that the noise floors decrease with the same amount of the decrease of the input swing by only choosing half of output levels.

In the proposed design, as shown in Fig.8, only odd cells are selected from the quantizer output. After one cycle delay, another 16 new outputs are achieved. By combining them together, it can accomplish a 32 level output and feedback DAC current. It is quite obvious that this method can save half of the DAC feedback area and power of the sigma-delta structure. Table I below shows the procedure of scaling the output signal and the DAC at the input swing of -1.94 dBFS.

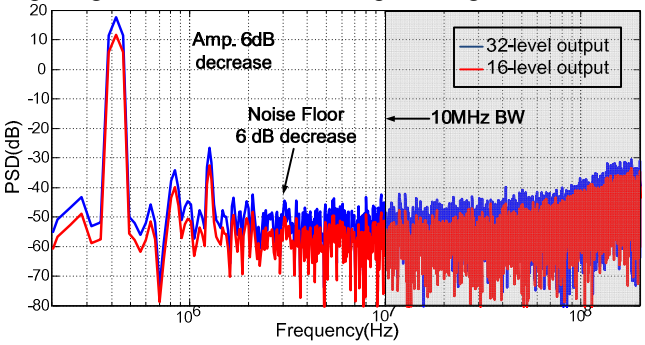

Figure 7. Output spectrum of less-level output.

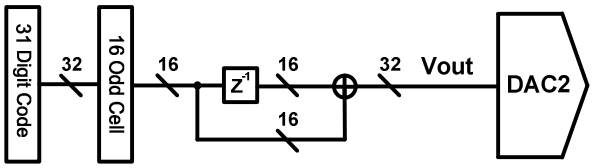

Figure 8. Element elimination of the DAC feedback.

TABLE I - SIMULATION RESULTS WITH DIFFERENT CONDITIONS.

Simulation conditions	THD/SNR/SNDR
Full number of DAC	69/63/63
Half number of DAC	72/68/67

IV. SIMULATION RESULTS

The proposed switched controlled VCO-based quantizer is designed and simulated in a 65 nm CMOS process. The quantizer is a 5-bit with 32 VCO elements, the signal bandwidth is 10MHz and the sampling clock is 575MHz. In our design, with zero input, the K_v around a common-mode voltage of 500mV it is close to 2.7GHz/V. Fig.9 shows the comparison between the output spectrum of the original and the proposed pure-VCO-based quantizer. It is clear that the linearity is significantly improved and the third order harmonic is decreased by 14dB, correspondingly, the total harmonic distortion is increased from 36dB to 50dB. The SNDR of the quantizer increases from 31dB to 43dB (12dB improvement), although the noise shaping is lost due to the reasons mentioned before. The total power consumption of the VCO-based quantizer is 0.965mW.

A 1st order CT ΣΔ modulator using the proposed quantizer with a simplified DAC structure has also been designed. Fig.10 shows the output spectrum of the ΣΔ modulator with the input amplitude of 0.8dBfs and frequency of 0.44MHz. The peak SNR/SNDR can reach 69/67dB with a 10MHz bandwidth and 575MHz sampling frequency. Fig.11 shows the dynamic range of the proposed ΣΔ modulator. Due to the high linearity of the proposed VCO based quantizer, the dynamic range is significantly enhanced, in the order of 78dB. As the input signal decreases, the residue harmonic drops more rapidly, so that the dynamic range is much larger than the peak SNDR. Finally, the summary of the performances of the proposed modulator is shown in Table II.

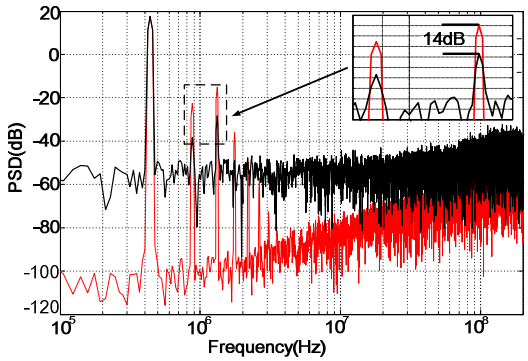

Figure 9. Comparison of output Spectrum between original and proposal VCO-based quantizer

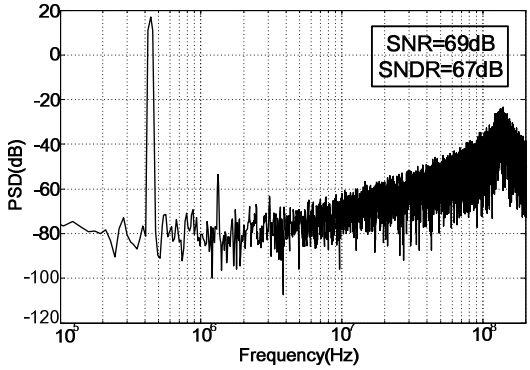

Figure 10. Output spectrum of first order ΣΔ modulator with the proposed quantizer.

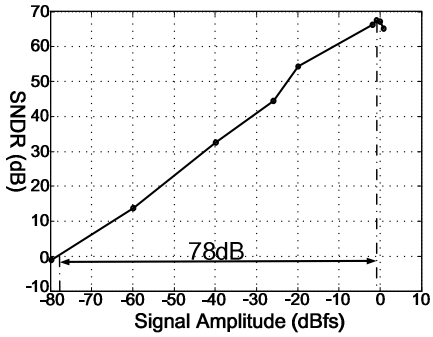

Figure 11. Dynamic Range of the modulator

TABLE II - SPECIFICATIONS OF THE ΣΔ MODULATOR.

Specification	Value
Sampling Frequency	575MHz
Input Bandwidth	10MHz
Supply Voltage	1V
Peak SNR	69dB
THD	72dB
Peak SNDR	67dB
Dynamic Range	78dB

V. CONCLUSIONS

A novel structure of switched controlled VCO based quantizer has been proposed to improve the linearity of the quantizer. It contains only one VCO-based quantizer and can maintain the intrinsic DEM function. A 1st order CT ΣΔ modulator with a switched controlled VCO-based quantizer of 5-bit is implemented in 65nm CMOS. Due to the modification of the DEM function, the DAC structure can be simplified with a highly feedback linearity. Then, the DAC structure is optimized to save half of the DAC current sources for feedback. Furthermore, due to the high linearity of the quantizer, the dynamic range of the modulator is also enlarged. The proposed modulator can reach the SNR/SNDR of 69/67dB and 78dB dynamic range with 10MHz bandwidth, under the supply voltage of 1V and with 575MHz sampling rate.

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