Design Techniques for Nanometer Wideband Power-Efficient CMOS ADCs

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***Abstract* — Aggressive CMOS technology scaling has been driving the design of analog-to-digital converters (ADCs) into new era in which many well-established conventional circuit techniques need to be largely modified to cater for the reduced supply headroom as well as the diminishing intrinsic gain of the transistors. However, the design of ADCs can surely benefits from the technology scaling by smart designs, due to the smaller transistors in nanometer CMOS, which is the key factor that the ADC can manipulate the signals with higher signal processing speed as well as reduced significantly the power consumption. This paper will present the design techniques, including the architectural improvements, power reduction and linearity improvement techniques for successful implementation of various examples of high-speed ADCs with high power efficiency in the state-of-the-art nanometer CMOS technology.**

***Index Terms* — Analog-to-Digital Converters, Successive Approximation, Nanometer CMOS.**

I. Introduction

Data Converters are one of the key building blocks in modern System-on-Chip (SoC) designs due to the need to convert the analog signal in nature for ease of processing in digital domain, and often become the major performance and power bottleneck of such the complete SoC. Innovative researches are carried out in order to improve such interface in four important aspects: resolution, speed, power and area, in the state-of-the-art CMOS technology. Designs in nanometer are preferred that allowed the easier integration of the SoC [1]-[7].

Nanometer designs have obvious benefits in terms of processing speed of the data converters, that makes the signal propagate faster in the logic and analog switches, settle faster in the operational amplifiers, as well as smaller design rules that reduce significantly the parasitics capacitances and resistances. The most major drawback is the drop in the intrinsic gain of transistors – $g_m r_o$ that came from the diminished channel length. As a result, operational amplifier became not quite robust in the nanometer CMOS although it still have speed benefits.

This paper will present the design considerations in nanometer CMOS technology which enable the implementation of wideband power efficient ADCs. The performance of the ADCs in nanometer designs can be improved by either from the innovative architecture improvements, power reduction techniques as well as the linearity enhancement techniques. These techniques help to relax the various design trade-offs that are encountered in nanometer CMOS ADC, especially the limited intrinsic gain of transistors, then the ADC performance can take full benefits from the scaled down transistor sizes and its parasitics. Four design examples will be discussed, with comparison to the state-of-the-art designs.

II. Nanometer ADC Design Methodology

Nanometer transistors suffered from various performance degradation due to the short channel effect, including the velocity saturation, mobility degradation, channel length modulation and Drain-Induced Barrier Lowering (DIBL) etc [8]. They degrade the transistor performance by reducing the effective transconductance as well as the output resistance, as shown in Fig. 1. This is transforming into the intrinsic gain $g_m r_o$ drop although the speed of the transistors ($f_T \propto g_m/C_{gs}$) is significantly improved due to the quadratically diminishing transistor sizes.

It is important to note that ADCs may not always need amplifiers, however the ADC must be capable to move the charges (like those in capacitors, either designed or parasitic) to complete the conversion. One may consider to reduce the usage of the opamp by various techniques, including:

a) Utilizing fully dynamic ADCs;
b) Comparator-/ Inverter-based circuitries;
c) Digital Calibration – that take advantages of digital processing power;
d) Reduce as much as possible the static power consumption.

ADCs that are composed of dynamic components, e.g. the Successive Approximation Register (SAR) [2] and subranging ADC [3] greatly benefits from the improved speed of the technology scaling and they are not heavily

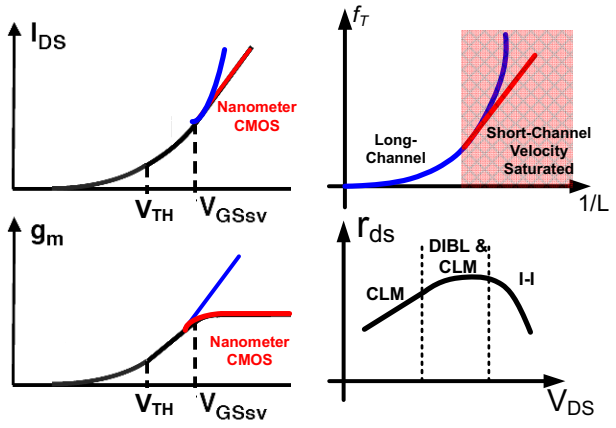


Fig. 1. Degradation of the intrinsic transistor performance in nanometer CMOS.

depends on the gain of the transistors. The design of nanometer CMOS ADCs thus should be oriented by these architectures. While flash-type ADCs the number of comparators increases exponentially with resolution, SAR ADCs are very good candidates in nanometer since they require only full dynamic elements and its key design trade-offs (speed) are mainly related linearly with resolution, and nanometer transistors increases significantly the speed of SAR ADCs. State-of-the-art SAR ADCs can achieve several tens of MHz with very competitive power consumption [2]. On the other hand, to further boost up the speed while keeping the same power effectiveness, architectural improvement or innovative circuit techniques must be adopted, which are presented in the three design examples.

III. NANOMETER ADC DESIGN EXAMPLES (DEs)

A. *DE1 – A 10b 100MS/s Reference-Buffer-Free SAR ADC with Complementary-Converging*

The SAR ADC operation relies heavily on the capability of the reference buffer that drives the capacitive DAC array to perform the SA conversion. The normal SAR ADC requires the reference well within the supply rails (e.g. $0.75V_{DD}$ & $0.25V_{DD}$) thus extra voltage buffers are required. To alleviate this drawback, the complementary converging techniques can be utilized, as shown in Fig. 2 [4]. Instead of the normal SAR that converges the residue voltage to the common-mode, The complementary-converging uses an additional pair of sampling capacitors C_s to sample the same differential input signals of the DACs and, in turn, driving the DAC_s to converge toward $-V_{in}$ instead of V_{cm}. Since the signal that the SA algorithm must compensate is equivalent to 2Vin, it requires reference voltages with value equal to twice of those in the conventional counterpart that allows the DAC to draw the reference voltages directly from the supply rail (V_{DD} and GND as reference sources).This

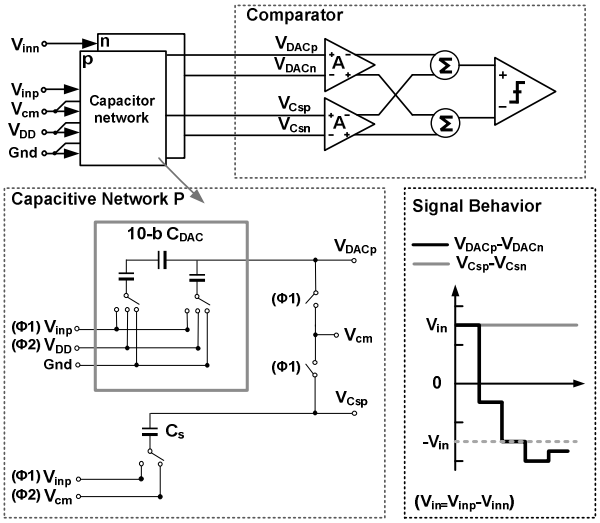


Fig. 2. Complementary Sampling that avoid reference buffer in SAR ADC.

technique eliminates the static power of reference buffer /ladder thus saves significantly the power consumption of the ADCs.

B. *DE2 – A 8b 400MS/s 2b/cycle SAR ADC with Resistive DAC*

This example shows an architectural improvement in nanometer CMOS. An N-bit SAR ADC requires N+1 cycles to complete the conversion, as shown in Fig. 2. This poses the speed limitation of such kind of the architectures, thus 2b/cycle SAR can be adopted that achieves the N/2+1 cycles per conversion (as shown in Fig. 3), thus allows a wideband application [5]. The reference voltage is provided by the resistive ladder which consumes static power, but this design adopted a switched-capacitor sampling front-ends that subtract the input with reference voltage in the high-impedance node at the input of comparators, making the reference ladder only required to drive the various parasitics (from switches and input of comparators). The reference switches are the key limiting factor in terms of speed and power consumption, but the interpolation combine with the nanometer CMOS significantly reduces the switches parasitics and make the ladder consumes only 12% of the total ADC power. Finally, the 3 comparators are offset-calibrated in foreground which also take advantages in robust digital circuits in nanometer CMOS.

C. *DE3 – A 11b 60MS/s Two-Step Pipelined-SAR ADC*

This example shows another architectural improvement. The usage of pipelined-SAR configuration in Fig. 4 can decouple the N-bit resolution into 2 steps, which can allow a more high-speed/low power configuration [6]. The 11b is divided into two 6b sub-SAR-ADCs with 1b overlap for error correction, with residue amplifier in between that composed of opamp. The pipelined operation

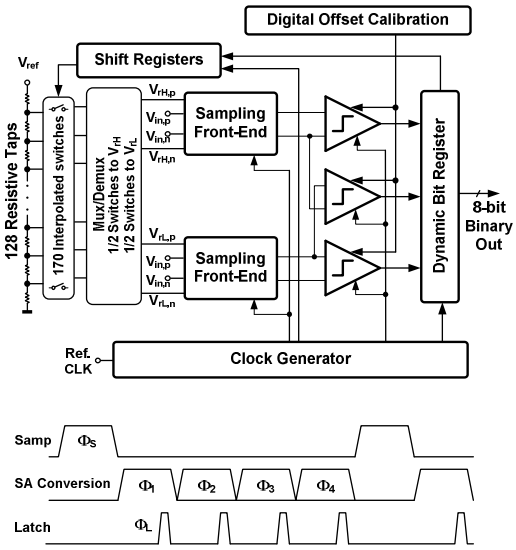


Fig. 3. The 2b/cycle SAR ADC.

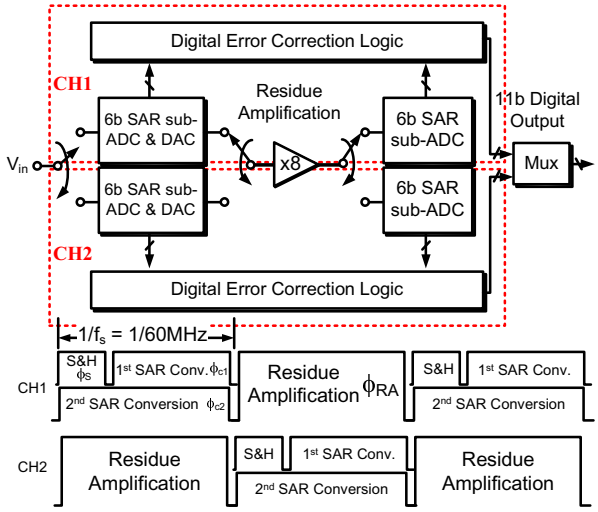


Fig. 4. The time-interleaved pipelined-SAR ADC.

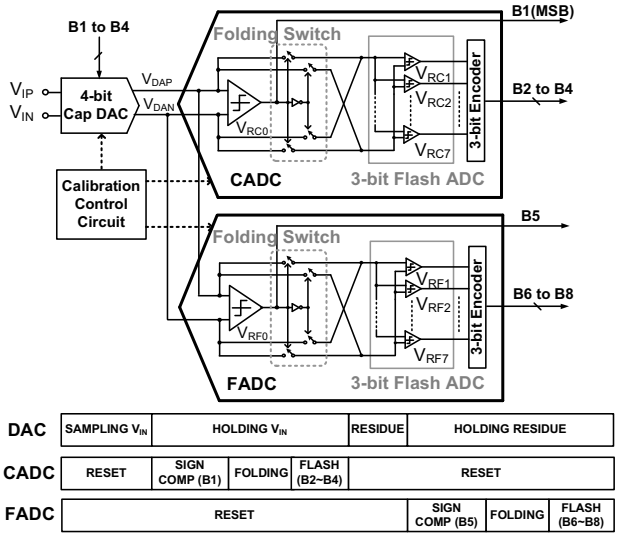


Fig. 5. The subranging ADC with embedded reference and gain-loss calibration.

also enables the 2-channel time-interleaving with shared amplifier. This design intentionally utilized a gain of x8, instead of nominal of x32, which reduces significantly the output swing and allow a telescopic opamp with gain boosting to be used in the amplifier designs. The gain is in the order of $(g_m r_o)^3$ and thus most of the transistors can take advantages with the nanometer CMOS. The opamp is occupied only 14% of the total power of the whole ADC. Indeed the static power from the reference ladder in this designs consume > 67% power of the ADC core, however this power is still quite small due to the relax requirement in the 2nd stages as a result of residue amplifiers as well as the error correction that help relax the sub-SAR errors in the 1st stage. This example shows that the static power is not always a limiting factor in nanometer CMOS ADC designs. The important consideration is to have innovative architectures that relax greatly the requirement imposed on the static power consumption.

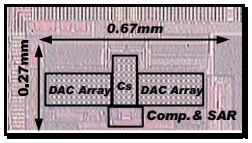
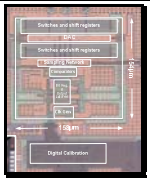
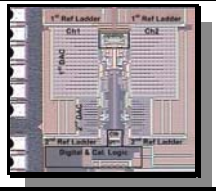
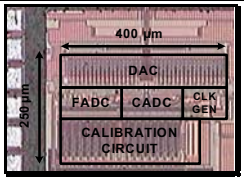
D. DE4 – A 7b 300MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration

This example related with the both architectural and circuit-level linearity improvements. To achieve wideband one may need to consider other architectures like subranging-flash as shown in Fig. 5 [7], which is also a good candidate in nanometer technology due to its fully dynamic nature. The ADC contains a coarse 4b and fine 4b sub-ADC (with 1b overdesign margin) and each sub-ADC consists of 1b folding selection and 3b flash. The residue after the coarse conversion is passed to the 2nd-stage in passive manner that induces a gain-loss due to the parasitics, which degrades the linearity. The gain-loss is calibrated together with the offset of the comparators by the foreground calibration that applies one-by-one the calibrating reference in the ADC front-end, which allows the reference pass through the same gain-loss as the signal and embedded to the threshold of the comparators.

III. Measurement Results and Conclusions

The four design examples are implemented with nanometer CMOS (DE1-90nm and DE2-4 65nm) with the measured results and utilized design techniques summarized in Table 1. The examples utilized the architecture improvements, linearity enhancement as well as power reduction circuit techniques, which lead to either fully-dynamic implementations, as well as the design with large portion of static power, with the Figure of Merit well below 100fJ. Fig. 6 presents the comparison to the state-of-the-art designs, showing the four design examples extending the power effectiveness boundaries, especially for wideband designs.

Table 1. Summary and comparison of 4 design examples with experimental verifications.

	DE1 JSSC'10 [4]	DE2 ISSCC'11 [5]	DE3 ESSCIRC'10 [6]	DE4 ESSCIRC'11 [7]
Technology	90nm	65nm	65nm	65nm
Architecture	1b/cycle SAR	2b/cycle SAR	TI-Pipelined-SAR	Subranging
Improvements for nanometer CMOS	Complementary Converging (Power Reduction Techniques)	Architectural (Speed Improvements) Offset Calibration (Linearity Improvements)	Architectural (Speed Improvements)	Architectural (Speed Improvements) Offset and Gain-loss Calibration (Linearity Improvements)
Resolution	10b	8b	11b	7b
Supply	1.2V	1.2V	1V AVDD,0.85V DVDD	1.2V
Sample Rate	100MS/s	400MS/s	60MS/s	300MS/s
Power	3mW	4mW	2.1mW	2.3mW
Static Power %	5% (from preamp in comparator)	12% (Reference ladder)	81% (Opamp + reference ladder)	0%
SNDR	56.6dB	44.5dB	57.6dB	40.5dB
FoM	55fJ	73fJ	57fJ	88fJ
Area	0.18mm^2	0.024mm^2	0.21mm^2	0.1mm^2
Chip Photograph				

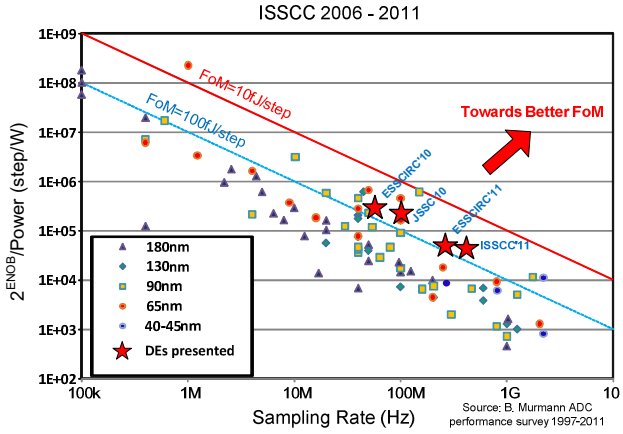


Fig. 6. Comparison to state-of-the-art ADCs

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