Hybrid Loopfilter Sigma-Delta Modulator With NTF Zero Compensation

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***Abstract*—A low power second order hybrid loopfilter Sigma-Delta modulator with high resolution is presented. The structure is composed by a first active integrator followed by a switched-capacitor (SC) integrator. This modulator architecture exploits the coefficient scaling property of the active integrator, while the SC integrator is modified to shift its pole from inside the unit circle to z=1 at DC in the z-domain. Poles of the loopfilter are zeroes of the noise transfer function (NTF). As a result the NTF zero is also shifted to z=1. This NTF zero compensation for the SC integrator will result in better in-band noise suppression & improved noise shaping. The second order hybrid sigma-delta modulator with a 4-bit quantizer and an oversampling ratio (OSR) of 32 is simulated in simulink. The modulator can achieve 89dB SNDR with a dynamic range of 91dB.**

Keywords-component; Sigma-Delta; Switched Capacitor;

I. INTRODUCTION

Low power Sigma-Delta modulator with high dynamic range is a preferred solution to be applied in many portable devices. In sub-micron technology the design of operational amplifier is challenging due to the need of stacking transistors within a 1V supply voltage. The passive switched-capacitor (SC) integrator [1]-[2] constitutes an alternative to avoid the power-hungry operational amplifier. Then, the loopfilter can be implemented only with switches and capacitors, presenting a simple circuit structure and consuming no power when compared with the operational amplifier. The SC integrator does not provide any gain rather than a loss factor which implies, in turn, a small swing in the loopfilter, and then requiring a large gain in the quantizer. In the SC integrator, its pole lies inside the unit circle, which does not provide better in-band noise attenuation. The poles of the loopfilter are the zeroes of the noise transfer function NTF(z) [3]. Recently, a new technique has been proposed to compensate the zeroes of the NTF(z) for passive sigma-delta modulator [4]. In this paper the technique is extended to compensate the zeroes of the hybrid loopfilter by scaling the operational amplifier coefficient.

Sigma-Delta modulator exploits oversampling and noise shaping to achieve high resolution. The 1st integrator is active with moderate dc gain (40dB) while the 2nd integrator is a SC integrator in the proposed structure. The simulink system level simulation of the overall 2nd order hybrid loopfilter modulator is analyzed for a 3-bit, 4-bit and 5-bit quantizer with an OSR ranging from 5 to 150.

The paper will have the following organization. In section II the basic understanding of the real and the traditional SC integrator are presented. Section III is focused on the proposed SC integrator. Section IV provides the modeling and simulation results, and section V draws the conclusions.

II. INTEGRATOR MODEL - REVIEW

A. Real Integrator Model

The commonly used delaying active integrator has the following transfer function H(z),

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \qquad (1)$$

It has a zero at the origin (z=0) and a pole (z=1) at dc.

B. Passive Switched-Capacitor Integrator

An SC integrator with non-overlapping clock can be implemented by analog switches and capacitors only, as shown,

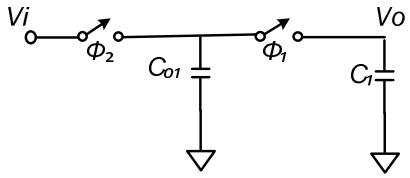

Figure 1. Switched-Capacitor Integrator

The transfer function [5] of the SC integrator is,

$$H(z) = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} \qquad (2)$$

$$\alpha = \frac{C_{01}}{C_1+C_{01}} \qquad (3)$$

Where α defines the ratio of capacitors, imposing the position of the pole on the unit circle, and the gain of the integrator. For stability, the position of the pole will still be at dc but shifted inside the unit circle.

III. Proposed Switched-Capacitor Integrator

A new SC integrator is proposed which removes the leakage effect of a traditional SC integrator, as shown in Figure 2. The integrator model uses a simple adder in front of the SC integrator to compensate the charge leakage. The transfer function of the proposed SC integrator behaves like a real integrator, and the pole of the proposed SC integrator is now shifted to z=1 at dc in the z-domain. The main leakage term in the denominator is cancelled, then leading to a real integrator. A model of the delaying SC integrator is presented to prove the concept.

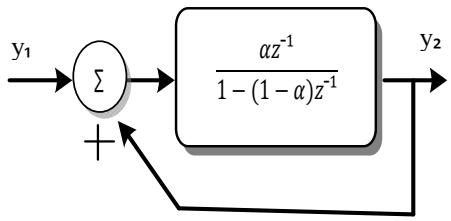

Figure 2. Proposed delaying SC integrator.

And, its mathematical formulation is presented here,

$$y_2 = (y_1 + y_2)\frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} \quad (4)$$

$$y_2\left[1 - \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} y_1 \quad (5)$$

$$y_2\left[\frac{1-z^{-1}+\alpha z^{-1}-\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]}\right] = \frac{\alpha z^{-1}}{[1-(1-\alpha)z^{-1}]} y_1 \quad (6)$$

$$y_2\left[1 - z^{-1}\right] = \alpha z^{-1} y_1 \quad (7)$$

$$y_2 = \frac{\alpha z^{-1}}{1-z^{-1}} y_1 \quad (8)$$

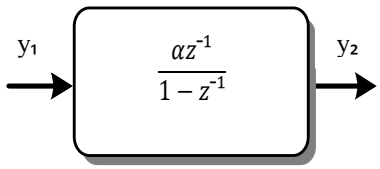

Figure 3. Proposed delay SC integrator (Mathematical model).

Then, equation (8) proves that it becomes a real delaying integrator with numerator coefficient as shown in Figure 3. The pole of the proposed SC integrator is shifted from inside the unit circle to the z=1 at dc.

IV. Modeling And Simulation Results

In this section, a design example of a 2nd-order hybrid loopfilter modulator is presented for the traditional and the proposed SC integrator models.

A. Design Example

A second order hybrid sigma-delta modulator design is simulated in simulink, with the traditional SC integrator as shown in Figure 4. First integrator coefficient a=0.3 is scaled for better performance. The feedback coefficients are A and B while the capacitor ratio α for the SC integrator is 0.18. The signal swing in front of the quantizer is very small, then requiring a large gain G,

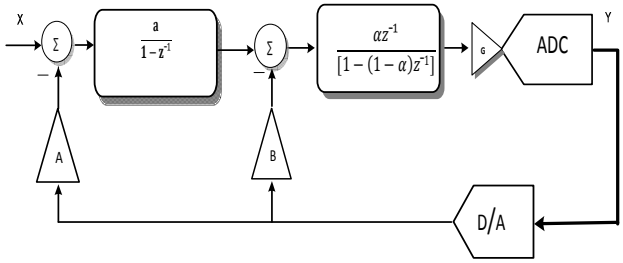

Figure 4. Hybrid modulator with the traditional SC integrator.

The NTF (z) of hybrid modulator for Figure 4 is given by

$$NTF(z) = \frac{[(1-z^{-1})(1-(1-\alpha)z^{-1})]}{D(z)} \quad (9)$$

$$D(z) = [1-z^{-1}][1-(1-\alpha)z^{-1}]+AGa\alpha z^{-1} +BG\alpha z^{-1}[1-(1-\alpha)z^{-1}]$$

Now the modulator model with the proposed SC integrator is shown in Figure 5,

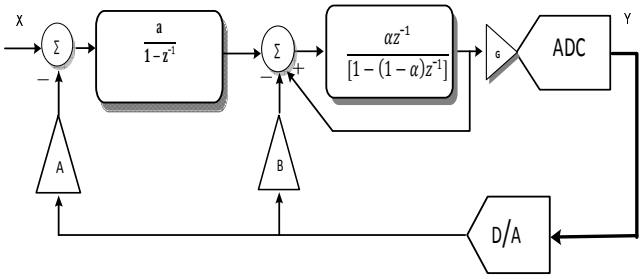

Figure 5. Hybrid modulator with the proposed SC integrator.

The associated noise transfer function NTF(z) of the proposed model, from Fig. 5, is given by,

$$NTF(z) = \frac{(1-z^{-1})^2}{D(z)} \quad (10)$$

$$D(z) = [1- z^{-1}]^2+AG\alpha a\, z^{-1}+BG\alpha\, z^{-1}[1- z^{-1}]$$

The equations (9) and (10) corresponds to the NTF(z) of the traditional and the proposed SC integrator. From (10), the NTF(z) zeroes shift to z=1 at dc in the proposed SC integrator, which eliminates noise from signal band and improves the signal to noise and distortion ratio (SNDR), when compared to the traditional SC integrator.

A system level simulation for performance evaluation of the 2nd order hybrid loopfilter modulator for the traditional and the proposed SC integrator has been performed. As every single bit increment in the quanztier resolution, results in a 6dB SNDR improvement. Then, 3-bit, 4-bit and 5-bit quantizers are known as the most reasonable to evaluate both SC integrator models. Figure 6 and Figure 7 show the simulation results for

OSR versus SNDR as a function of the quantizer resolution. On the other hand, the comparison of the 2nd order hybrid loopfilter modulator output spectrum for both SC integrators types having an OSR of 32 with a 4-bit quantizer, while the input signal amplitude Vi=0.9V is shown in Figure 8.

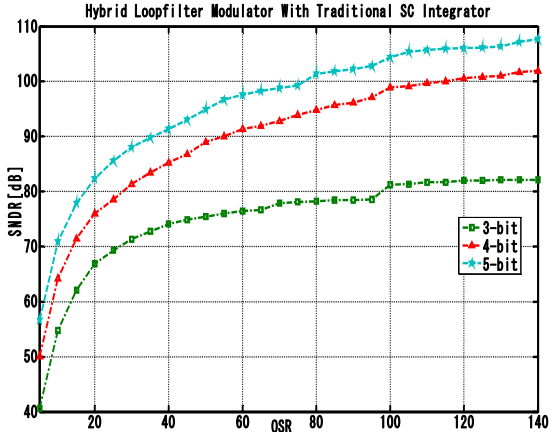

Figure 6. Hybrid modulator with traditional SC – SNDR versus OSR.

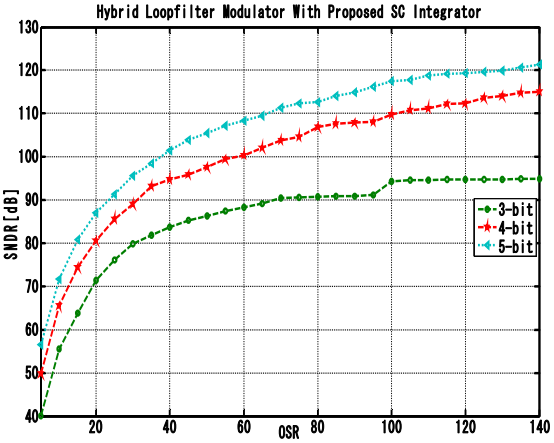

Figure 7. Hybrid modulator with proposed SC – SNDR versus OSR.

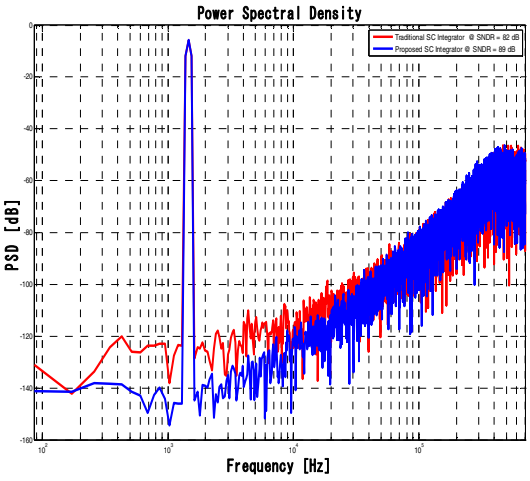

Figure 8. Simulated output spectrum.

Table 1 summarizes and compares some of the results from Figures 6 and 7.

TABLE 1: 2nd Order Hybrid Loopfilter Modulator Comparison between the proposed and traditional integrators.

Specification	Values				
SNDR	86dB	89dB	91dB	83dB	111dB
SNDR Improvement	11dB	7dB	13dB	10dB	13dB
OSR	50	32	80	40	70
Quantizer	3-bit	4-bit	3-bit	3-bit	5-bit

B. Dynamic Range

Here, the dynamic range analysis of the hybrid 2nd order modulator with a 4-bit quantizer and OSR of 32 is presented. The first integrator is active and the second SC integrator is evaluated for dynamic range comparison. The traditional SC integrator dynamic range is about 79dB while the proposed SC integrator exhibits 91dB, as shown in Figure 9.

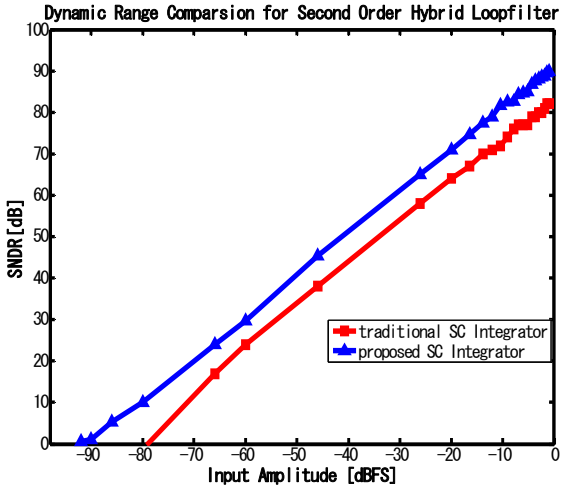

Figure 9. Dynamic range of the 2nd order hybrid modulator.

C. Integrator with incomplete charge transfer

The proposed model of the SC integrator is evaluated here, with a non-ideal effect. As a property of the sampled systems, incomplete charge transfer effect C in the feedback path has been modeled. The parameter C can be used to estimate the charge lost from the output to the input of the switched capacitor integrator. A 2nd order hybrid modulator with OSR of 32 utilizing a 4-bit quantizer containing the proposed SC integrator is shown in Figure 10. Signal-to-Noise and Distortion Ratio (SNDR) degradation due to charge loss is represented in Figure 11. Simulated dc gain of the first active integrator is 40dB for incomplete charge transfer analysis.

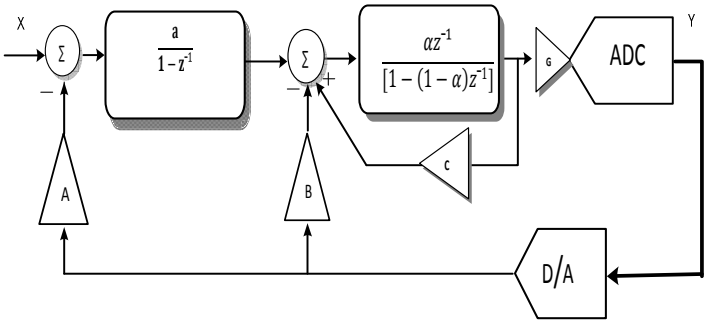

Figure 10. 2nd order hybrid modulator with non-ideal effect.

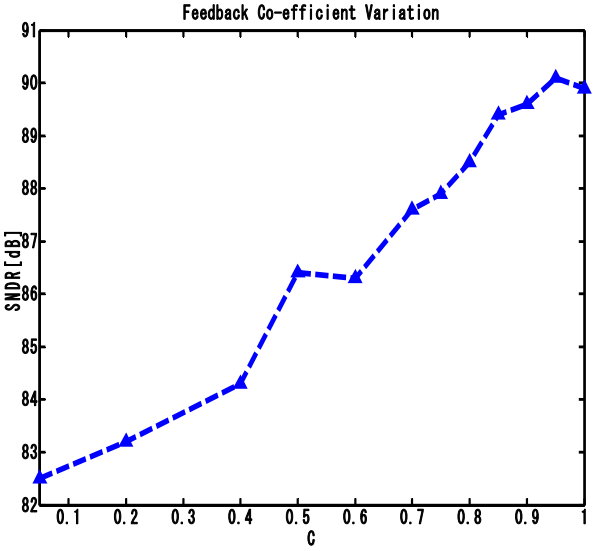

Figure 11. Feedback parameter C versus SNDR [dB].

D. Operational Amplifier

The slew rate simulation of the 2nd order hybrid modulator with an active 1st integrator (with operational amplifier) and the 2nd integrator, as proposed before having an OSR of 32 and a 4-bit quantizer, is analyzed here. The operational amplifier gain causes a shift in NTF zeroes from z=1 to a location inside the unit circle. Thus, causing an increase in the noise floor, and may introduce distortion. The slew-rate causes non-linear distortion in the modulator output spectrum. Figure 12 shows the power spectral density (PSD) of the modulator for different slew rate values. For lower limits of the slew rate more harmonic distortion will be introduced.

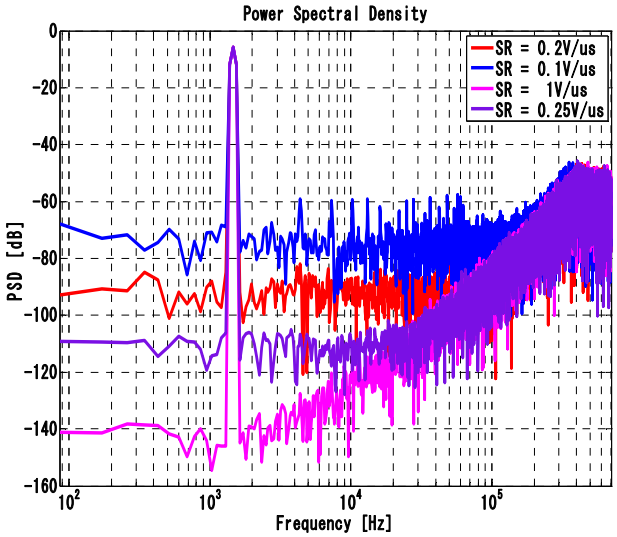

Figure 12. Operational amplifier slew rate effect

V. CONCLUSIONS

A single opamp low power 2nd order hybrid loopfilter modulator has been presented. The modulator achieves 89dB SNDR and 91dB dynamic range with a 4-bit quantizer with an OSR of 32. The opamp coefficient has been scaled for maximum performance while a new SC integrator model was proposed. This, results in a real integrator operation with a numerator coefficient, as a result the zero of NTF(z) for the modulator also changes, which significantly eliminates in-band noise and improves the noise-shaping performance.

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REFERENCES

[1] Feng Chen, Bosco Leung, " A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input", *IEEE J.Solid-State Circuits*, Vol.32, No.6, pp.774-782 , Jun. 1997.

[2] Feng Chen, Srinath Ramas, Bertan Bakkaloglu, "A 1.5V 1mA 80dB Passive ∑Δ ADC in 0.13um Digital CMOS Process," *ISSCC 2003 Dig. Tech. Papers*, pp. 32-33, Feb. 2003.

[3] Richard Schreier, Gabor C. Temes, "Understanding Delta-Sigma Data Converter," , *Willey-IEEE Press*.

[4] Arshad Hussain, Sai-Weng Sin, Seng-Pan U, R. P. Martins, "NTF Zero Compensation Technique For Passive Sigma-Delta Modulator", *Proceedings PrimeAsia 2011,* pp. 82-85, Oct. 2011.

[5] Ramy Yousry, Emad Hegazi, Hani F. Ragai, "A Third-Order 9-bit 10-MHz ΔΣ Modulator with one Active stage", *IEEE Trans. on Circuits & Systems-I,* Vol.55, No.9, pp. 2469-2482 , Oct. 2008.

[6] Tongyu Song, Shouli Yan, "A Low Power 1.1MHz CMOS Continous-Time Delta-Sigma Modulator With Active-Passive Loopfilters", *IEEE Proceedings ISCAS 2006*, pp. 4423-4426 , May. 2006.

[7] Tongyu Song, Zhiheng Cao, Shouli Yan, "A 2.7-mW 2-MHz Continous-Time ∑Δ Modulator With a Hybrid Active-Passive Loop Filter", *IEEE J. Solid-State Circuits*, Vol.43, No.2, pp. 330-341 , Feb. 2008.