A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators

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Abstract—**This paper presents a topology to improve the system linearity and reduce the complexity of high-speed binary-search ADCs. The proposed topology, when compared with previous binary-search ADC architectures, further reduces the number of comparators from 2N-1 to N for N-bit precision, the comparator structure is simplified, and it can avoid both the signal dependent offsets and the kickback noise. The proposed binary-search ADC has been implemented in 65nm CMOS process and it consumes 1.63mW at an operation frequency of 500MS/s. The measurement results demonstrate that the binary-search ADC achieves 30.7dB SNDR (4.8-bit ENOB).**

Keywords-- Analog-to-Digital Converter (ADC), flash ADC, asynchronous binary-search ADC, SAR ADC.

I. INTRODUCTION

Low resolution high-speed ADCs are widely used for wireless communication applications such as ultra wideband (UWB) systems. In recent years, binary-search ADCs **Error! Reference source not found. Error! Reference source not found.** have been proposed for low-resolution, high-speed, low power consumption and small active area design specifications. The binary-search architecture performs the binary-search algorithm [1] to approach the sampled input bit by bit. The first binary-search architecture [1] shown in Figure 1 is similar to the flash ADCs. Instead of activating all 2^N-1 comparators at the same time, it activates the comparators one-by-one, which operates like the SAR ADC [2] such that N comparisons are required for N-bit resolution. In this way, the power consumption and kickback noise is relaxed compared to flash ADCs. On the other hand, it compared with the SAR ADC, the binary-search ADC does not need to wait for the digital feedback loop and DAC settling because the threshold voltages are prepared for multiple comparators for quantization. Therefore, the conversion time is minimized.

The first binary-search ADC architecutre **Error! Reference source not found.** requires 2^N–1 comparators for N-bit resolution. The number of comparators increases exponentially with resolution. The modified architecture **Error! Reference source not found.** reduces the number of comparators to 2N-1 by selecting the reference voltages for the comparators during quantization steps. However, changing the threshold voltages of the comparators for different input signals causes signal depend offset error, leading to non-linearity problems in the overall ADC performance.

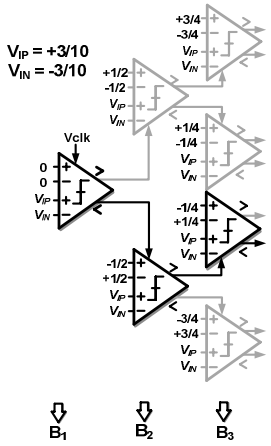


Fig. 1. The first binary-search ADC [1]

Furthermore, both **Error! Reference source not found.** and **Error! Reference source not found.** suffers from the kickback noise of the comparators because the track-and-hold (T/H) is shared among all. Thus, they usually employ large sampling capacitors and a small comparator input pair to eliminate the kickback noise, which is in conflict with a high-speed low-power design approach.

In this paper, the proposed topology further reduces the number of comparators from *2N-1* to *N* for N-bit resolution. The comparator structure is simplified from *4-input* to *2-input*. In addition, the proposed scheme does not suffer from *kickback noise* and *signal dependent offset* problem, so higher ENOB can be achieved.

II. CIRCUIT THEORY

The second binary-search ADC **Error! Reference source not found.** is shown in Figure 2 (a). During the sampling phase, Φ_{SAMP}, the global T/H samples the input voltage, V_{IN}. The quantization starts from the first stage at the first clock phase, Φ_1. After the first stage comparator finished quantizing the MSB, B_1, the first stage comparator outputs, Φ_{U2} and Φ_{L2}, generates the asynchronous clock phase to trigger the comparator of the second stage to quantize B_2. At the same moment, the result of the MSB, B_1, selects the reference voltages for the comparators in the third stage by decoder logic. The ADC keeps quantizing bit-by-bit until the LSB, B_N, is quantized.

This work was financially supported by Research Grants from University of Macau and Macao Science & Technology Development Fund (FDCT).

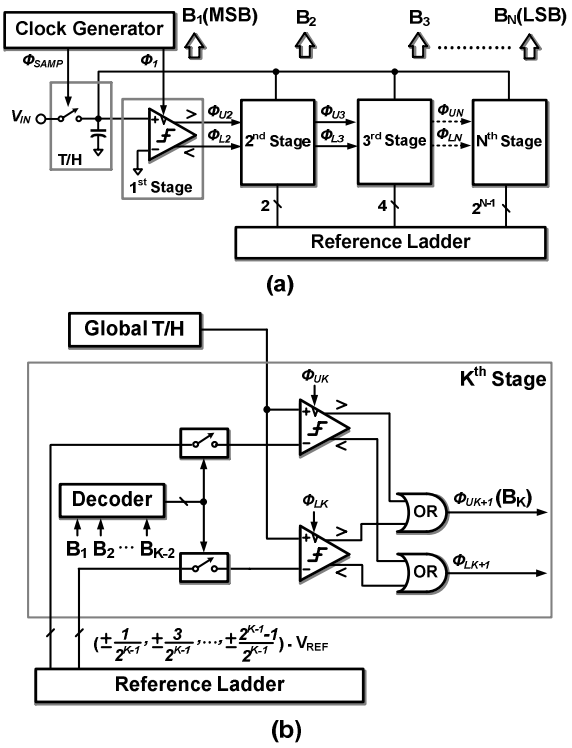


Fig. 2: (a) Block diagram of the second binary-search ADC [2]
(b) Scheme of the K[th] stage.

The first stage comprises only a single comparator. Besides, each stage is constituted by an upper comparator and a lower comparator, a decoder, and two switching networks connecting the comparators and the reference ladder as shown in Figure 2 (b). The comparator outputs are connected to the OR gates to generate the asynchronous clock phases, Φ_{UK+1} and Φ_{LK+1}, in order to trigger the comparator of the next stage.

The block diagram of the proposed binary-search ADC is shown in Figure 3 (a). Figure 3 (b) shows the detail of the K[th] Stage scheme. Each stage comprises one comparator, shared by the two switches, S_{UK} and S_{LK}. The switches are controlled by outputs, Φ_{UK} and Φ_{LK}, of the previous stage. During the sampling phase, Φ_{SAMP}, the switch, S_C, clears the charges remaining on the input of the comparator, so that the memory effect can be prevented.

Comparing to previous binary-search ADCs [1] [2], the proposed architecture can further achieve the significant advantages as below.

A. *Number of comparators*

Using the proposed scheme, each stage comprises only one comparator, instead of two as in [2]. Thus, the number of comparators can be reduced from 2N-1 to N for N-bit resolution. The only tradeoff is the settling speed caused by the switching network, which can be solved by careful design. Reducing the number of comparators saves chip area as well as the effort of the calibration circuit.

B. *Kickback noise*

The circuits in [1] and [2] share the global T/H between the stages. When a comparator is active, there will be a kickback noise injected to the global T/H. Therefore, the size of the input

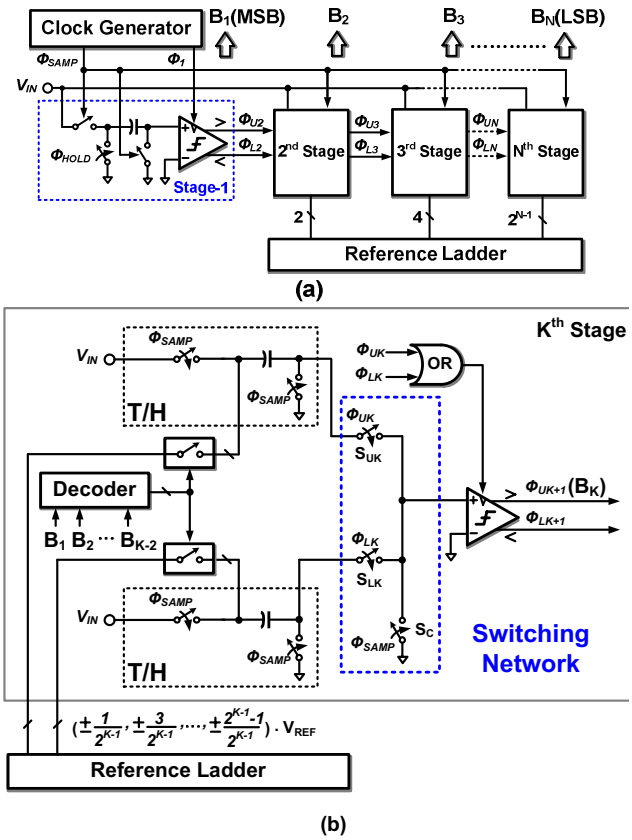


Fig. 3. (a) Block diagram of the proposed binary-search ADC
(b) Scheme of K[th] stage of the proposed binary-search ADC

transistor pairs of the comparators needs to be minimized, thus limiting the current flow through the comparator and its corresponding operating speed. Instead of sharing the global T/H among all stages, the proposed scheme distributes the T/H for each stage. Since the T/H is distributed among different stages, the kickback noise of the comparator is only injected into the T/H of the current stage, but not the next stage. The kickback noise injected to the current stage does not affect the output because the comparator has already quantized the output of the current stage during the kickback. Since the T/Hs are distributed, timing skew must be concerned. By calculation, for 6-bit and input frequency of 700MHz, timing skew within 2ps (feasible to be achieved in nanometer technology effortlessly) is required.

C. *Signal dependent offset*

The circuit structure of [2] utilized the reference prediction to reduce the number of comparators, which changes the thresholds of the comparators by selecting the reference voltages, causing signal dependent offset errors, which cannot be calibrated. Using the proposed topology, all the comparators are calibrated with foreground offset calibration (as shown next) because the threshold of the comparators are fixed.

D. *Comparator structure*

The architectures of [1] and [2] have to employ four input dynamic comparator. Using four input comparators will impose a common-mode error because it is difficult to match the common-mode voltages between the input signal and the comparator thresholds. Therefore, two input dynamic comparator

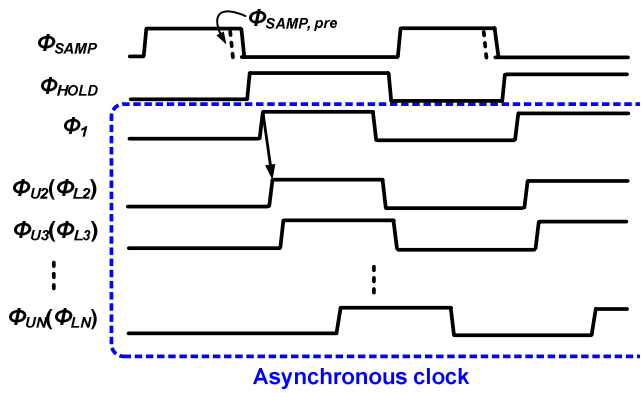


Fig. 4. Clock generation and asynchronous clock phase diagram

is employed in the proposed binary-search ADC for better matching.

III. Circuit Implementation

The following sub-sections describe the circuits that were implemented with the proposed architecture for a 5-bit binary-search ADC.

A. T/H clock and asynchronous clock generation

Figure 4 shows the clock generation and asynchronous clock phase diagram. The clock generation circuit generates the T/H phases, Φ_{SAMP}, $\Phi_{SAMP,\ pre}$, and Φ_{HOLD}, for the T/H circuit to sample the input voltage. The asynchronous clock generates the first clock phase, Φ_1, for the comparator in the first stage by delay of the hold phase, Φ_{HOLD}. After the first bit (MSB) has been quantized, the outputs of the comparator, Φ_{U2} and Φ_{L2}, triggers and activates the comparator of the second stage. The comparator outputs of each stage keep triggering the comparator outputs of the coming stage until the N^{th} stage comparator has been triggered by Φ_{UN} and Φ_{LN}.

B. Comparator architecture and offset calibration

Figure 5 (a) shows the two input dynamic comparator. Once the strobe signal goes low, the memory of the comparator is cleared. While the comparator is activated by the strobe signal, the regenerative back-to-back inverters converts the difference between $V_{in,P}$ and $V_{in,\ N}$ into digital signal. The digital output is then stored before the strobe signal clears the memory. After the regeneration of the back-to-back inverters, the current branches are cut-off from supply to ground, while consuming no static power.

The comparator offset calibration block diagram is shown on Figure 5 (b). The calibration scope is balancing the parasitic capacitance between the input pair **Error! Reference source not found.**. The inputs of the comparator, $V_{in,\ P}$ and $V_{in,\ N}$, must be set to the common-mode during calibration. The flip detector determines the offset polarity at the beginning of the calibration from the comparator outputs. The polarity determines the outputs of multiplexers, MUX, to either connect to the coarse reference ladder or supply. The counter, together with the MUX, controls the reference voltage feedback to the calibration capacitor bank. The feedback voltage adjusts the control voltage, VTD, of the MOS capacitor. Decreasing the control voltage slightly increases the capacitance of the capacitor bank. Thus, the counter counts up to increase the feedback voltage until the comparator outputs

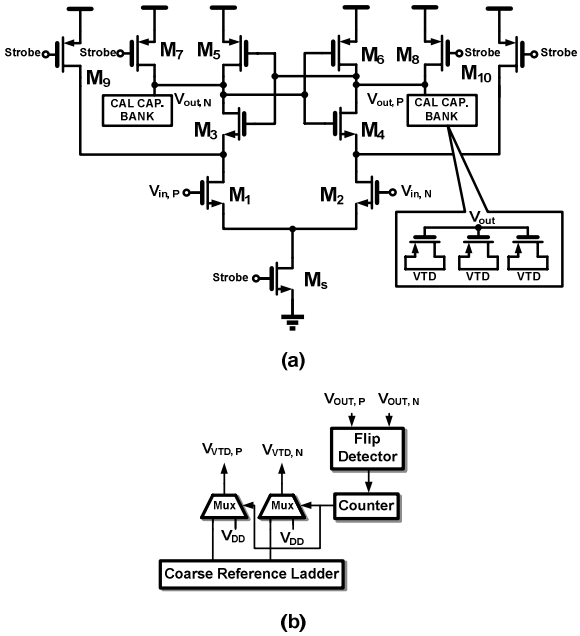


Fig. 5. (a) Two input dynamic comparator scheme

(b) Comparator offset calibration block diagram

are flipped, which means the offset is minimized. Afterwards, the calibration result is stored into the counter, and the whole calibration circuit will be powered-off during normal ADC operation.

C. Distributed T/H

The implemented passive T/H is shown in Figure 6. The sampling scheme utilizes a bottom-plate sampling using three switches, and a 50fF sampling capacitor, C_S. The switches are bootstrapped for higher sampling linearity. The proposed binary-search ADC requires 2N-1 distributed T/H for N-bit quantization.

IV. Measurement Results

The proposed 5-bit binary-search ADC has been fabricated in 65nm CMOS with 1.2V supply. The measurement results demonstrate that the proposed binary-search ADC can operate with 5-bit at 500MS/s consuming 1.63mW of power, resulting in a peak FoM of 117fJ/conversion-step. The analog part, digital part, and reference ladder consume 382µW, 980µW, and 273µW, respectively. At 250MS/s, the ADC consumes 400µW from a 0.8V supply, resulting in a peak FoM of 59fJ/conversion-step. Figure 7 (a) shows the input frequency versus SNDR with and without offset calibration. The ERBW is about 250MHz. Figure 7 (b) shows sampling frequency versus SNDR. Using offset calibration, the DNL is reduced from 1.28 LSB to 0.55 LSB, and the INL is reduced from 0.95 to 0.45 LSB, as shown in Figure 8. Figure 9 shows the FFT spectrum of the proposed binary-search ADC. Table 1 shows the performance summary and benchmark

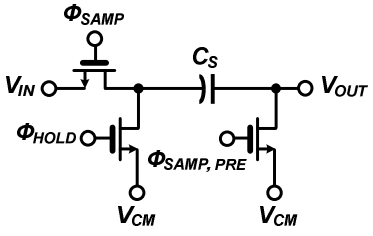
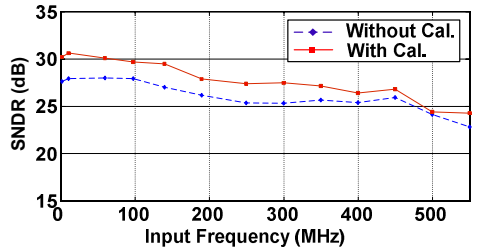


Fig. 6. Distributed passive track-and-hold circuit

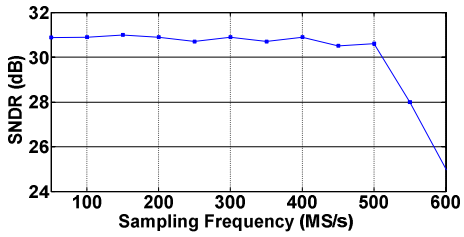
for 5 to 6 bit 500MS/s to 1GS/s ADCs. Figure 10 shows the micrograph of the proposed binary-search ADC. The dimension of the ADC core is 150μm□100μm = 0.015mm^2, where the calibration logic is 86μm□130μm = 0.011mm^2.

V. CONCLUSION

A 5-bit 500MS/s binary-search ADC architecture has been implemented in 65nm CMOS. The proposed architecture reduces the number of comparators from 2N-1 to N for N-bit resolution. Using distributed T/H, the kickback noise effect is avoided without signal dependent offset error, so that the comparator offset can be calibrated by foreground digital calibration. The measurement results demonstrate that the proposed binary-search ADC consuming 1.63mW at 500MS/s, resulting in a peak FoM of 117fJ/conversion-step. At 250MS/s, the ADC consumes 400μW from a 0.8V supply, resulting in a peak FoM of 59fJ/conversion-step. Using offset calibration, the SNDR is increased from 27.9dB (4.3-bit ENOB) to 30.7dB (4.8-bit ENOB).



(a)



(b)

Figure 7. (a) SNDR versus input frequencies at f_S = 500MS/s
(b) SNDR versus sampling frequencies

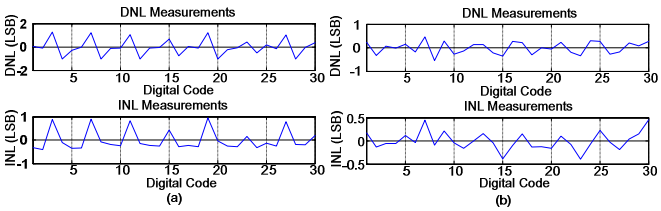


Fig. 8. (a) DNL/INL before calibration
(b) DNL/INL after calibration

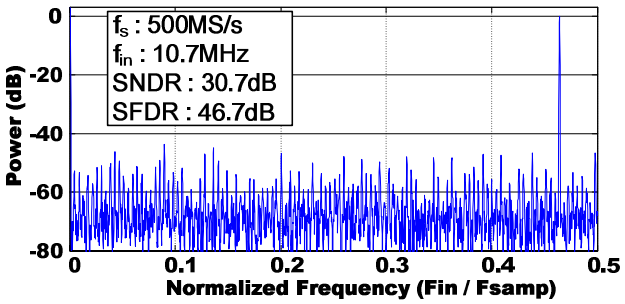


Fig. 9. FFT spectrum with 10.7MHz input (Output Decimated by 25)

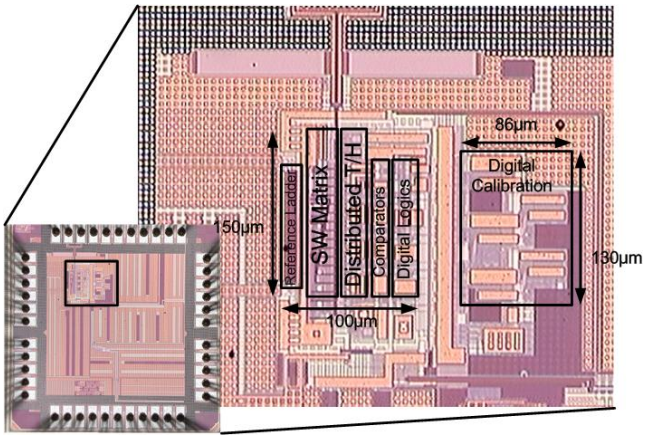


Fig. 10. Chip micrograph

TABLE I
PERFORMANCE SUMMARY & BENCHMARK

	ISSCC'09 [2]		CICC'09 [6]	ASSCC'10 [7]	This work		Unit
Architecture	BS		TI-SAR	Flash	BS		
Technology	65		65	90	65		nm
Supply Voltage	1		1.2	0.5	0.8	1.2	V
Resolution	5		6	5	5		bit
ENOB	4.52	4.4	4.9	4.2	4.8		bit
Sampling Rate	500	800	1000	600	250	500	MS/s
DNL/INL	0.56/0.62		0.4/0.45	0.8/1.0	0.55/0.45		LSB
SFDR	37		NA	38	44.87	46.7	dB
THD	NA		38.9	NA	40.4	41.7	dB
Power	1.39	1.97	6.7	1.2	0.5	1.63	mW
FoM	121	116	210	160	59	117	fJ/step
Active Area	0.018		0.11	0.083	0.015		mm^2
CalibrationArea	NA		Off-chip	Off-chip	0.011 (On-chip)		mm^2

ACKNOWLEDGEMENT

The authors would like to thanks He-Gong Wei for his layout support on floor plan and reference ladder.

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