

art results for medium resolution and conversion speed in the 100-200 MS/s range.

II. ADC ARCHITECTURE

Fig. 1 shows the ADC architecture and timing diagram. The scheme is composed by two interleaved pipelined-SAR ADCs with a residue amplifier shared by the two channels (similar to [1]). Each channel uses 6b and 7b SAR ADCs (2b of the second stage are for offset cancellation) with 1 bit overlapping for digital error correction. The 1st-stage SAR converts the coarse 6b code and generates the residue at top-plate of the DAC, which is amplified by 8 to the 2nd-stage DAC. The 2nd SAR operates in a pipeline fashion while the first stage starts a new cycle. The 6b coarse and the 5b fine codes enter the digital correction logic to build the final 10b output. The two extra bit of the second stage used for offset calibration do not require extra time because the S&H phase is not necessary for 2nd SAR conversion. The gain mismatch between two TI channels determined by the inherit capacitor matching of 1st-stage CDAC is not problematic at 10b, while the inter-stage gain error caused by parasitic capacitance of DACs degrades the conversion linearity, which will be discussed in section IV.

III. OFFSET-CANCELLATION

Time-interleaved architectures augment the conversion rate but suffer from the offset mismatches. These issues can be addressed with various solutions. Sharing the inter-stage amplifier avoids the offset mismatch in the residual generation. The use of digital error correction relaxes the conversion accuracy of the 1st SA decisions from 10b to 7b. Because of the relaxed matching accuracy the 1st-stage comparator offset is calibrated with the unbalanced capacitive loading method [6]. The residue amplification by 8 is a proper trade-off between power limits and accuracy. Since the required conversion accuracy in 2nd-stage is 8b with the offset requirement of 9b, it is necessary to use a more effective offset calibration method.

Fig. 2 shows block and timing diagrams of the 2nd-stage SAR ADC with the implementation of offset-cancellation technique. It is a 7b split DAC array used for both conventional SA conversion and offset measurement. In the calibration mode the input of the stage is set to zero. The output of the 2nd-stage DAC gives rise to the comparator offset with 9b accuracy. The value is stored on a memory to be subtracted afterwards during the normal SA

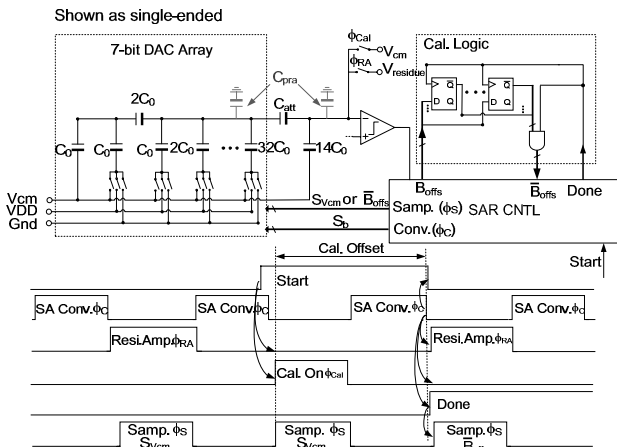


Fig. 2: 2nd-stage SAR ADC architecture and calibration timing diagram.

conversion. As Fig. 2 outlines when calibration is not active (Start=0), the residue is sampled at the top-plate of the DAC by connecting its bottom-plate to V_{cm} during the sampling (Φ_S). Since the input swing is relatively small ($V_{p-p}=1/8V_{DD}$), the top-plate switch is sized smaller to avoid sampling nonlinearity due to the signal dependent charge injection of the switch. When calibration is active (Start=1), the residue amplification phase (Φ_{RA}) is disabled. Both top- and bottom-plates of the DAC are reset to V_{cm} . Since there is no initial charge in the capacitive array, two inputs of the comparator are set to zero. After 7b conversion (Φ_C) is completed (Done=1), the output of the DAC approximates to the comparator offset voltage according to switch control logic S_b , which are locked and stored by 7 flip-flops as offset code B_{offs} . When the next residue sampling phase Φ_{RA} appears the offset cancellation is achieved by switching a 7b complementary offset code at DAC's bottom-plate instead of V_{cm} , consequently, leading to a value of $V_{residue}-V_{offs}$ at the DAC's output for subsequent 5b SA comparison.

The technique allows the maximum offset cancellation range up to full-scale of the 2nd-stage reference voltage and compensates the offset with 1/4 LSB accuracy. The calibration logic, consisting of dynamic flip-flops and AND gates, are easily implemented with small area costs. The offset of the shared op-amp is not cancelled. However, a relatively low value is required as a large op-amp offset, other than causing an overall offset, limits the error tolerance range of the 1st-stage. This design obtains a 3σ input referred op-amp's offset $V_{off-opm}$ well within $1/32 V_{FS-2nd}$ (The $8xV_{off-opm}$ needs be suppressed within $1/4V_{FS-2nd}$), which is achieved by using a large input differential pair operating in the sub-threshold region.

IV. CAPACITIVE DAC AND MDAC DESIGNS

Fig. 3 shows the 1st-stage SAR architecture with the residue amplification. This design utilized a binary weighted DAC with two sub-capacitive arrays DAC_C and DAC_A , each containing 64 units for different functions. During Φ_S the input voltage pre-charges the total DAC array. Then, the DAC_C performs 6b binary-searched conversion, while the DAC_A keeps connecting to V_{cm} that serves as the capacitive-dividing by 2 of the supply to match the required reference level. The solution prevents the use of resistive-ladder/buffer for low power consideration, which is similar to that was done in [2][3], while this work achieve more design benefit from the sub-CDAC for the flip-around MDAC implementation.

After the 6b SA conversion, amplification occurs as a flip-around MDAC. The sub-array DAC_A are separated into $48C_0$ non-feedback units and the other C_{RA} of $16C_0$ that is feedback to op-amp's output for the flip-around amplification by 8. The

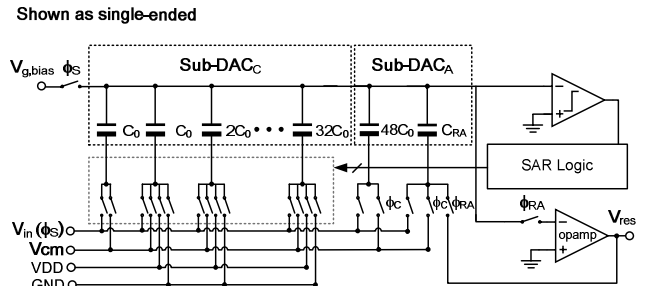


Fig. 3: 1st-stage SAR ADC architecture with flip-around MDAC.

residue amplification is solely depends on the ratio of $\beta=C_{RA}/C_{total}=1/8$, which is decoupled with the resolution of the complete DAC array. This improved feedback factor in pipelined-SAR ADC.

Since two channels share the same op-amp, the DAC reset is at a reference voltage $V_{g,bias}$ instead of op-amp's output. The cost is an offset dependence that is, however, the same for the two channels and is kept at its minimum by design. Thus, the op-amp generates the residual of one channel during the even sampling periods and the residual of the other during the odd periods. The value of the unit capacitor ($5.6\mu\text{m}\times 5.6\mu\text{m}$ equivalent to 13fF) of 1st-stage DAC complies with matching requirements. The total sampling capacitance is 1.66pF.

For the 2nd-stage DAC design the residue amplification by 8 imposes the reference voltages of 2nd-SAR equal to $\pm 1/8V_{DD}$. Since the plain split solution of the 1st-stage would require a too large capacitance that possibly affects the op-amp's slew-rate and GBW requirements, the capacitive DAC in the second stage employs a capacitive attenuator as shown in Fig. 2. The total capacitance to fulfill the 2nd-stage kT/C noise limit is 177fF. The used unit capacitor is ($5\mu\text{m}\times 5\mu\text{m}$) of 10.53fF. The value of the capacitance of C_{att} ($8.9\mu\text{m}\times 8.9\mu\text{m}$ equivalent to 31.25fF) is enough to compensate for the gain error caused by the parasitic of internal and external nodes of the DAC array. Accounting for the foreseeable gain mismatch due to process variation, the expected SNDR degradation is just 0.5dB without gain calibration.

V. CIRCUIT IMPLEMENTATION

Both op-amp and comparator are implemented for low power consideration. The architecture of the op-amp [1] is shown in Fig. 4, which exploits the low output voltage swing by using a telescopic configuration with gain-boost. The control of the current bias enables the tracking of process variations. The used currents keep transistors in the sub-threshold, thus minimizing overheads and making possible a 1.1-V supply. Since the boosting branches must enhance the gain at low frequency they can consume little power, just 7% of the total current burnt by the entire op-amp (700 μ A). The op-amp achieves a low frequency gain of 67dB gain, 1.36GHz GBW and 73 $^\circ$ phase margin with $\beta=1/8$.

Differential dynamic latches without pre-amplifier make the comparators [6] used in this design. Fig.5 shows the schematic of the comparator with NMOS transistors at input. When the strobe is off, there is no current flowing. The relevant nodes are reset to cancel the memory of the previous status. The use of very small

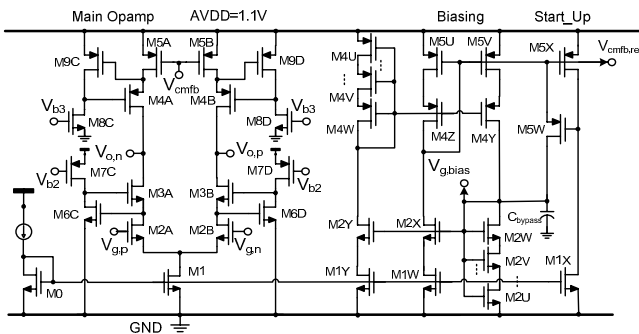


Fig.4: The circuit schematic of the op-amp.

transistors minimizes the parasitic, thus obtaining very high speed even with one LSB imbalance at input. However, a small area of the transistors' gate give rise to large mismatches and, consequently, large input referred offset. Thankfully, the used on-chip offset calibrations compensate for that limit and allow a very low power implementation of the comparators.

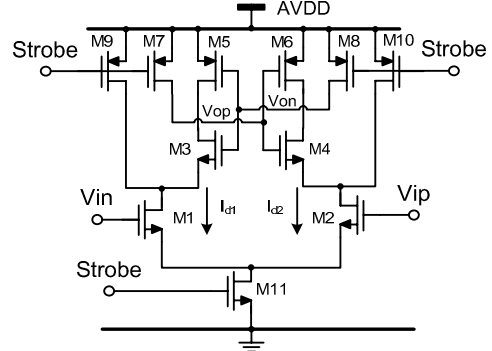


Fig.5: The circuit schematic of 2nd-stage dynamic comparator.

VI. MEASUREMENT RESULTS

The 10-bit TI pipelined-SAR was implemented in 1P7M 65nm CMOS process with metal-oxide-metal (MOM) capacitor. Fig.6 shows the die photograph; the active area is 0.21mm². All the calibrations, including the ones of the 1st and 2nd stage offsets, are implemented on-chip. Fig.7 shows the measured dynamic performances of the combined two and one of interleaved channels. The ADC achieves a SNDR of 55.4dB at 1.5MHz input frequency and loses 3.2 dB (52.2dB) near the Nyquist frequency (79MHz) with a conversion rate equal to 160 MS/s. The channel mismatches denotes a drop of the SNDR by 0.5dB. Fig.8 shows the measured FFT plotted with 1.5MHz input frequency at 160MS/s sampling rate. Fig.9(a) shows the static performance when calibration is not active. The DNL and the INL without calibration are quite large at the full scale of the 2nd SAR that carries a new LSB of 1st SAR. The large errors are due to the comparator offsets that cause the 2nd-stage to saturate. When calibration is active, as shown in Fig.9(b), the DNL improves from 27.6 LSB to 0.46LSB and the INL from 16.7LSB to 1.7LSB.

Table I summarizes the overall measured performance. The analog power consumption is 1.35mW. The digital power including the SAR logic, offset calibration and clock generator is 1.37mW. The total power consumption is 2.72mW at 160MS/s from 1.1V supply. Table II compares the FoM with state-of-the-art pipelined-SAR ADCs. This work achieves the lowest FoM for the considered high-speed.

VII. CONCLUSIONS

Self-embedded offset cancellation and the CDACs for two stage SAR ADCs have been presented. The offset cancellation enables a more relaxed calibration range with less additional offset calibration effort, thus allowing the implementation of high-speed and low-power comparators. The design of CDACs allows both flip-around MDAC amplification and prevents the use of reference generator that consumes static power. The ADC

achieves 8.9b ENOB without any gain calibration. The prototype ADC draws only 2.72mW power from the 1.1-V supply and has a FoM of 35fJ/conv.-step.

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Fig. 6: Die microphotograph of the ADC.

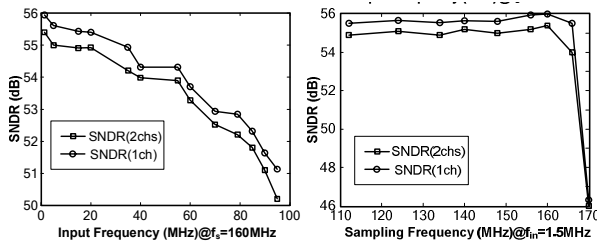


Fig. 7: Measured Dynamic performances.

Table I Summary of performance

Technology	65-nm CMOS
Resolution	10-bit
Sampling Rate	160-MS/s
Supply Voltage	1.1-V
Full Scale Analog Input	1.1-V _{pp}
SNDR	55.4dB
SFDR	61.3dB
ENOB	8.9-bit
DNL	+0.46/-0.3LSB
INL	+1.3/-1.7LSB
Power Consumption	
Analog	1.35mW
Digital	1.37mW
Total	2.72mW
FoM	35 fJ/conv.-step

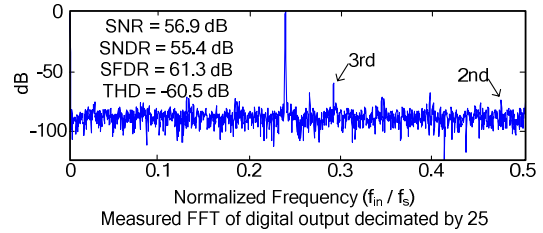


Fig. 8: FFT of the digital output. The input is a 1.5MH sine wave (full-scale) sampled at 160MS/s.

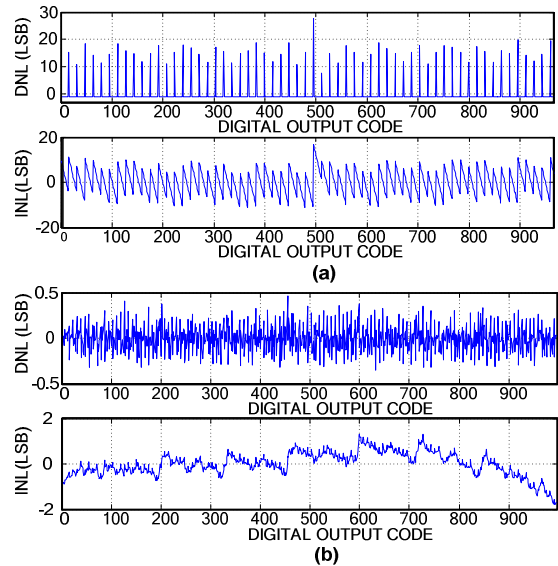


Fig.9: Measured INL and DNL. (a) Without offset calibration. (b) With offset calibration.

Table II Comparison to state-of-the-art works

	[3]	[4]	[5]	This work
Architecture	VLSI' 10 Pipelined-SAR	CICC' 10 Pipelined-SAR	ISSCC' 10 Pipelined-SAR	Pipelined-SAR
Technology (nm)	65	65	65	65
Resolution (bit)	12	10	10	10
Sampling Rate (MS/s)	50	204	40	160
Input Range V _{pp} (V)	2	N/A	1	1.1
Supply Voltage (V)	1.3	1	1.1	1.1
SNDR (dB)	66	55.2	55.1	55.4
ENOB (bit)	10.4	8.87	8.86	8.91
Power (mW)	3.5	9.15	1.21	2.72
FoM (fJ/conv.-step)	52	95.4	65	35