# A Time-Efficient Dither-Injection Scheme for Pipelined SAR ADC

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*Abstract*—**This paper presents a time-efficient dither-injection scheme in digital domain for pipelined successive approximation register analog-to-digital converter (SAR ADC). Compared with the conventional dither injection method, the proposed method can achieve faster injection speed and reduce the disturbance during the quantization of the ADC. Only 1 LSB dither injection is discussed in this method. Simulation results show more than 8 times speed improvement comparing to the conventional configuration.**

***Keywords- SAR ADC; pipelined; digital calibration; dither injection.***

## I. INTRODUCTION

Pipeline ADCs have been the most prevalent topology, which utilize in the aspect of high speed and high resolutions converters designs [1-3]. In order to realize pipelined structure, N-bit resolution ADC usually consists of N stages of flash ADC and N-1 operational amplifiers, which is noted as single bit structure. In the single bit structure, the burden of the precision requirement has been transferred from flash ADCs to the first few stages of operation amplifiers. For relaxing the requirements of operational amplifiers, multi-bit pipeline ADC structure is adopted in [4] where every single stage can contain two types of ADC such as flash ADCs and SAR ADCs. By utilizing flash ADC at each stage, the fastest conversion can be achieved at the cost of lager areas and more comparators, whose existence introduces another nonlinear error in need of the help from dynamic element matching (DEM) technique. As utilizing SAR ADC at each stage, smaller die areas with less power consumptions can be achieved in the tradeoff of conversion speed, whose limit will become less critical due to the trend of technology scaling.

With the target of high resolution ADC implementation in Nano-meter technology, digital calibration has to be applied into the traditional ADC designs. Among the various types of the digital calibration methods, dither injection is one of the popular schemes [5-7]. Dither injection, generally, is used to extract both the information of gain error and nonlinear error of operational amplifiers, which function with digital output codes in certain algorithm to calibrate errors. On the purpose of injecting the calibration signal into the input of the operational amplifiers, dither codes need to be transformed into residues. There are two ways of dither transformation: digital domain and analog domain. Compared with analog domain, digital domain method only requires the modification of the digital circuits with the cost of disturbance to the normal conversion of ADC.

This paper presents a digital-domain dither-injection scheme, which is applied in pipelined SAR ADC. With the proposed scheme, the speed of the dither injection can be increased and the disturbance, which causes by dither injection, to both the regular SAR ADC and operational amplifier operations, is reduced.

## II. DITHER INJECTION FOR PIPELINED SAR ADC

### A. Pipelined SAR ADC architecture

As shown in Fig.1, a pipelined SAR ADC consists of N sub-ADC stages, operational amplifiers and a digital encoder block [8]. Although some modifications are made for adapting to extra phase of amplification for pipelined structure, every sub-ADC is a traditional SAR ADC [9], which contains the SAR logic, the capacitive DAC array and the comparator. Because every sub-stage is one SAR ADC, pipelined SAR ADC can be categorized into multi-bit structure [10]. $V_{ref}$ is the reference voltage and $V_{in}$ is input signal of each stage. The operational amplifier in each stage is used to transfer the residue from the

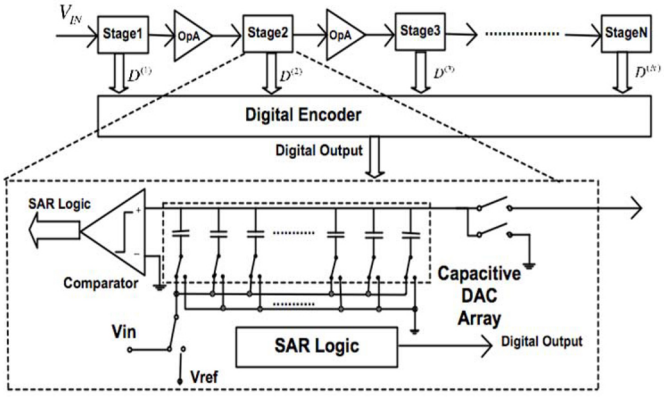


Fig.1. Pipelined SAR ADC without dither injection

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last stage with gain to the next stage in pipeline fashion, which is achieved by feeding part of the capacitors in DAC array to the outputs of the operational amplifier depending on the close loop gain.

### *B. SAR Logic Operation with Conventional Dither Injection*

In order to inject dither signal in digital domain, digital circuits of each pipelined SAR stage have to be modified. Therefore, the modification of each stage is focused on the SAR logic part.

Fig.2 shows a self-timing SAR logic with a conventional dither injection method, which is directly derived from traditional pipeline flash ADC [6]. It includes a pulse generator, shift registers and bit registers. The pulse generator produces the self-timing strobe phase $\Phi_{SAR}$ and activates the shift registers to generate multiple shifted clocks $CLK_1$ to $CLK_n$. The bit registers are turned on/off by the shifted clocks $CLK_1$ to $CLK_n$, which record the conversion result of each bit from SAR ADC and transfer it to switch the DAC through buffers. For the dither injection part, the adders are directly inserted between bit registers and buffers. Besides, the dither signal is required to be ready before the regular SAR operation. Although this structure of dither injection in the traditional pipeline flash ADCs can be effective, it causes significant performance degradation in the pipelined SAR ADC architecture.

Because of the dither addition operation is directly inserted into SAR operation loop, each bit of SAR operation will be affected, which causes extra charging and discharging power consumption. Besides, for the critical path of SAR logic operation, the final bit signal need to pass through a series of n bit adders of each stage in total. Therefore, either the resolution of each stage after dither injection is limited or the whole speed of the pipelined SAR ADC is decreased.

### *C. Delay-reduced Post-dither Code Selection Network*

To avoid the problems in the SAR logic with conventional dither injection, a new technique named Delay-reduced Post-dither Code Selection Network (DPCSN) is proposed, which can directly replace the conventional bit adders group without adjusting other circuits in the SAR logic as shown in Fig.3.

DPCSN provides path one for the bit registers to pass the digital bits from bit registers to buffers quickly, and it also provides path two to perform the dither injection by DPCSN core. Two paths have to be chosen by multiplexers controlled by signal S1. During the first n-1 bits quantization, the path one has been chosen, and the first n-1 bits are not affected by dither injection. Although the DPCSN core is not mingled into the path one, it is still working with the input of both dither and input codes without interrupting the regular SAR operation. After the n-th bit has been generated from comparator, the path two is chosen. Unlike the conventional dither injection method affecting the whole SAR operation, the proposed DPCSN only affects the n-th bit SAR operation. Nevertheless, the following discussion shows that disturbance to the n-th bit caused by dither injection will be greatly reduced through the DPCSN core.

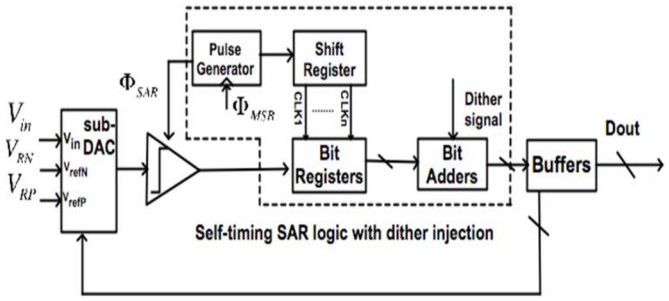


Fig.2. SAR logic with conventional dither injection.

Assuming the sub-ADC is n-bit and the dither of 1 LSB has been injected before SAR operation, where the number of n can be expressed as

$$n = mK + 1 \qquad (1)$$

Formula (1) illustrates that the whole n bits can be divided into m of K bits each with one extra bit and the block diagram of the DPSCN core derived from it is shown in Fig.4:

As shown in fig.4, there are m sub-blocks to synthesize the Code_New<1:n-1>, which stands for Code<1:n-1> through dither injection. Since the final bit of 1 LSB dither signal always equals to one, the polarity of Code_New<n> is always opposite to the polarity of Code<n>. Since there are no related signals between each block, all of the m+1 sub-blocks are independent between each other.

Fig.5 shows the detailed description of i-th sub block of the DPCSN core, which contains two K-bit full adders, one mux group and one XOR tree Traditionally, after Code<iK-K+1:iK> has been generated from i-th sub-stage SAR operation, digital series derived from both dither signal and carry signal of unknown Code<iK+1:n> will affect Code<iK-K+1:iK>, producing complex addition operations. However, the digital series mentioned above can only be three combinations, which are $\underbrace{0\cdots0}_{K-1}1$, $\underbrace{1\cdots1}_{K}$ and $\underbrace{0\cdots0}_{K}$. The first combination happens when Code<iK+1:n> are all ones and dither signal is positive. The second combination happens when Code<iK+1:n> are all zeros and dither signal is negative. In other scenarios, the third combination is satisfied.

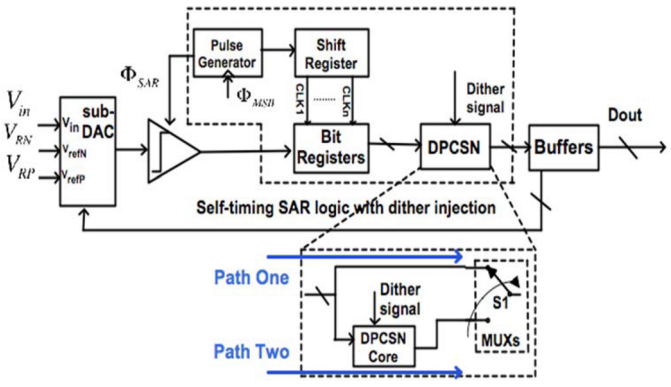


Fig.3. Proposed SAR logic with dither injection.

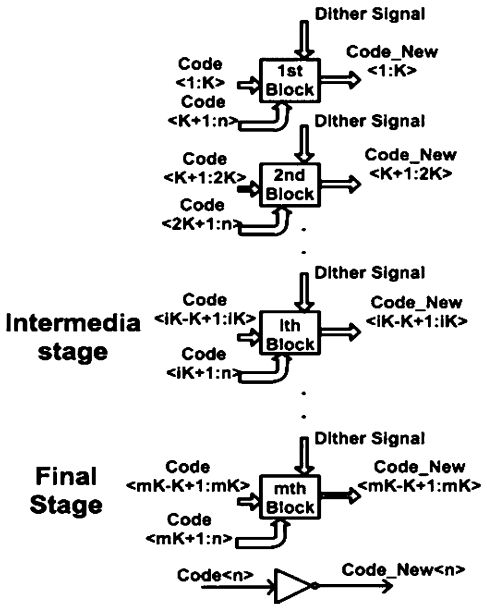


Fig.4. Proposed block diagram of DPCSN core

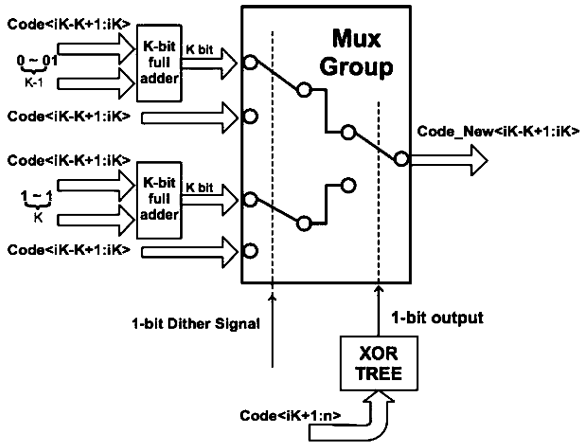


Fig.5. i-th sub-block of the DPCSN core

As shown in Fig.5, the K-bit output codes of the two K-bit full adders and Code< iK-K+1:iK >, which reflect the three possible digital series, will appear at the input of the multiplexers group for the latter digital codes to select from in order to generate Code_New<iK-K+1:iK> directly. Therefore, the addition operation of dither injection in the i-th sub block can be finished before the generation of Code<iK-K+1:n>. Then, only multiplexers operation of selecting the three possible series is needed and thus reduces the penalty of addition operations. However, another selecting signal besides dither signal has to be generated by XOR tree as shown in Fig.6.

From the three scenarios mentioned above, it is noteworthy that the three cases can be distinguished only by the XOR operation of the Code<iK+1:n>. Besides, after realizing that each of the Code<iK+1:n> is generated subsequently, the number of n-iK+1 input XOR operation can be redistributed as a XOR tree in order to minimize the critical path illustrated in red.

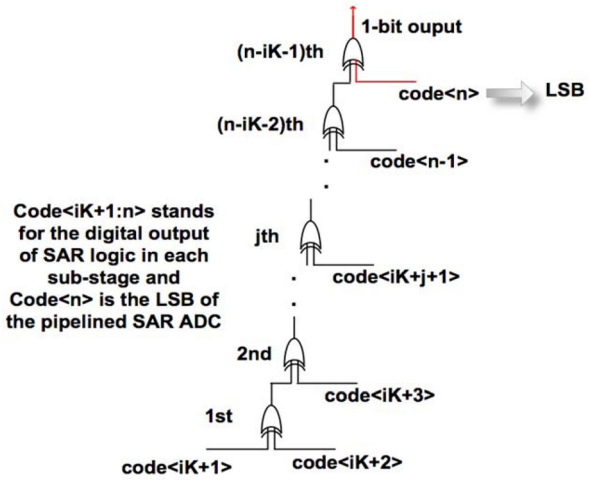


Fig.6. i-th XOR tree

## III. DESIGN STRATEGY OF DPCSN

As the formula (1) illustrated in section II, K needs to be chosen according to both the delay of one-bit adders and the interim between consecutive comparator trigger pulses, whose value is related to the silicon process. To minimize the influence of dither injection, K has to satisfy the condition as below

$$K < \frac{T_{\Delta} - (T_{comparator} + T_{lock})}{T_{adder}} \qquad (2)$$

where $T_{\Delta}$, $T_{comparator}$, $T_{adder}$, $T_{lock}$ denote the period between two consecutive trigger pulses of the comparator, the comparison time of the comparator, the delay time of one bit adder and the time for bit registers to lock the comparator output respectively. Actually, formula (2) demonstrates a design strategy, that addition operation can be distributed into the interim of SAR operation of subsequence bit in order to prevent inserting it into the final SAR operation, which is related to the critical path.

Once the formula (2) is satisfied, the addition operation of the first m sub-blocks had been finished before the Code<N> is generated. Besides, for each sub-block, before the generation of the Code<N>, the inputs of the final XOR gate in XOR tree had been ready. Therefore, the critical path that Code<N> signal passes one multiplexer and one XOR gate is the same for every sub-block. Combining the whole SAR logic and transmission gates are implemented as multiplexers, we can conclude that the delay time of dither injection has been reduced to a couple of inverters' delay plus one multiplexer's, which is much less than the conventional dither injection method.

If the following condition is also satisfied, m>2 can be degraded to m=2 and less sub-block can be used without changing critical path mentioned above.

$$(N-K-1)T_{adder} < K[T_{\Delta} - (T_{comparator} + T_{lock})] \qquad (3)$$

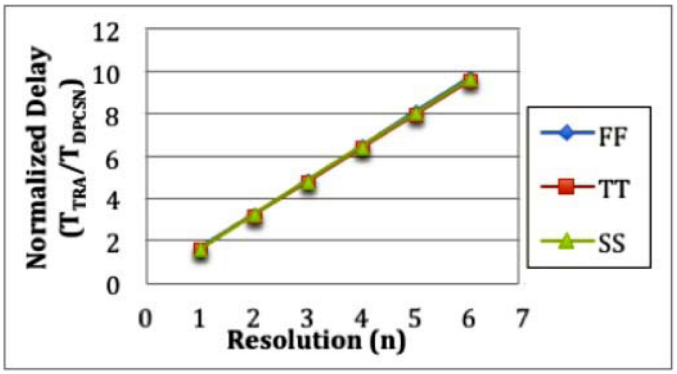


Fig.7 Normalized delay versus the pipelined stage resolution

Formula (3) illustrates that after grouping, addition operation can also be distributed into the interim of the SAR operation of succeeding groups.

## IV. Analysis and Comparison

Assume the resolution of each stage is n-bit in Pipelined SAR ADC. As mentioned in Section III, the critical path of traditional dither injection method is that the n-th bit signal will pass through the whole n-bit full adder and thus affects the additions of previous n-1 bits. Therefore, the delay time after the generation of the n-th bit, $T_{TRA}$ should be:

$$T_{TRA} = n \times T_{adder} \qquad (4)$$

With the implementation of the DPCSN, as long as the formula (2) is satisfied, the critical path of proposed dither injection method is that the final bit signal just passes through one XOR gate, one 2-to-1 multiplexer and one inverter. $T_{inv}$, $T_{mux}$, and $T_{XOR}$ denote the delay time of the inverter, the 2-to-1 multiplexer and of XOR gate respectively. Eventually, the delay time $T_{DPCSN}$ after n-th bit quantization can be expressed as:

$$T_{DPCSN} = T_{mux} + T_{XOR} + T_{inv} \qquad (5)$$

Using the 65nm CMOS technology, the delay of $T_{inv}$, $T_{XOR}$ and T*mux* can be obtained by the post layout simulation. $T_{inv}$ equals to 14ps, 20ps and 25ps with respect to FF, TT and SS corner respectively. $T_{mux}$ equals to 17ps, 24ps and 30ps with respect to FF, TT and SS corner respectively. $T_{XOR}$ equals to 40ps, 50ps and 60ps with respect to FF, TT and SS corner respectively. $T_{adder}$ equals to 115ps, 150ps and 185ps with respect to FF, TT and SS corner respectively. And Then, the delay of $T_{DPCSN}$ is a factor of $T_{TRA}$ by the calculation of (4) and (5). Fig.7 shows the normalize curve of $T_{TRA}/T_{DPCSN}$ versus the pipelined stage resolution n. As the increasing of n, the factor will become bigger, which manifests the benefit of DPCSN furthermore.

## V. Conclusion

This paper proposes a time-efficient dither-injection scheme used by pipelined SAR ADC. This method not only prevents the disturbance of dither injection to the first n-1 bits but also reduces the delay time induced by dither injection to the level of a few inverters, thus minimizes the disturbance to the final bit. As a result, the speed of SAR ADC and settling time of operational amplifiers will not be affected by the dither injection, which speeds up the whole pipelined SAR ADC operation.

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